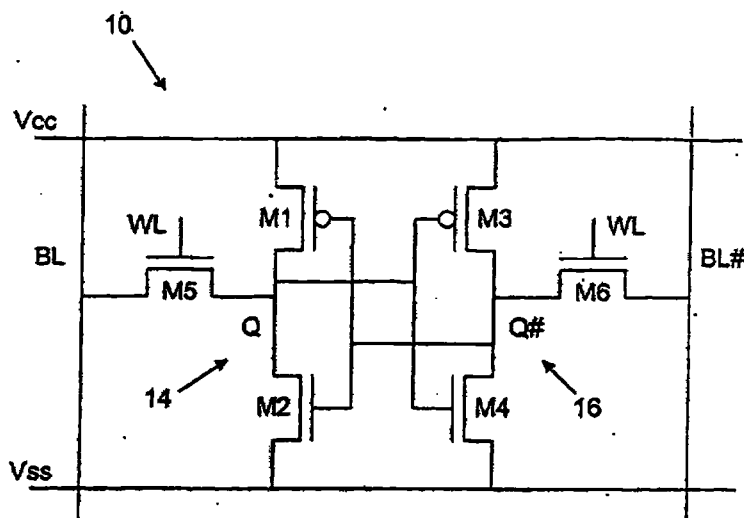




INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification ⁷ : G11C 11/412, 11/418		A1	(11) International Publication Number: WO 00/52702
			(43) International Publication Date: 8 September 2000 (08.09.00)
(21) International Application Number: PCT/US00/04239 (22) International Filing Date: 17 February 2000 (17.02.00) (30) Priority Data: 09/261,915 3 March 1999 (03.03.99) US (71) Applicant (for all designated States except US): INTEL CORPORATION [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95052 (US). (72) Inventors; and (75) Inventors/Applicants (for US only): KESHAVARZI, Ali [IR/US]; 2341 NW Birkendene Street, Portland, OR 97229 (US). ZHANG, Kevin [CN/US]; 14258 NW Tradewind Street, Portland, OR 97229 (US). YE, Yibin [CN/US]; Apartment 332, 3081 NW Overlook Drive, Hillsboro, OR 97124 (US). DE, Vivek [IN/US]; 9785 SW 151st Avenue, Beaverton, OR 97007 (US). (74) Agents: MILLIKEN, Darren, J. et al.; Blakely, Sokoloff, Taylor & Zafman LLP, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025 (US).		(81) Designated States: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG). Published With international search report.	

(54) Title: **DUAL THRESHOLD VOLTAGE SRAM CELL WITH BIT LINE LEAKAGE CONTROL**

(57) Abstract

In some embodiments, the invention includes an integrated circuit including a bitline and a bitline#, wordlines, and memory cells. The memory cells each corresponding to one of the wordlines and each include first and second pass transistors coupled between first and second storage nodes, respectively, and the bitline and bitline#, respectively, the corresponding wordline being coupled to gates of the first and second pass transistors. The memory cells include first and second inverters cross-coupled between the first and second storage nodes, wherein the first and second pass transistors each have a lower threshold voltage than do transistors of the first and second inverters. Wordline voltage control circuitry coupled to the wordlines selectively controls wordline signals on the wordlines. In some embodiments, the wordline voltage control circuitry asserts the wordline signal for a selected wordline corresponding to a memory cell selected to be read and underdrives the wordline signals for the wordlines not corresponding to the selected memory cell.