FORMING MICROSCALE STRUCTURES FROM POLYCRYSTALLINE MATERIALS

The present invention generally relates to the fabrication of microscale or nanoscale structures, such as metallization for microelectronic applications, using polycrystalline materials.

As represented in Figure 1, backend of the line (BEOL) interconnect metallization 10 often includes an electrically-conductive layer 12 of an aluminum- copper alloy that is sandwiched between a pair of diffusion barrier layers 14. The diffusion barrier layers 14 reduce the solid state diffusion rate between the conductive layer 12 and metals from surrounding metal structures, so as to improve the reliability and sheet resistance of the metallization 10. In the past, metallization 10 of this type has been patterned by conventional lithographic techniques to produce various structural features, such as metal pads and lines. While lithographic techniques are widely and successfully used in the art, nanoscale features (i.e., operative structures and components that require a controlled dimension of less than ten nanometers) are difficult to form by conventional lithography. In view of the demand for greater miniaturization of microcircuits and their components, it would be desirable if a method were available that enabled the patterning of metallization to form nanoscale features.

Accordingly the invention provides a method as defined in the attached claims for forming microscale or nanoscale features with polycrystalline structures.

Thus a mechanism has been determined by which lateral grain growth can be induced and controlled in a multilayer structure having a polycrystalline layer and a second layer that serves as a constraining layer when the multilayer structure is heated. This mechanism is believed to involve the growth of grains that have been sectioned by patterning to have fewer than six grain boundaries, six grain boundaries being the most thermodynamically stable grain structure. If sufficiently heated, those grains having fewer than six boundaries and located at the patterned edge of the polycrystalline layer will undergo grain growth. If constrained, as is the case when the polycrystalline layer contacts a second layer with a lower coefficient of thermal expansion, stresses induced by the second layer will cause this grain growth to be predominantly lateral (i.e., two-dimensional and in the plane of the polycrystalline layer) and outward from the patterned edge of the polycrystalline layer.

In view of the above, a preferred embodiment of the invention generally entails forming a multilayer structure that includes a polycrystalline layer and at least one constraining layer. The multilayer structure is patterned to form first and second structures, each of which includes the polycrystalline and constraining layers. At least the first structure is then locally heated, during which time the constraining layer restricts the thermal expansion of the polycrystalline layer of the first structure. As a result, stresses are induced in the polycrystalline layer of the first structure, causing substantially two-dimensional grain growth from the edge of the first structure. Sufficient grain growth occurs to produce a third structure which is, based on an average grain size of, for example, 4 lm or less, a nanoscale structure (ie typically a structure with at least one dimension that is less than ten nanometers). When appropriately configured, nanoscale structures formed by such a method can be used as components of an electrical, mechanical, optical or fluid-handling device.

Thus as described in more detail below, a significant advantage of the approach disclosed herein is that a range of nanoscale features can be selectively formed for devices that may be employed in a wide variety of applications. An important example is the forming of nanoscale features from conventional circuit metallization such as that shown in Figure 1, in which the electrically-conductive layer 12 is a polycrystalline layer sandwiched between a pair of diffusion barrier layers 14 that serve as constraining layers. Notably, the approach disclosed herein makes use of a phenomenon that might otherwise be viewed as a flaw, as would be the case if the nanoscale feature creates an electrical short between adjacent interconnect metallizations.

Various preferred embodiments of the invention will now be described in detail by way of example only with reference to the following drawings:

Figure 1 represents a perspective view of a multilayer metallization both known in the prior art and suitable as the basis for use in the present invention;

Figures 2 and 3 represent process steps for forming a cantilever with one end stabilized by a microscale feature for use in mechanical applications;

Figures 4 and 5 represent process steps for forming nanoscale features that form a fluid restrictor for fluid-handling applications;

Figures 6 and 7 represent process steps for forming a nanoscale feature that forms an optical switch or light filter for optical applications;

Figures 8 and 9 represent process steps for forming a nanoscale fuse for electrical applications; and

Figures 10 and 11 represent process steps for forming a nanoscale on- switch for electrical applications.

In the preferred embodiment, nanoscale structures or components are formed from a multilayer structure that includes a polycrystalline layer sandwiched between a pair of constraining layers by initiating lateral grain growth. Thus, lateral grain growth has been found to occur with metallization formed by prior art metallization processes, in which the metallization is patterned to form such conventional circuit interconnects as metal lines and metal pads.

In Figures 2 and 3, the upper diffusion barrier layer 14 of the metallization 10 of Figure 1 has been omitted, allowing the grain boundaries of the polycrystalline layer 12 to be schematically represented to help illustrate the mechanism determined to be active in causing lateral (two-dimensional) grain growth, i.e., grain growth that is substantially in the plane of the polycrystalline layer 12.

Figures 2 and 3 represent the typical grain structure of an Al-Cu alloy polycrystalline layer 12 after deposition by such methods as electroplating, sputtering, evaporation, chemical or physical vapor deposition, etc. The grain structure and texture of the polycrystalline layer 12 will depend on many factors, including deposition conditions and the type of substrate and barrier materials used. In one example, the average grain size of the Al-Cu polycrystalline layer 12 may be on the order of about 0.005 to about 20 lm if deposited by electroplating, sputtering, evaporation, or chemical or physical vapor deposition. The metallization 10 is shown in Figure 2 as having been patterned by such known methods as lithography and metal reactive ion etching (RIE), by which two features 16 and 18 have been delineated by a trench 22 in the metallization 10. The trench 22 delineates opposing edges 24 and 26 of the features 16 and 18, respectively. The spacing between these edges 24 and 26 is shown as being approximately equal to the average grain size in the polycrystalline layer 12 (e.g., about 2 to 3 lm), though greater and lesser line spacing could be employed. The grains at the edges 24 and 26 of the metal pad 16 and metal lines 18 are sectioned by the trench 22 as a result of the patterning process. Figure 3 represents the effect of selectively and locally heating the feature 16, such as with a laser or electrical probe current, causing lateral grain growth of one or more grains at the edge 24 of this feature 16. In Figure 3, sufficient lateral

grain growth has occurred such that a third feature 20 has been extruded from the polycrystalline layer 12 between the barrier layers 14, projecting across the trench 22 so as to abut the second feature 18.

In accordance with the present invention, the third feature 20 is the result of stress conditions in the polycrystalline layer 12 during the localized heat treatment. In the present example, the Al-Cu polycrystalline layer 12 has a higher coefficient of thermal expansion than the titanium and/or titanium nitride barrier layers 14, but is physically constrained by the barrier layers 14. As a result of the patterning process, grains along the patterned edge 24 of the feature 16 are left with grain boundaries greater or fewer than six. As taught herein, grains with fewer than six grain boundaries are unstable and, if sufficiently heated, subject to lateral (two-dimensional) grain growth as a result of the diffusion barrier layers 14 inhibiting grain growth and thermal expansion of the polycrystalline layer 12 in the direction of the thickness of the metallization 10.

Modeling such as Mullins-Von Neumann can be used to predict the grain growth under such conditions. Based on two-dimensional grain growth modeling, when the edge 24 of the feature 16 from which the third feature 20 grows is sufficiently heated, generally to a temperature below the melting temperature of the polycrystalline layer 12 (e.g., about 200âC to about 300âC for Al-Cu alloys), those grains within the heated edge and with less than six grain boundaries will grow to effectively form a nano-scale extrusion that projects from between the diffusion barrier layers 14 into the trench 22.

In Figures 2 and 3, the feature 18 has been formed as a cantilevered structure by etching or otherwise removing the lower barrier layer 14 from between the polycrystalline layer 12 and the underlying substrate, or by selectively etching the substrate from beneath the polycrystalline layer 12. The method described herein is used to form the third feature 20 as an abutment to stabilize one end of the cantilever feature 18.

Alternative structures and components in accordance with the present invention are shown in Figures 4 through 11. In Figures 4 and 5, the metallization 10 has been patterned to form two features 30 and 32 with opposing and parallel patterned edges 34 and 36 separated by a trench 28. Figure 5 shows the result of locally heating two regions along each edge 34 and 36 to form two pairs of "extrusions" 38. The extrusions 38 are paired so that two restrictions 40 are formed within the trench 28. In

such an embodiment, after laminating a film (not shown) to the surface of the metallization 10 to enclose the trench 28, the restrictions 40 serve to restrict fluid flow through the trench 28. Figures 6 and 7 illustrate a similar embodiment, in which only a single extrusion 42 is formed to project into a trench 44 that separates a pair of features 46 and 48 patterned from the metallization 10. This embodiment is useful as an optical switch or light filter as a result of the nano-scale size of the extrusion 42.

The approach described herein is also useful for forming nano-scale electrical components for a microcircuit formed from the metallization 10. In Figure 8, a pair of features 50 and 52 are shown as being interconnected by a third feature 56 but otherwise separated by trenches 54. The trenches 54 are shown as being defined so that the features 50 and 52 have opposing and parallel edges 58 and 60, and the third feature 56 has two edges 62 that are perpendicular to the edges 58 and 60 of the features 50 and 52. The edges 58 and 60 of the features 50 and 52 are spaced apart a distance that is preferably less than or equal to the average grain size of the polycrystalline layer 12.

Figure 9 represents the result of locally heating the four regions of the third feature 56 where its two edges 62 intersect the edges 58 and 60 of the features 50 and 52. As a result of the heating process, four extrusions 64 have formed due to grain growth of those grains of the polycrystalline layer 12 located within contiguous heated portions of the edges 58, 60 and 62. The extrusions 64 provide the third feature 56 with an hourglass shape, in which the width of the third feature 56 is greater at its intersections with the first and second features 50 and 52 than at a midsection 66 between the localized heated regions. This electrical structure is useful as a fuse or an "off" switch if the features 50 and 52 are current conductors. As a fuse, the midsection 66 would overheat and create an open circuit if a sufficiently high overcurrent condition occurred in the features 50 and 52. If overheated by an appropriate overcurrent condition, the midsection 66 can be configured to expand if so desired. As an off-switch, a laser or other suitable device could be used to sever the midsection 66 under appropriate conditions.

Finally, Figures 10 and 11 illustrate another electrical application of the approach described herein. In Figure 10, a pair of features 68 and 70 are shown as being delineated from the metallization 10 by a trench 72, so that the features 68 and 70 have opposing and parallel edges 74 and 76. Figure 11 represents the result of locally heating a region of the feature

70 at or near its edge 76, by which an extrusion 78 is formed due to grain growth of those grains of the polycrystalline layer 12 that were heated. The width of the trench 72 is sufficiently narrow and the heating process is performed in such a manner as to cause the extrusion 78 to project across the trench 72 and contact the other feature 68. This electrical structure is useful as an "on" switch if the features 50 and 52 are current conductors. In use as an on-switch, a laser or other localized energy input could be used to heat the edge 76 of the feature 70 and form the extrusion 78, thereby electrically connecting the features 68 and 70 under appropriate conditions.

Thus Figures 2 through 11 have presented process steps for forming nanoscale electrical, mechanical, optical and fluid-handling structures or components from the multilayer metallization 10 shown in Figure 1, having a conductive polycrystalline layer 12 sandwiched between a pair of diffusion barrier layers 14. Those skilled in the art will appreciate that a wide variety of materials and material combinations could be employed for the polycrystalline and constraining layers of the multilayer structure, including dielectric, conductive and semiconductive materials, providing simply that the first layer has a polycrystalline grain structure, and that at least one other layer contacting the first layer has a coefficient of thermal expansion that is sufficiently lower than the first layer such that, when the multilayer structure is sufficiently heated, stresses are induced within the polycrystalline layer to initiate lateral grain growth from the polycrystalline layer. Note that while described in the context of metallizations, the teachings described herein are also applicable to other applications that might employ fine narrowly-spaced polycrystalline lines of essentially any type of material (e.g., conductive, dielectric or semiconductive).

In addition, while the invention has been described in terms of preferred embodiments, it is apparent that other forms could be adopted by one skilled in the art. For example, as is known in the art, aluminum-copper alloys are widely used for the conductive polycrystalline layer of circuit interconnect metallizations, such as BEOL interconnect metallizations, and diffusion barrier layers 14 formed of materials such as titanium, titanium nitride and combinations of both, are typically used to reduce the solid state diffusion rate between the polycrystalline layer 12 and metals from surrounding metal structures. Nevertheless, the barrier layers 14 (or any other form of constraining layer) can have an amorphous, polycrystalline or single crystal microstructure. Thus while Al-Cu alloys are preferred for the polycrystalline layer, and titanium and

titanium nitride are preferred materials for the barrier layers 14, other materials could foreseeably be used to form the metallization 10. In addition, one of the barrier layers 14 could be omitted, and additional metal layers could be encapsulated within the polycrystalline layer 12 or between the conductive and barrier layers 12 and 14. Furthermore, the thickness of the metallization 10 can vary, with thicknesses of about 0.25 lm and less being typical for certain interconnect applications. The thicknesses of the metallization 10 and its layers 12 and 14 are not particularly sensitive limitations, as long as sufficient stresses can be induced to cause the desired lateral grain growth in the polycrystalline layer 12.

CLAIMS

1. A method including the steps of:

forming a multilayer structure on a substrate, the multilayer structure comprising a polycrystalline layer and at least one constraining layer, the polycrystalline layer comprising grains having a size distribution characterized by an average grain size;

patterning the multilayer structure to form at least a first structure and a second structure, each of the first and second structures comprising the polycrystalline layer and at least one constraining layer, the first and second structures having patterned edges; and

locally heating at least the first structure to below the melting point of the polycrystalline layer, the at least one constraining layer restricting thermal expansion of the polycrystalline layer of the first structure such that stresses induced in the polycrystalline layer cause substantially two-dimensional grain growth from the patterned edge of the first structure to produce a third structure that is an operative component of an electrical, mechanical, optical or fluid-handling device.

2. The method of claim 1, wherein sufficient two-dimensional grain growth occurs during the heating step to cause the third structure to contact the second structure.

3. The method of claim 2, wherein the first and second structures are electrical conductors separated by a gap before the heating step, and the third structure forms an electrical switch therebetween.

4. The method of claim 2, wherein the second structure is formed during the patterning step to be a cantilevered structure, and the third structure abuts the cantilevered structure to substantially immobilize a portion of the cantilevered structure.

5. The method of claim 1, wherein the patterned edges of the first and second structures are substantially parallel to each other and spaced apart from each other by a gap, and wherein the third structure projects across the gap toward the patterned edge of the second structure but does not contact the second structure so as to define a restriction between the first and second structures.

6. The method of claim 5, wherein the restriction is for filtering light radiating through the gap, or for functioning as an optical switch operating in response to light radiating through the gap.

7. The method of claim 1, wherein the patterned edges of the first and second structures are substantially parallel to each other and spaced apart from each other by a gap, and wherein the third structure projects across the gap toward the patterned edge of the second structure but does not contact the second structure, a portion of the second structure also being locally heated during the heating step to cause substantially two-dimensional grain growth from the patterned edge of the second structure across the gap toward the patterned edge of the first structure, the two-dimensional grain growth from the second structure producing a fourth structure that is an operative component of said device.

8. The method of claim 7, wherein the fourth structure does not contact the first structure.

9. The method of claim 8, wherein the fourth structure is oppositely disposed from the third structure, the third and fourth structures forming a restriction between the first and second structures.

10. The method of claim 9, wherein the restriction is dimensioned for suitability for use as a fluid flow restrictor.

11. The method of claim 1, wherein the patterning step forms a fourth structure from the multilayer structure, the first structure being between and interconnecting the second and fourth structures, the fourth structure having a patterned edge separated from the patterned edge of the second structure by a gap.

12. The method of claim 11, wherein the patterned edge of the first structure is substantially perpendicular to the patterned edges of the second and fourth structures.

13. The method of claim 11 or 12, wherein the heating step causes the third structure to form at an intersection of the first and second structures and causes a fifth structure to form at an intersection of the first and fourth structures, so that the first structure is wider adjacent the second and fourth structures and is narrower at a midsection thereof.

14. The method of claim 13, wherein the second and fourth structures are electrical conductors and the first structure midsection is dimensioned so as to make the first structure suitable for use as a fuse between the second and fourth structures.

15. The method of any of claims 1 to 10, wherein the first and second structures have patterned edges substantially parallel to each other and separated by a gap so as to be spaced apart from each other, the polycrystalline layer of the first and second structures having grains with fewer than six grain boundaries at the patterned edges thereof, whereby said local heating causes the grains with fewer than six grain boundaries to undergo substantially two-dimensional grain growth from the patterned edge of the first structure across the gap toward the patterned edge of the second structure to produce said third structure.

16. The method of any of claims 11 to 14, wherein the second and fourth structures have patterned edges substantially parallel to each other, the first structure having two patterned edges that intersect the patterned edges of the second and fourth structures, the polycrystalline layer of the first structure having grains with fewer than six grain boundaries at each of the two patterned edges thereof; and wherein said heating of the first structure is performed at the intersections where the two patterned edges of the first structure intersect the patterned edges of the second and fourth structures to cause grains with fewer than six grain boundaries to undergo substantially two-dimensional grain growth from the two patterned edges of the first structure at each of said intersections, thereby increasing the width of the first structure at said intersections so that the first structure is wider where the first structure intersects the second and fourth structures as compared to a midsection of the first structure.

17. The method of any preceding claim, wherein the first and second structures are spaced apart by a gap having a width that is less than the average grain size of the polycrystalline layer.

18. The method of any preceding claim, wherein there are first and second constraining layers, said polycrystalline layer being sandwiched between the first and second constraining layers which both constrain thermal expansion of the polycrystalline layer to cause two-dimensional grain growth from the first structure.

19. The method of any preceding claim, wherein said polycrystalline material is a metal.

20. A component for use in an electrical, mechanical, optical or fluid-handling device, the component comprising:

first and second structures on a substrate, each of the first and second structures comprising a polycrystalline layer and a constraining layer that constrains thermal expansion of the polycrystalline layer, the polycrystalline layers comprising grains having a size distribution characterized by an average grain size, each of the first and second structures having patterned edges, and wherein the first and second structures are spaced apart by a gap having a width that is less than the average grain size of the polycrystalline layer; and

a nanoscale third structure comprised of substantially two-dimensional grain growth from the polycrystalline layer at the patterned edge of the first structure.

21. The component of claim 20, wherein the third structure contacts the second structure.

22. The component of claim 21, wherein the first and second structures are electrical conductors separated by the gap, and the third structure forms an electrical switch therebetween.

23. The component of claim 21, wherein the second structure is cantilevered, and the third structure abuts the cantilevered structure to substantially immobilize a portion of the cantilevered structure.

24. The component of claim 20, wherein the patterned edges of the first and second structures are substantially parallel to each other, and wherein the third structure projects across the gap toward the patterned edge of the second structure but does not contact the second structure so as to define a restriction between the first and second structures.

25. The component of claim 24, wherein the restriction is for filtering light radiating through the gap, or for functioning as an optical switch operating in response to light radiating through the gap.

26. The component of claim 20, wherein the patterned edges of the first and second structures are substantially parallel to each other, and wherein the third structure projects across the gap toward the patterned edge of the second structure but does not contact the second structure, the component further comprising a fourth structure defined by substantially two-dimensional grain growth from the patterned edge of the second structure, the fourth structure projecting across the gap toward the patterned edge of the first structure.

27. The component of claim 26, wherein the fourth structure does not contact the first structure.

28. The component of claim 27, wherein the fourth structure is oppositely disposed from the third structure, the third and fourth structures forming a restriction between the first and second structures.

29. The component of claim 28, wherein the restriction is dimensioned to be suitable for use as a fluid flow restrictor.

30. The component of claim 20, further comprising a fourth structure comprising a polycrystalline layer and a constraining layer, the first structure being between and interconnecting the second and fourth structures, the fourth structure having a patterned edge separated from the patterned edge of the second structure by a gap.

31. The component of claim 30, wherein the patterned edge of the first structure is substantially perpendicular to the patterned edges of the second and fourth structures.

32. The component of claim 30 or 31, wherein the third structure is formed at an intersection of the first and second structures, the component further comprising a fifth structure at an intersection of the first and fourth structures, so that the first structure is wider adjacent the second and fourth structures and is narrower at a midsection thereof.

33. The component of claim 32, wherein the second and fourth structures are electrical conductors and the first structure midsection is dimensioned so as to make the first structure suitable for use as a fuse between the second and fourth structures.

34. The component of any of claims 20 to 33, wherein there are first and second constraining layers, said polycrystalline layer being sandwiched between the first and second constraining layers which both serve to constrain thermal expansion of the polycrystalline layer.

35. The component of any of claims 20 to 34, wherein said polycrystalline material is a metal.