

CMOSFET WITH HYBRID STRAINED CHANNELS

ABSTRACT

Disclosed is a method of manufacturing microelectronic devices including forming a silicon substrate with first and second wells of different dopant characteristics, forming a first strained silicon-germanium-carbon layer of a first formulation proximate to the first well, and forming a second strained silicon-germanium-carbon layer of a second formulation distinct from the first formulation proximate to the second well. Capping and insulating layers, gate structures, spacers, and sources and drains are then formed, thereby creating a CMOS device with independently strained channels.

Figure 8