FIG. 1

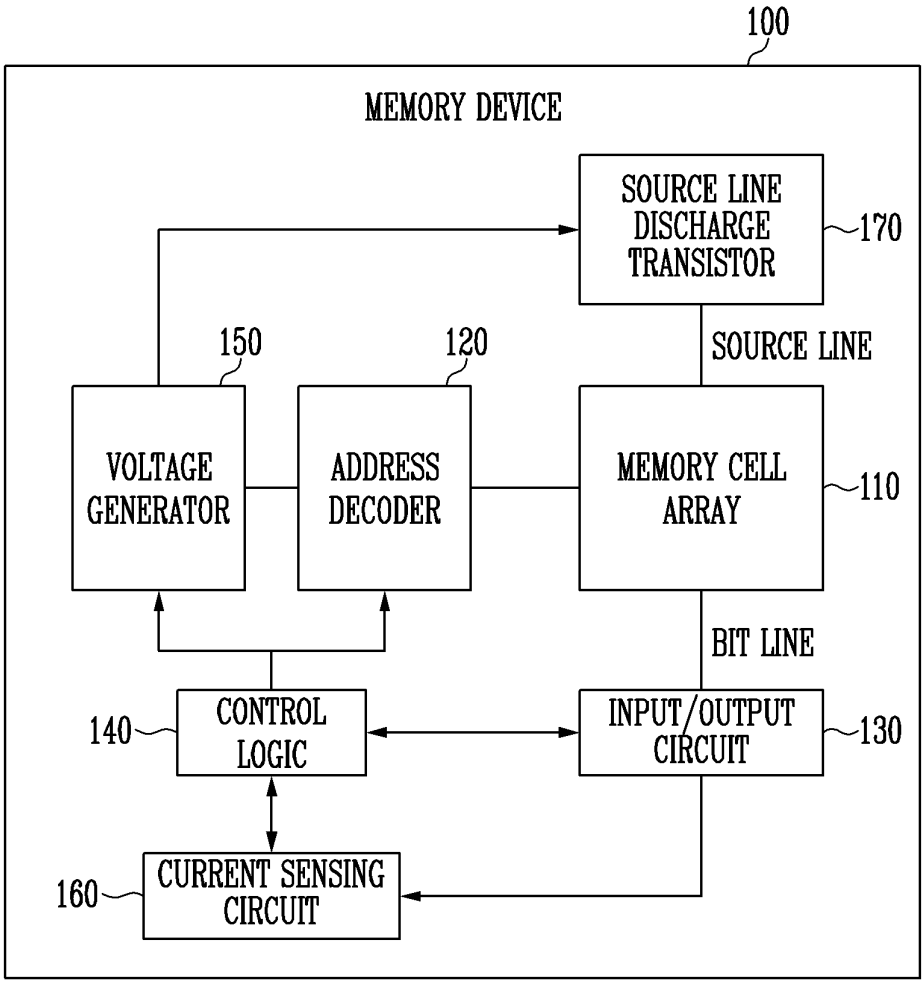

100
MEMORY DEVICE
SOURCE LINE DISCHARGE TRANSISTOR
170
SOURCE LINE
150
120
VOLTAGE GENERATOR
ADDRESS DECODER
MEMORY CELL ARRAY
110
BIT LINE
140
CONTROL LOGIC
INPUT/OUTPUT CIRCUIT
130
160
CURRENT SENSING CIRCUIT

FIG. 2

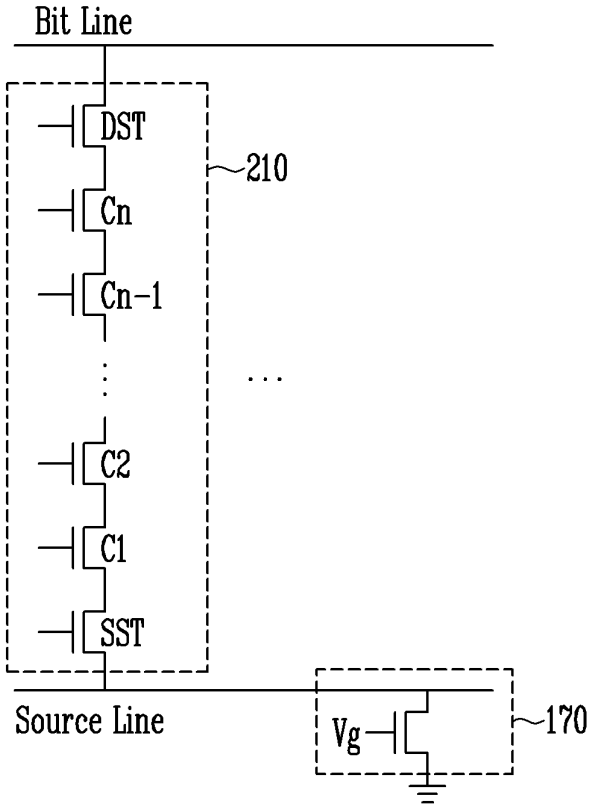


FIG. 3

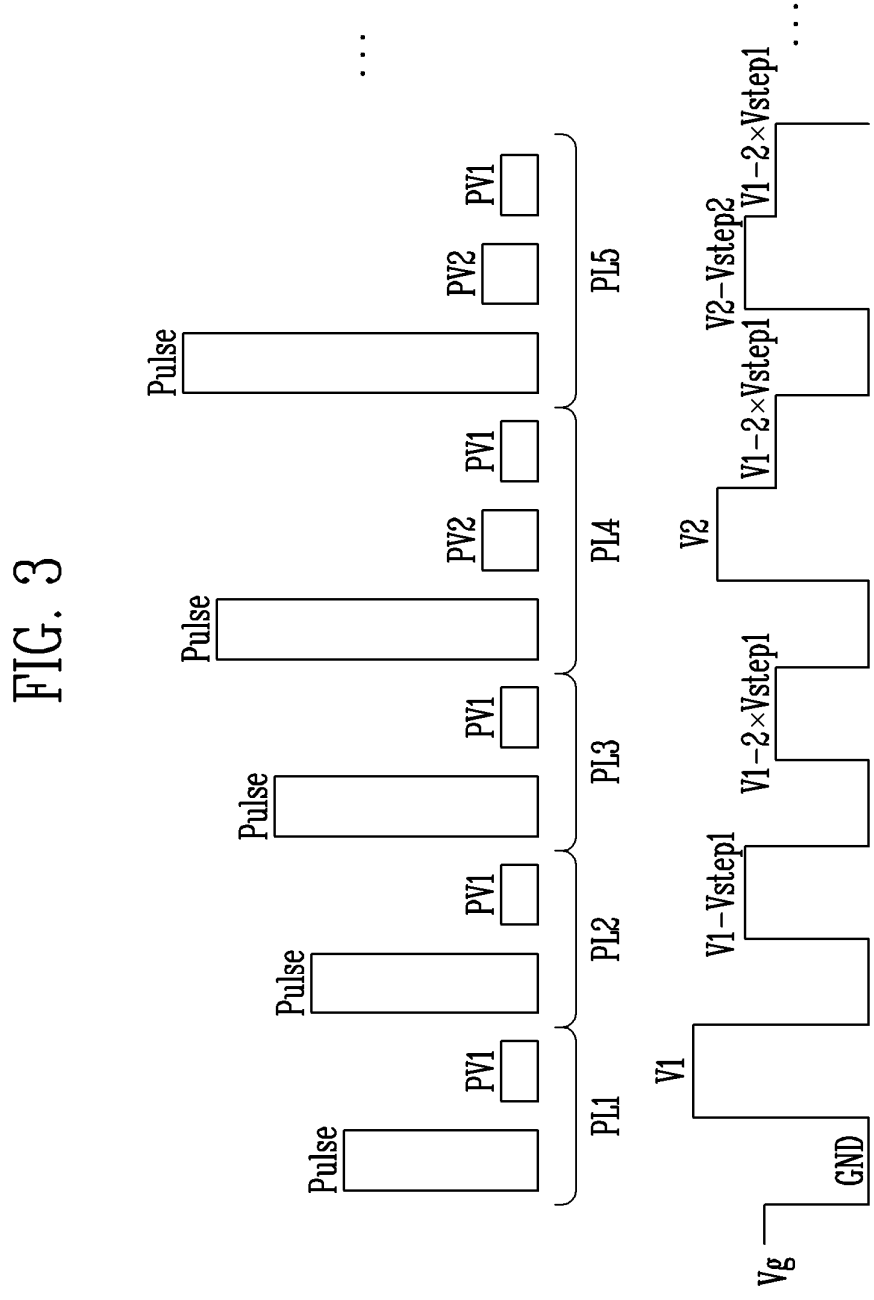

Pulse
PV1
PL1
Pulse
PV1
PL2
Pulse
PV1
PL3
Pulse
PV2
PV1
PL4
Pulse
PV2
PV1
PL5
...
Vg
GND
V1
V1-Vstep1
V1-2×Vstep1
V2
V1-2×Vstep1
V2-Vstep2
V1-2×Vstep1
...

FIG. 4

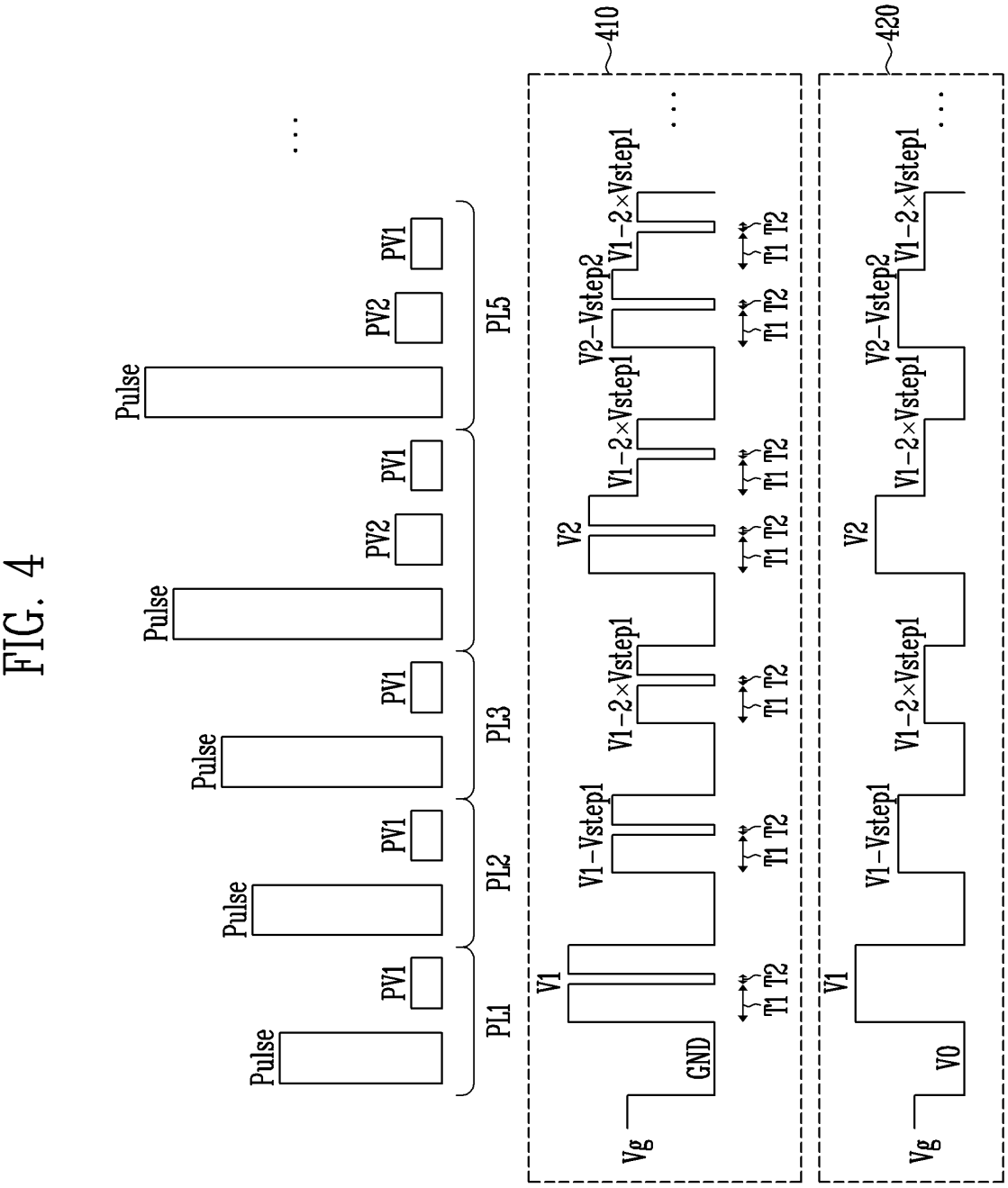

Pulse
PV1
PV2
PI1
PI2
PI3
PI5
410
420
Vg
GND
V0
V1
V2
V1-Vstep1
V1-2×Vstep1
V2-Vstep2
V1-2×Vstep2
T1
T2

FIG. 5

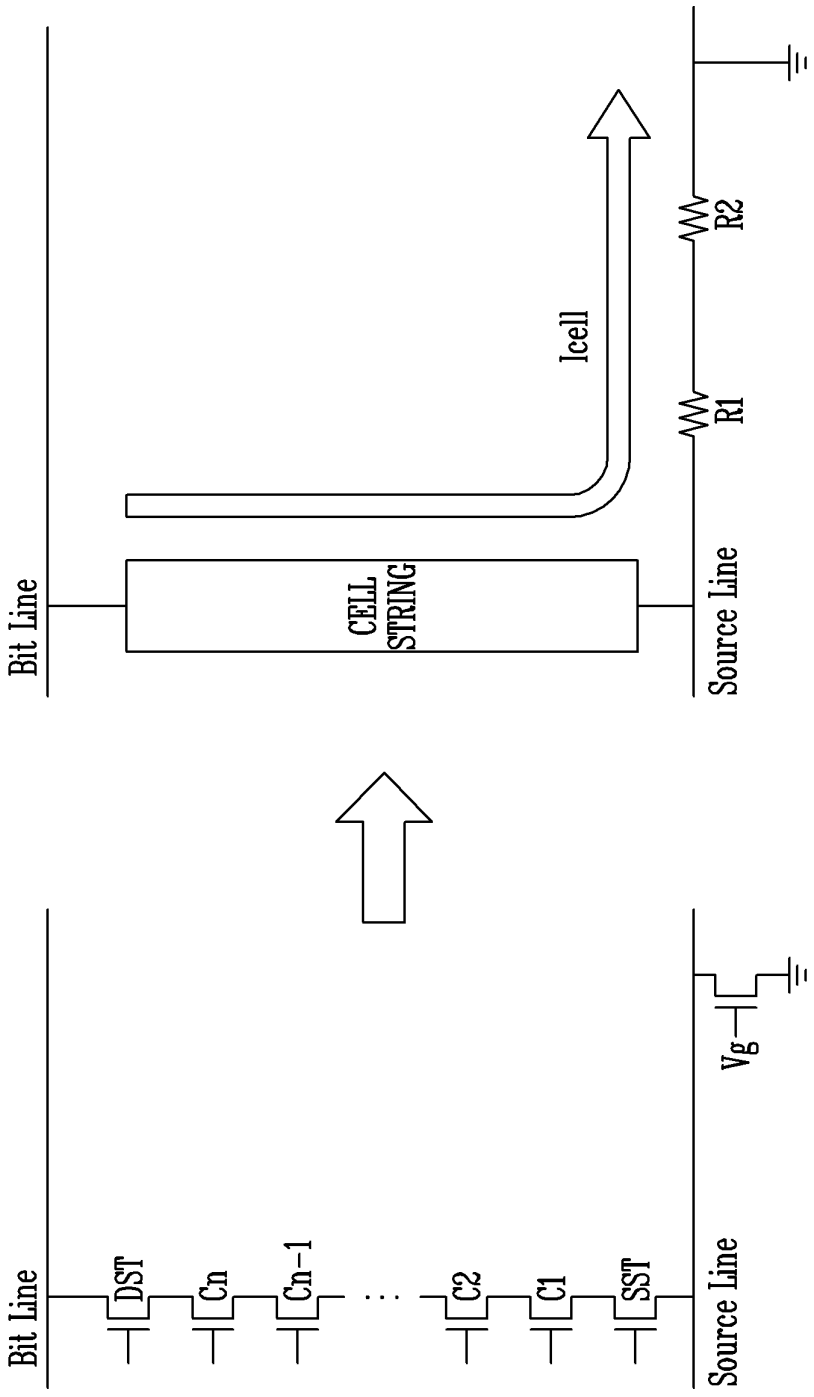

Bit Line
DST
Cn
Cn-1
C2
C1
SST
Source Line
Vg
Bit Line
CELL STRING
Source Line
Icell
R1
R2

FIG. 6

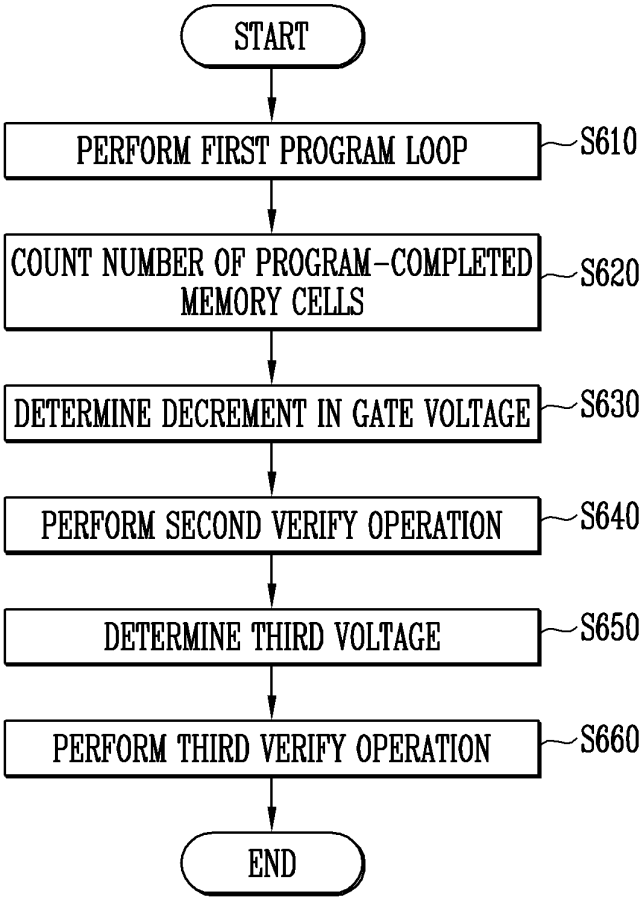
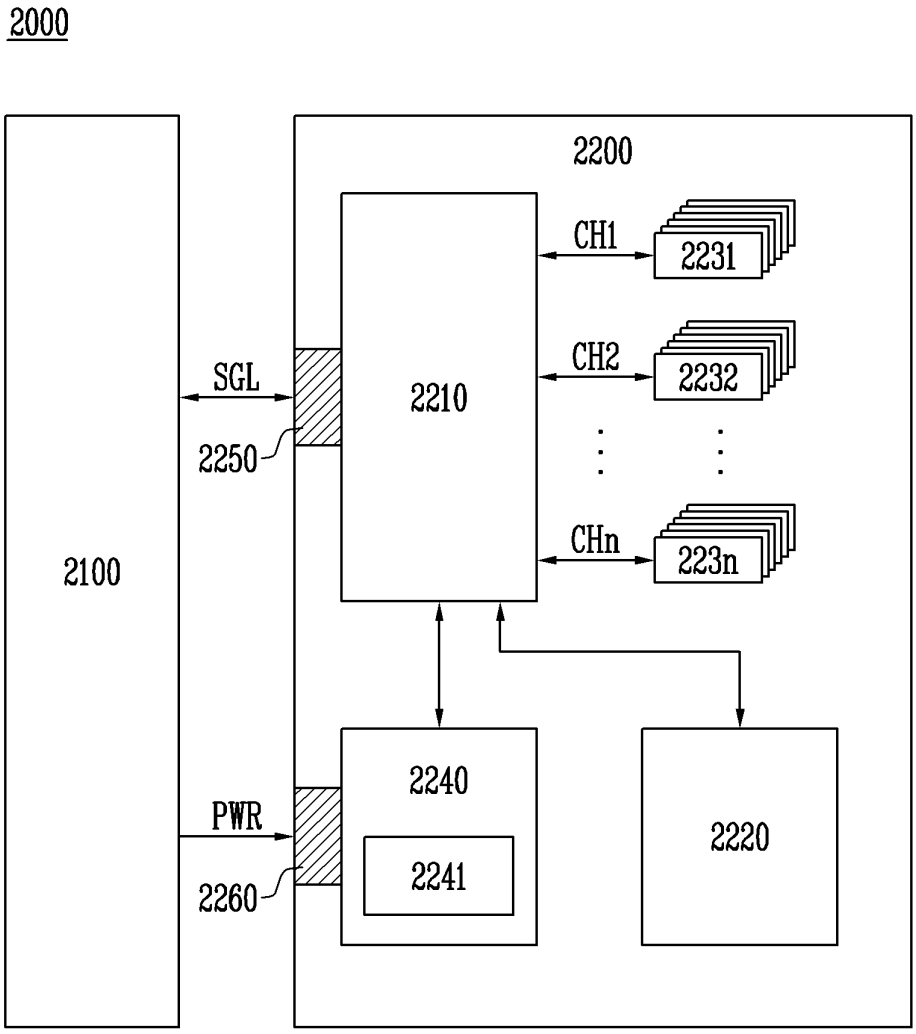

START
PERFORM FIRST PROGRAM LOOP
S610
COUNT NUMBER OF PROGRAM-COMPLETED MEMORY CELLS
S620
DETERMINE DECREMENT IN GATE VOLTAGE
S630
PERFORM SECOND VERIFY OPERATION
S640
DETERMINE THIRD VOLTAGE
S650
PERFORM THIRD VERIFY OPERATION
S660
END

FIG. 7


2000
2200
2100
2210
CH1
2231
CH2
2232
CHn
223n
SGL
2250
PWR
2260
2240
2241
2220