

FAILURE LOG DATA LOGGING CIRCUIT

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a failure log data logging circuit for logging failure log data in a failure analysis memory used for a failure analysis of devices.

Description of Related Art

A failure analysis of devices is generally carried out by using a failure analysis memory that stores failure data of devices under test by an IC tester. In the failure analysis memory used for the failure analysis of devices, failure data is logged by a failure log data logging circuit or the like. Therefore, the failure analysis memory stores address data, expectation value data, I/O data of devices under test, and so on, every test pattern.

The failure log data logging circuit according to an earlier development, logs the above-described failure data of devices under test, obtained every test pattern, in the failure analysis memory, in order.

However, the failure log data logging circuit according to an earlier development, loges the failure data of devices under test in the failure analysis memory, in order, without deciding whether it is necessary that the failure data is logged in the failure analysis memory, or not. Accordingly, in case the storage capacity of the failure analysis memory has run short, the failure analysis memory could store the necessary failure data therein.

SUMMARY OF THE INVENTION

The present invention was developed in order to solve the problems as mentioned above.

An object of the present invention is to provide a failure data logging circuit for logging not only necessary failure log data but also effective data including a number of failures counted on data not stored in a failure analysis memory, for the failure analysis of devices, in the failure analysis memory.

In accordance with an aspect of the present invention, according to a failure log data logging circuit (for example, a failure log data logging circuit 1 as shown in FIG. 1) for logging failure log data of a device under test based on a plurality of test patterns in a failure analysis

memory when a IC tester tests the device, the failure log data logging circuit comprising: a counter (for example, a counter 3 as shown in FIG. 1) for counting a number of failures of I/O (PASS/FAIL) data outputted from an output line of I/O (PASS/FAIL) data of the device under test; and a masking circuit (for example, a selection FAIL number masking circuit 4 as shown in FIG. 1) for masking I/O (PASS/FAIL) data outputted after the number of failures counted by the counter becomes equal to a predetermined value.

According to the failure log data logging circuit for logging failure log data of a device under test based on a plurality of test patterns in a failure analysis memory when a IC tester tests the device, the counter counts a number of failures of I/O (PASS/FAIL) data outputted from an output line of I/O (PASS/FAIL) data of the device under test, and the masking circuit masks I/O (PASS/FAIL) data outputted after the number of failures counted by the counter becomes equal to a predetermined value.

Consequently, because the masking circuit can mask I/O (PASS/FAIL) data after the number of failures counted by the counter becomes equal to the predetermined value, it is possible that the failure log data to be logged in the failure analysis memory is controlled.

Preferably, according to the failure log data logging circuit as described above, the masking circuit comprises a selector circuit (for example, a selector 41 as shown in FIG. 3) which can select the predetermined value voluntarily; and the failure log data logging circuit logs the failure log data of I/O (PASS/FAIL) data in the failure analysis memory, according to the predetermined value selected by the selector circuit.

Consequently, because the selector circuit can select the predetermined value voluntarily, it is possible that the failure log data logging circuit logs the effective failure log data in the failure analysis of the devices, of I/O (PASS/FAIL) data in the failure analysis memory, according to the predetermined value selected by the selector circuit.

Preferably, according to the failure log data logging circuit as described above, the counter comprises a first counting member (for example, a H-FAIL counter 31 as shown in FIG. 2) for counting a number of HIGH failures of I/O (PASS/FAIL) data and a second counting member (for example, a L-FAIL counter 32 as shown in FIG. 2) for counting a number of LOW failures of I/O (PASS/FAIL) data; and the masking circuit masks I/O (PASS/FAIL) data according as the

number of HIGH failures counted by the first counting member becomes equal to the predetermined value or the number of LOW failures counted by the second counting member becomes equal to the predetermined value, to control the failure log data to be logged in the failure analysis memory according as the failures are HIGH or LOW.

Consequently, because the first counting member of the counter counts a number of HIGH failures of I/O (PASS/FAIL) data and the second counting member of the counter counts a number of LOW failures of I/O (PASS/FAIL) data, the masking circuit can mask I/O (PASS/FAIL) data according as the number of HIGH failures counted by the first counting member becomes equal to the predetermined value or the number of LOW failures counted by the second counting member becomes equal to the predetermined value, to control the failure log data to be logged in the failure analysis memory according as the failures are HIGH or LOW.

Preferably, according to the failure log data logging circuit as described above, the counter counts a number of failures of I/O (PASS/FAIL) data of the device under test based on all test patterns.

Consequently, because the counter can count a number of failures of I/O (PASS/FAIL) data of the device under

test based on all test patterns, it is possible that the number of failures not logged in the failure analysis memory is displayed on an external display unit or the like. As a result, it is possible that the failure analysis of the device under test is voluntarily carried out in detail.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will become more fully understood from the detailed description given hereinbelow and the accompanying drawings which are given by way of illustration only, and thus are not intended as a definition of the limits of the present invention, and wherein;

FIG. 1 is a block diagram showing a circuit structure of a failure log data logging circuit 1 according to an embodiment of present invention;

FIG. 2 is a block diagram showing circuit structures of a H-FAIL/L-FAIL isolation circuit 2 and a counter 3;

FIG. 3 is a block diagram showing a circuit structure of a selection FAIL number masking circuit 4;

FIG. 4 is a timing chart showing behaviors of devices of the failure log data logging circuit 1;

FIG. 5 is a diagram showing results of I/O (PASS/FAIL) data corresponding to I/O_0 to 7 pins of devices under test based on test patterns 1 to 24;

FIG. 6 is a diagram showing failure log data stored in a failure analysis memory 9 according to the embodiment; and

FIG. 7 is a diagram showing an example of the case total failure numbers are displayed on a display unit of an external device.

PREFERRED EMBODIMENT OF THE INVENTION

Hereinafter, an embodiment of a failure log data logging circuit 1 according to the present invention will be explained with reference to FIGS. 1 to 7, in detail.

First, the structure of the failure log data logging circuit 1 will be explained, as follows.

FIG. 1 is a block diagram showing a circuit structure of the failure log data logging circuit 1 according to the embodiment of present invention.

As shown in FIG. 1, the failure log data logging circuit 1 comprises a plurality of H-FAIL/L-FAIL isolation circuits 2 for isolating each I/O data of devices under test to H-FAIL data and L-FAIL data, a plurality of counters 3, a plurality of selection FAIL number masking circuits 4, a plurality of AND gates 5, an OR gate 6, an

AND gate 7, an address pointer control circuit 8, and a failure analysis memory 9.

Each of the plurality of H-FAIL/L-FAIL isolation circuits 2 is connected to an output line of I/O (PASS/FAIL) data of a device under test and an output line of expectation value data, of an IC tester not shown in figures. Further, the H-FAIL/L-FAIL isolation circuit 2 comprises an AND gate 21 and an AND gate 22, as shown in FIG. 2.

FIG. 2 is a block diagram showing circuit structures of the H-FAIL/L-FAIL isolation circuit 2 and the counter 3 as described later.

The AND gate 21 operates a logical multiply of the I/O (PASS/FAIL) data of the device under test, by the expectation value data corresponding to the I/O (PASS/FAIL) data, wherein the I/O (PASS/FAIL) data and the expectation value data is outputted from the IC tester. Thereafter, the AND gate 21 outputs a result of operating the logical multiply, to a H-FAIL counter 31 of the counter 3.

The AND gate 22 operates a logical multiply of the I/O (PASS/FAIL) data of the device under test, by the data inverse to the expectation value data corresponding to the I/O (PASS/FAIL) data, wherein the I/O (PASS/FAIL) data and

the expectation data is outputted from the IC tester. Thereafter, the AND gate 22 outputs a result of operating the logical multiply, to a L-FAIL counter 32 of the counter 3.

Each of the plurality of counter 3 is connected to an output line of the H-FAIL/L-FAIL isolation circuit 2 and an output line of a clock generation circuit not shown in figures. Further, the counter 31 comprises a H-FAIL counter 31 and a L-FAIL counter 32, as shown in FIG. 2.

The H-FAIL counter 31 counts up the number of H-FAIL signals whenever receiving the H-FAIL signal as the result of the operation by the AND gate 21 of the H-FAIL/L-FAIL isolation circuit 2, in synchronism with a clock signal (CLK signal) generated by the clock generation circuit not shown in figures. Thereafter, the H-FAIL counter 31 outputs the counter value data as a result of counting the number of H-FAIL signals, to the selection FAIL number masking circuit 4.

The L-FAIL counter 32 counts up the number of L-FAIL signals whenever receiving the L-FAIL signal as the result of the operation by the AND gate 22 of the H-FAIL/L-FAIL isolation circuit 2, in synchronism with the clock signal (CLK signal) generated by the clock generation circuit not

shown in figures. Thereafter, the L-FAIL counter 32 outputs the counter value data as a result of counting the number of L-FAIL signals, to the selection FAIL number masking circuit 4.

When the counter value of each counter 3 is outputted to an external device such as a personal computer or the like through an interface not shown in figures, it is possible that the total failure number as a result of adding the number of failures of each I/O data is displayed on a display unit of the external device. Further, the counter value of each counter 3 may be displayed on a LCD, a LED or the like through a data bus or the like.

Each of the plurality of selection FAIL number masking circuits 4 is connected to the output line of the I/O (PASS/FAIL) data of the device under test of the IC tester not shown in figures, an output line of the counter 3, and an output line of a clock generation circuit not shown in figures. Further, the selection fail number mask circuit 4 comprises a selector 41, an AND gate 42, a flip-flop circuit 43, and a NOT circuit 44, as shown in FIG. 3.

FIG. 3 is a block diagram showing a circuit structure of the selection FAIL number masking circuit 4.

The selector 41 outputs an instruction signal "H" to

the AND gate 42 when the counter value outputted from each of the H-FAIL counter 31 and the L-FAIL counter 32 becomes equal to a predetermined value. On the other hand, the selector 41 outputs an instruction signal "L" to the AND gate 42 when counter value is not equal to the predetermined value. For example, in case the failure log data is logged in the failure analysis memory 9 when each I/O pin of the device under test outputs the failures in four test patterns, the predetermined value is equal to three.

Although the selector 41 is provided at each selection FAIL number masking circuit 4 according to the embodiment, one selector may be provided at the failure log data logging circuit 1. In case the failure log data logging circuit 1 comprises one selector, the selector is connected to a plurality of output lines of counters. Accordingly, the selector can output the instruction signal to each AND gate 42 of the selection FAIL number masking circuit 4, considering the counter values of the counters.

The AND gate 42 operates a logical multiply of the I/O (PASS/FAIL) data of the device under test outputted from the IC tester, by the instruction signal outputted from the selector 41. Thereafter, the AND gate 42 outputs a logical multiply signal as a result of operating the logical multiply, to the flip-flop circuit 43.

The flip-flop circuit 43 receives the logical multiply signal outputted from the AND gate 42 and an Enable signal (EN signal) that is the inverse of an output signal from the flip-flop circuit 43. Then, the flip-flop circuit 43 holds the logical multiply signal received from the AND gate 42, therein. Thereafter, the flip-flop circuit 43 outputs the logical multiply signal to the NOT circuit 44 in synchronism with the CLK signal. Because the flip-flop circuit 43 further has a R terminal as a reset signal input terminal, it is possible that the flop-flop circuit 43 is reset and initialized by receiving the reset signal.

The NOT circuit 44 inverts the logical multiply signal outputted from the flip-flop circuit 43, to output the inverse signal of the logical multiply signal to the AND gate 5.

Each of the plurality of AND gates 5 is connected to the output line of the I/O (PASS/FAIL) data of the device under test of the IC tester not shown in figures, and an output line of the selection FAIL number masking circuit 4.

The AND gate 5 operates a logical multiply of the I/O (PASS/FAIL) data of the device under test outputted from the IC tester, by the inverse signal outputted from the NOT circuit 44. Thereafter, the AND gate 5 outputs a logical

multiply signal as a result of operating the logical multiply, to the OR gate 6.

The OR gate 6 is connected to a plurality of output lines of AND gates 5. The OR gate 6 operates a logical addition of a plurality of logical multiply signals outputted from the plurality of AND gate 5. Thereafter, the OR gate 6 outputs a logical addition signal as a result of operating the logical addition, to the AND gate 7.

The AND gate 7 is connected to an output line of the OR gate 6 and an output line of a clock generation circuit not shown in figures. The AND gate 7 operates a logical multiply of the logical addition signal outputted from the OR gate 6, by the CLK signal. Thereafter, the AND gate 7 outputs a logical multiply signal as a result of operating the logical multiply, to the address pointer control circuit 8 and to a WE (Write Enable) terminal of the failure analysis memory 9.

The address pointer control circuit 8 is connected to an output line of the AND gate 7, and is a circuit for pointing an address of the failure analysis memory 9, wherein the data is logged in the storage area of the address, according to the logical multiply signal outputted from the AND gate 7. The address pointer control circuit 8

outputs an address pointer signal for pointing the address, to an ADD (Address) terminal of the failure analysis memory 9.

The failure analysis memory 9 comprises the I/O terminal, the WE terminal and the ADD terminal. The failure analysis memory 9 stores the failure log data therein.

The I/O terminal is connected to the output line of the I/O (PASS/FAIL) data the device under test, the output line of the expectation value data, the output line of the address data, and so on, of the IC tester not shown in figures. Each data is transmitted to the I/O terminal through each line, in synchronism with the CLK signal.

The WE terminal is connected to the output line of the AND gate 7. According to the logical multiply signal inputted to the WE terminal from the AND gate 7, the failure analysis memory 9 gets the condition wherein the data transmitted to the I/O terminal can be logged therein.

The ADD terminal is connected to the output line of the address pointer control circuit 8. According to the address pointer signal inputted to the ADD terminal from the address pointer control circuit 8, the failure log data

is logged in the storage area of the address pointed by the address pointer on the failure analysis memory 9. The failure log data includes the I/O (PASS/FAIL) data of the device under test, the expectation value data of the I/O data, the address data, a test pattern number and so on.

Next, the behavior of each device on the failure log data logging circuit 1 shown in FIG. 1 will be explained with reference to the timing chart shown in FIG. 4, as follows.

Hereinafter, the case two devices each of which has four I/O pins are tested by the IC tester not shown in figures, will be explained as an example. According to the devices under test, the I/O pins thereof are references to as the reference numerals 0 to 7, respectively. According to the IC tester, the output lines of I/O (PASS/FAIL) data corresponding to the I/O_1 to 7 pins of the devices under test are used to output the I/O_0 to 7 (PASS/FAIL) data, respectively.

According to the embodiment, the case will be explained as an example, that the I/O_1 to 3 (PASS/FAIL) data is always the PASS data and the I/O_0 and 4 to 7 (PASS/FAIL) data has been the FAIL data. Therefore, FIG. 4 shows the timing charts of only the I/O_0 and 4 to 7

(PASS/FAIL) data, not the I/O_1 to 3 (PASS/FAIL) data.

Further, according to the embodiment, because the expectation value data of each I/O data is fixed at the HIGH, the AND gate 22 of the H-FAIL/L-FAIL isolation circuit 2 and the L-FAIL counter 32 of the counter 3 are not used. Therefore, FIG. 4 shows the timing chart of the output data of the H-FAIL counter 31, not the output data of the L-FAIL counter 32.

According to the timing chart of FIG. 4, the S1 is the I/O_0 (PASS/FAIL) data, the S2 to S5 are the I/O_4 to 7 (PASS/FAIL) data, the S6 is the output data of the H-FAIL counter 31 for the I/O_0 data, the S7 to S10 are the output data of the H-FAIL counters 31 for the I/O_4 to 7 data, the S11 is the output data of the selection FAIL number masking circuit 4 for the I/O_0 data, the S12 to S15 are the output data of the selection FAIL number masking circuits 4 for the I/O_4 to 7 data, the S16 is the output data of the AND gate 5 for the I/O_0 data, and the S17 to S20 are the output data of the AND gates 5 for the I/O_4 to 7 data.

Further, the pulses of the CLK signal are referenced to as the reference numerals 1 to 25, respectively. Therefore, the pulses of the CLK signal will be explained as the CLK signals '1' to '25', respectively, as follows.

In FIG. 4, the FAIL signal is shown as "H" and the

PASS signal is shown as "L".

Further, in FIG. 4, the initial condition of the output data shown in each of the S1 to S10 and S16 to S20 is "L (Low)" and the initial condition of the output data shown in each of the S11 to S15 is "H (High)".

When the IC tester not shown in figures starts the IC test for devices, the test patterns 1 to 24 are transmitted to the I/O terminal of the failure analysis memory 9 shown in FIG. 1, in synchronism with the CLK signals '1' to '24' shown in FIG. 4, respectively. Further, the address data, the expectation value data of the I/O data, the I/O (PASS/FAIL) data of the device under test and so on are transmitted to the I/O terminal of the failure analysis memory 9, in synchronism with the CLK signals '1' to '24'.

First, the behavior of each device on the failure log data logging circuit 1 when the IC test is carried out on the basis of the test patterns 1 and 2, that is, when the CLK signals '1' and '2' are inputted to the failure log data logging circuit 1, will be explained, as follows.

According to the I/O_0 and 4 to 7 (PASS/FAIL) data of the device under test, because any FAIL has not generated, the S1 to S5 are the "L" signals showing the PASS. Therefore, because the H-FAIL/L-FAIL isolation circuits 2 does not output the "H" signal as the FAIL signal, each

device of the failure log data logging circuit 1 holds the initial condition. Accordingly, the test patterns 1 and 2 are not logged in the failure analysis memory 9.

Next, the behavior of each device on the failure log data logging circuit 1 when the IC test is carried out on the basis of the test patterns 3 to 6, that is, when the CLK signals '3' to '6' are inputted to the failure log data logging circuit 1, will be explained, as follows.

According to the I/O_0 and 4 to 7 (PASS/FAIL) data of the device under test, the S1 is the "H" signal and the S2 to S5 are the "L" signals. Therefore, the "H" signal of the S1 is inputted to the H-FAIL/L-FAIL isolation circuit 2 corresponding to the I/O_0 data.

According to the H-FAIL/L-FAIL isolation circuit 2, the AND gate 21 operates the logical multiply of the I/O_0 data S1 by the expectation value data, to output the "H" signal to the H-FAIL counter 31 for the I/O_0 data.

According to each counter 3, the H-FAIL counter 31 counts the "H" signal as the H-FAIL signal, and outputs the counter value to each selector 41. For example, according to the I/O_0 and 4 to 7 H-FAIL counter 31 output data as shown in the S6 to S10, the counter value of the I/O_0 data is 1 to 4, the counter value of the I/O_4 data is 0, the counter value of the I/O_5 data is 0, the counter value of the I/O_6 data is 0, and the counter value of the I/O_7

data is 0.

According to the selection FAIL number masking circuit 4 for the I/O_0 data, when the counter value as shown in the S6 (for example, 1 to 4) outputted from the H-FAIL counter 31 is equal to the predetermined value, the selector 41 for the I/O_0 data outputs the predetermined instruction signal "H" to the AND gate 42. For example, in case the failure log data is logged in the failure analysis memory 9 when each I/O pin of the device under test outputs the failures in four test patterns, the predetermined value is equal to three.

The AND gate 42 operates the logical multiply of the I/O_0 FAIL data S1 counted up at the four times, by the instruction signal "H" outputted from the selector 41. Thereafter, the AND gate 42 outputs the logical multiply signal as the result of operating the logical multiply, to the flip-flop circuit 43.

The flip-flop circuit 43 has held the initial condition until receiving the CLK signal '6' counted up at the four times, so that the selection FAIL number masking circuit 4 outputs the "H" signal as shown in the S11, of the initial condition to the AND gate 5. After receiving the CLK signal '6', the selection FAIL number masking circuit 4 keep outputting the "L" signal as shown in the S11.

When the selection FAIL number masking circuit 4 outputs "H" signal as shown in the S11, the AND gate 5 shown in FIG. 1 operates the logical multiply of the I/O_0 data S1 by the "H" signal S11 outputted from the selection FAIL number masking circuit 4, to output "H" signal as shown in the S16 to the OR gate 6.

Then, the OR gate 6 operates the logical addition of the signals S16 to S20, to output the "H" signal to the AND gate 7.

Thereafter, the AND gate 7 operates the logical multiply of the "H" signal as the logical addition signal operated by the OR gate 6 by the CLK signal, to output the "H" signal to the address pointer control circuit 8 and the WE terminal of the failure analysis memory 9.

When the "H" signal is inputted to the WE terminal from the address pointer control circuit 8, the failure analysis memory 9 get the condition wherein the data can be logged therein. Therefore, according to the failure analysis memory 9, the failure log data of the test patterns 3 to 6 inputted to the I/O terminal is logged in the storage area of the address inputted to the ADD terminal, in order.

When the selection FAIL number masking circuit 4 outputs the "L" signal as shown in the S11, the AND gate 5

shown in FIG. 1 operates the logical multiply of the I/O_0 data S1 by the "L" signal S11 outputted from the selection FAIL number masking circuit 4, to output the "L" signal as shown in the S16 to the OR gate 6.

Then, the OR gate 6 operates the logical addition of the signals S16 to S20, to output the "L" signal to the AND gate 7.

Thereafter, the AND gate 7 operates the logical multiply of the "L" signal as the logical addition signal operated by the OR gate 6 by the CLK signal, to output the "L" signal to the address pointer control circuit 8 and the WE terminal of the failure analysis memory 9.

When the "L" signal is inputted to the WE terminal from the address pointer control circuit 8, the failure analysis memory 9 does not get the condition wherein the data can be logged therein. Therefore, the failure log data is not logged in the failure analysis memory 9.

Next, the behavior of each device on the failure log data logging circuit 1 when the IC test is carried out on the basis of the test patterns 7 and 8, that is, when the CLK signals '7' and '8' are inputted to the failure log data logging circuit 1, will be explained, as follows.

According to the I/O_0 and 4 to 7 (PASS/FAIL) data of the device under test, the S1 is the "H" signal and the S2 to S5 are the "L" signals. Therefore, the "H" signal of

the S1 is inputted to the H-FAIL/L-FAIL isolation circuit 2 corresponding to the I/O_0 data.

According to the H-FAIL/L-FAIL isolation circuit 2, the AND gate 21 operates the logical multiply of the I/O_0 data S1 by the expectation value data, to output the "H" signal to the H-FAIL counter 31 for the I/O_0 data.

According to each counter 3, the H-FAIL counter 31 counts the "H" signal as the H-FAIL signal, and outputs the counter value to each selector 41. For example, according to the I/O_0 and 4 to 7 H-FAIL counter 31 output data as shown in the S6 to S10, the counter value of the I/O_0 data is 5 to 6, the counter value of the I/O_4 data is 0, the counter value of the I/O_5 data is 0, the counter value of the I/O_6 data is 0, and the counter value of the I/O_7 data is 0.

According to the selection FAIL number masking circuit 4 for the I/O_0 data, when the counter value as shown in the S6 (for example, 5 to 6) outputted from the H-FAIL counter 31 is inputted to the selector 41 for the I/O_0 data, the selector 41 outputs the predetermined instruction signal "L" to the AND gate 42.

The AND gate 42 operates the logical multiply of the I/O_0 FAIL data S1, that is, the "H" signal, by the instruction signal "L" outputted from the selector 41. Thereafter, the AND gate 42 outputs the "L" signal to the

flip-flop circuit 43.

The flip-flop circuit 43 holds the output condition when receiving the CLK signal '6', when receiving the CLK signal '7', so that the flip-flop circuit 43 outputs the "H" signal to the NOT circuit 44.

The NOT circuit 44 inverts the "H" signal outputted from the flip-flop circuit 43. Therefore, the selection FAIL number masking circuit 4 outputs the "L" signal as shown in the S11, to the AND gate 5.

Therefore, like the case the CLK signal '6' is inputted to the flip-flop circuit 43, that is, the case the selection FAIL number masking circuit 4 outputs the "L" signal as shown in the S11, the AND gate 5 operates the logical multiply of the I/O_0 data S1 by the "L" signal S11 outputted from the selection FAIL number masking circuit 4, to output the "L" signal as shown in the S16 to the OR gate 6.

Then, the OR gate 6 operates the logical addition of the signals S16 to S20, to output the "L" signal to the AND gate 7.

Thereafter, the AND gate 7 operates the logical multiply of the "L" signal as the logical addition signal operated by the OR gate 6 by the CLK signal, to output the "L" signal to the address pointer control circuit 8 and the WE terminal of the failure analysis memory 9.

When the "L" signal is inputted to the WE terminal from the address pointer control circuit 8, the failure analysis memory 9 does not get the condition wherein the data can be logged therein. Thereafter, the failure log data is not logged in the failure analysis memory 9.

Next, the behavior of each device on the failure log data logging circuit 1 when the IC test is carried out on the basis of the test pattern 9, that is, when the CLK signal '9' is inputted to the failure log data logging circuit 1, will be explained, as follows.

According to the I/O_0 and 4 to 7 (PASS/FAIL) data of the device under test, the S1, S2 and S3 are the "H" signals, and the S4 and S5 are the "L" signals. Therefore, the "H" signals of the S1, S2 and S3 are inputted to the H-FAIL/L-FAIL isolation circuits 2 corresponding to the I/O_0, 4 and 5 data, respectively.

According to each of the H-FAIL/L-FAIL isolation circuits 2 for the S1, S2 and S3, the AND gate 21 operates the logical multiply of each I/O data by the expectation value data, to output the "H" signal to the H-FAIL counter 31 for each I/O data.

According to each counter 3, the H-FAIL counter 31 counts the "H" signal as the H-FAIL signal, and outputs the counter value to each selector 41. For example, according to the I/O_0 and 4 to 7 H-FAIL counter 31 output data as

shown in the S6 to S10, the counter value of the I/O_0 data is 7, the counter value of the I/O_4 data is 1, the counter value of the I/O_5 data is 1, the counter value of the I/O_6 data is 0, and the counter value of the I/O_7 data is 0.

According to the selection FAIL number masking circuit 4 for the I/O_0 data, when the counter value as shown in the S6 (for example, 7) outputted from the H-FAIL counter 31 is inputted to the selector 41 for the I/O_0 data, the selector 41 outputs the predetermined instruction signal "L" to the AND gate 42.

The AND gate 42, the flip-flop circuit 43 and the NOT circuit 44 operate the process like the case of the CLK signal '7'. Therefore, the selection FAIL number masking circuit 4 outputs the "L" signal as shown in the S11, to the AND gate 5.

Further, according to the selection FAIL number masking circuits 4 for the I/O_4 and 5 data, when the counter values as shown in the S7 and S8 (for example, 1 and 1) outputted from the H-FAIL counters 31 are inputted to the selectors 41 for the I/O_4 and 5 data, each flip-flop circuit 43 has held the initial condition until each counter value becomes equal to or more than the predetermined value (for example, 3). Therefore, the

selection FAIL number masking circuits 4 output the "H" signals like the initial condition, as shown in the S12 and S13, from the NOT circuits 44, to the AND gates 5, respectively.

The AND gate 5 for the I/O_0 data operates the logical multiply of the I/O_0 data S1 by the "L" signal S11 outputted from the selection FAIL number masking circuit 4, to output the "L" signal as shown in the S16 to the OR gate 6. Further, the AND gate 5 for the I/O_4 data operates the logical multiply of the I/O_4 data S2 by the "H" signal S12 outputted from the selection FAIL number masking circuit 4, to output the "H" signal as shown in the S17 to the OR gate 6. Furthermore, the AND gate 5 for the I/O_5 data operates the logical multiply of the I/O_5 data S3 by the "H" signal S13 outputted from the selection FAIL number masking circuit 4, to output the "H" signal as shown in the S18 to the OR gate 6.

Then, the OR gate 6 operates the logical addition of the signals S16 to S20 from the AND gates 5, to output the "H" signal to the AND gate 7.

Thereafter, the AND gate 7 operates the logical multiply of the "H" signal as the logical addition signal operated by the OR gate 6 by the CLK signal, to output the "H" signal to the address pointer control circuit 8 and the WE terminal of the failure analysis memory 9.

When the "H" signal is inputted to the WE terminal, the failure analysis memory 9 gets the condition wherein the data can be logged therein. Therefore, according to the failure analysis memory 9, the failure log data of the test pattern 9 inputted to the I/O terminal is logged in the storage area of the address inputted to the ADD terminal, in order.

Next, the behavior of each device on the failure log data logging circuit 1 when the IC test is carried out on the basis of the test pattern 10, that is, when the CLK signal '10' is inputted to the failure log data logging circuit 1, will be explained, as follows.

According to the I/O_0 and 4 to 7 (PASS/FAIL) data of the device under test, the S1, S4 and S5 are the "H" signals, and the S2 and S3 are the "L" signals. Therefore, the "H" signals of the S1, S4 and S5 are inputted to the H-FAIL/L-FAIL isolation circuit 2 corresponding to the I/O_0, 6 and 7, respectively.

According to each of the H-FAIL/L-FAIL isolation circuits 2 for the S1, S4 and S4, the AND gate 21 operates the logical multiply of each I/O data by the expectation value data, to output the "H" signal to the H-FAIL counter 31 for each I/O data.

According to each counter 3, the H-FAIL counter 31

counts the "H" signal as the H-FAIL signal, and outputs the counter value to each selector 41. For example, according to the I/O_0 and 4 to 7 H-FAIL counter 31 output data as shown in the S6 to S10, the counter value of the I/O_0 data is 8, the counter value of the I/O_4 data is 1, the counter value of the I/O_5 data is 1, the counter value of the I/O_6 data is 1, and the counter value of the I/O_7 data is 1.

According to the selection FAIL number masking circuit 4 for the I/O_0 data, when the counter value as shown in the S6 (for example, 8) outputted from the H-FAIL counter 31 is inputted to the selector 41 for the I/O_0 data, the selector 41 outputs the predetermined instruction signal "L" to the AND gate 42.

The AND gate 42, the flip-flop circuit 43 and the NOT circuit 44 operate the process like the case of the CLK signal '7'. Therefore, the selection FAIL number masking circuit 4 outputs the "L" signal as shown in the S11, to the AND gate 5.

Further, according to the selection FAIL number masking circuits 4 for the I/O_6 and I/O_7 data, when the counter values as shown in the S9 and S10 (for example, 1 and 1) outputted from the H-FAIL counter 31 are inputted to the selector 41 for the I/O_6 and 7 data, each flip-flop

circuit 43 has held the initial condition until each counter value becomes equal to or more than the predetermined value (for example, 3). Therefore, the selection FAIL number masking circuits 4 output the "H" signals like the initial condition, as shown in the S14 and S15, from the NOT circuits 44, to the AND gates 5, respectively.

The AND gate 5 for the I/O_0 data operates the logical multiply of the I/O_0 data S1 by the "L" signal S11 outputted from the selection FAIL number masking circuit 4, to output the "L" signal as shown in the S16 to the OR gate 6. Further, the AND gate 5 for the I/O_6 data operates the logical multiply of the I/O_6 data S4 by the "H" signal S14 outputted from the selection FAIL number masking circuit 4, to output the "H" signal as shown in the S19 to the OR gate 6. Furthermore, the AND gate 5 for the I/O_7 data operates the logical multiply of the I/O_7 data S5 by the "H" signal S15 outputted from the selection FAIL number masking circuit 4, to output the "H" signal as shown in the S20 to the OR gate 6.

Then, the OR gate 6, the AND gate 7 and the address pointer control circuit 8 operate the processes like the case of the CLK signal '9'. Therefore, according to the failure analysis memory 9, the failure log data of the test

pattern 10 inputted to the I/O terminal is logged in the storage area of the address inputted to the ADD terminal from the address pointer circuit 8.

Next, the behavior of each device on the failure log data logging circuit 1 when the IC test is carried out on the basis of the test patterns 11 to 20, that is, when the CLK signals '11' to '20' are inputted to the failure log data logging circuit 1, will be explained, as follows.

According to the I/O_0 and 4 to 7 (PASS/FAIL) data of the device under test, the S1 is the "H" signal, and the S2, S3, S4 and S5 are the "L" signals. Therefore, the "H" signal of the data S1 is inputted to the H-FAIL/L-FAIL isolation circuit 2 corresponding to the I/O_0 data.

According to the H-FAIL/L-FAIL isolation circuit 2, the AND gate 21 operates the logical multiply of the I/O_0 data S1 by the expectation value data, to output the "H" signal to the H-FAIL counter 31 for the I/O_0 data.

According to each counter 3, the H-FAIL counter 31 counts the "H" signal as the H-FAIL signal, and outputs the counter value to each selector 41. For example, according to the I/O_0 and 4 to 7 H-FAIL counter 31 output data as shown in the S6 to S10, the counter value of the I/O_0 data is 9 to 18, the counter value of the I/O_4 data is 1, the counter value of the I/O_5 data is 1, the counter value of the I/O_6 data is 1, and the counter value of the I/O_7

data is 1.

According to the selection FAIL number masking circuit 4 for the I/O_0 data, when the counter value as shown in the S6 (for example, 9 to 18) outputted from the H-FAIL counter 31 is inputted to the selector 41 for the I/O_0 data, the selector 41 outputs the predetermined instruction signal "L" to the AND gate 42.

Thereafter, the AND gate 5, the OR gate 6, the AND gate 7 and the address pointer control circuit 8 operate the process like the case of the CLK signals '7' and '8'. Therefore, the failure log data of the test patterns 11 to 20 is not logged in the failure analysis memory 9.

Next, the behavior of each device on the failure log data logging circuit 1 when the IC test is carried out on the basis of the test pattern 21, that is, when the CLK signal '21' is inputted to the failure log data logging circuit 1, will be explained, as follows.

According to the I/O_0 and 4 to 7 (PASS/FAIL) data of the device under test, the S1 and S2 are the "H" signals, and the S3, S4 and S5 are the "L" signals. Therefore, "H" signals of the S1 and S2 are inputted to the H-FAIL/L-FAIL isolation circuit 2 corresponding to the I/O_0 and 4, respectively.

According to each of the H-FAIL/L-FAIL isolation circuit 2 for the S1 and S2, the AND gate 21 operates the logical multiply of each I/O data by the expectation value data, to output the "H" signal to the H-FAIL counter 31 for each I/O data.

According to each counter 3, the H-FAIL counter 31 counts the "H" signal as the H-FAIL signal, and outputs the counter value to each selector 41. For example, according to the I/O_0 and 4 to 7 H-FAIL counter 31 output data as shown in the S6 to S10, the counter value of the I/O_0 data is 19, the counter value of the I/O_4 data is 2, the counter value of the I/O_5 data is 1, the counter value of the I/O_6 data is 1, and the counter value of the I/O_7 data is 1.

According to the selection FAIL number masking circuit 4 for the I/O_0 data, when the counter value as shown in the S6 (for example, 19) outputted from the H-FAIL counter 31 is inputted to the selector 41 for the I/O_0 data, the selector 41 outputs the predetermined instruction signal "L" to the AND gate 42.

The AND gate 42, the flip-flop circuit 43 and the NOT circuit 44 operate the process like the case of the CLK signal '7'. Therefore, the selection FAIL number masking circuit 4 outputs the "L" signal as shown in the S11, to the AND gate 5.

Further, according to the selection FAIL number masking circuit 4 for the I/O_4 data, when the counter value as shown in the S7 (for example, s) outputted from the H-FAIL counter 31 is inputted to the selector 41 for the I/O_4 data, each flip-flop counter 43 has held the initial condition until the counter value becomes equal to or more than the predetermined value (for example, 3). Therefore, the selection FAIL number masking circuit 4 outputs the "H" signal like the initial condition, as shown in the S12, from the NOT circuit 44, to the AND gate 5.

The AND gate 5 for the I/O_0 data operates the logical multiply of the I/O_0 data S1 by the "L" signal S11 outputted from the selection FAIL number masking circuit 4, to output the "L" signal as shown in the S16 to the OR gate 6. Further, the AND gate 5 for the I/O_4 data operates the logical multiply of the I/O_4 data S2 by the "H" signal S12 outputted from the selection FAIL number masking circuit 4, to output the "H" signal as shown in the S17 to the OR gate 6.

Then, the OR gate 6, the AND gate 7 and the address pointer control circuit 8 operate the processes like the case of the CLK signal '9'. Therefore, according to the failure analysis memory 9, the failure log data of the test

pattern 21 inputted to the I/O terminal is logged in the storage area of the address inputted to the ADD terminal from the address pointer circuit 8.

Next, the behavior of each device on the failure log data logging circuit 1 when the IC test is carried out on the basis of the test patterns 22 to 24, that is, when the CLK signals '22' to '24' are inputted to the failure log data logging circuit 1, is like the above-described case.

According to each counter 3, the H-FAIL counter 31 counts the "H" signal as the H-FAIL signal, and outputs the counter value to each selector 41. For example, according to the I/O_0 and 4 to 7 H-FAIL counter 31 output data as shown in the S6 to S10, the counter value of the I/O_0 data is 20 to 22, the counter value of the I/O_4 data is 2, the counter value of the I/O_5 data is 2, the counter value of the I/O_6 data is 1 to 2, and the counter value of the I/O_7 data is 1 to 2.

According to the selection FAIL number masking circuit 4 for the I/O_0 data, the selector 41 outputs the predetermined instruction signal "L" to the AND gate 42. Therefore, the selection FAIL number masking circuit 4 for the I/O_0 data outputs the "L" signal as shown in the S11, to the AND gate 5.

Further, according to the selection FAIL number

masking circuits 4 for the I/O_4 to 7 data, each flip-flop circuit 43 has held the initial condition until each counter value becomes equal to or more than the predetermined value (for example, 3). Therefore, the selection FAIL number masking circuits 4 for the I/O_4 to 7 data output the "H" signals as shown in the S12 to 15, to the AND gates 5, respectively.

Then, the AND gate 5 for the I/O_0 data outputs the "L" signal as shown in the S16, to the OR gate 6, and the AND gates 5 for the I/O_4 to 7 data output the "H" signals as shown in the S17 to S20, to the OR gate 6.

Thereafter, when the "H" signals are inputted to the WE terminal in synchronism with the CLK signals '22' to '24', the failure analysis memory 9 get the condition wherein the data can be logged therein. Thereafter, according to the failure analysis memory 9, the failure log data of the test patterns 22 to 24 inputted to the I/O terminal is logged in the storage area of the address inputted to the ADD terminal, in order.

As described above, in the failure log data logging circuit 1 according to the embodiment of the present invention, when the IC tester starts the IC tests on the basis of the test patterns 1 to 24, and the FAIL data is generated as the result of the IC test, the I/O (PASS/FAIL)

data is inputted to the failure log data logging circuit 1 through the output line of the I/O (PASS/FAIL) data of the device under test, and transmitted to the H-FAIL/L-FAIL isolation circuit 2.

The H-FAIL/L-FAIL isolation circuit 2 isolates the FAIL signal of the I/O (PASS/FAIL) data to the H-FAIL signal and the L-FAIL signal. Then, H-FAIL/L-FAIL isolation circuit 2 outputs the H-FAIL signal to the H-FAIL counter 31 and the L-FAIL signal to the L-FAIL counter 32.

Each counter outputs the counter value data to each selector 41 every the CLK signals '1' to '24' in synchronism with the test patterns 1 to 24, respectively.

The selector 41 holds the initial condition until the counter value becomes equal to the predetermined value, to output the instruction signal "L". When the counter value becomes equal to the predetermined value, the selector 41 outputs the instruction signal "H". Each device of the selection FAIL number masking circuit 4 operates according to the instruction signal, to output the signal for controlling the FAIL number to the AND gate 5.

The OR gate 6 operates the logical addition of the signals outputted from the AND gates 5, respectively, to output the logical addition signal to the AND gate 7. The AND gate 7 operates the logical multiply of the logical addition signal outputted from the OR gate 6 by the CLK signal, to output the signal to the address pointer control

circuit 8 and the WE terminal of the failure analysis memory 9.

FIG. 5 is a diagram showing the results of the I/O (PASS/FAIL) data corresponding to I/O_0 to 7 pins of the devices under test based on the test patterns 1 to 24.

In FIG. 5, the "P" means the "PASS", and the "F" means the "FAIL". Further, as shown in FIG. 5, it is indicated that the FAIL signals are generated according to the I/O_0 pin of the device under test based on the test patterns 3 to 24, the I/O_4 pin of the device under test based on the test patterns 9 and 21, the I/O_5 pin of the device under test based on the test patterns 9 and 22, the I/O_6 pin of the device under test based on the test patterns 10 and 23, and the I/O_7 pin of the device under test based on the test patterns 10 and 24.

FIG. 6 is a diagram showing the failure log data stored in the failure analysis memory 9 according to the embodiment.

As shown in FIG. 6, the results of the I/O (PASS/FAIL) data corresponding to I/O_0 to 7 pins of the device under test based on ten test patterns that is the test patterns 3 to 6, 9 to 10, and 21 to 24 of the test patterns 1 to 24, are stored in the failure analysis memory 9. In comparison between the results shown in FIG. 5 and the results shown

in FIG. 6, it is impossible to be understood that the failure log data shown in FIG. 6 is limited.

FIG. 7 is a diagram showing an example of the case the counter value of the counter 3 is displayed on an external device such as a personal computer or the like, through an interface not shown in figures.

As shown in FIG. 7, the failure number of the I/O_0 (PASS/FAIL) data is 22, 0, the failure number of each of the I/O_1 to 3 (PASS/FAIL) data is 0, and the failure number of each of the I/O_4 to 7 (PASS/FAIL) data is 2.

Accordingly, because the failure log data corresponding to the number based on the predetermined value of the selector can be logged in the failure analysis memory 9, it is possible that the failure log data effective in the failure analysis of the device is logged in the failure analysis memory 9. Further, because the failure log data not logged in the failure analysis memory 9 can be displayed on a display unit of an external device, it is possible that the failure analysis of the device under test is voluntarily carried out in detail.

Although the present invention has been explained according to the above-described embodiment, it should also be understood that the present invention is not limited to

the embodiment and various changed and modifications may be made to the invention without departing from the gist thereof.

For example, although the predetermined value of the selector 41 is 3 according to the embodiment, the selector 41 may set the value voluntarily.

Further, the selection FAIL number masking circuit 4 is set every I/O (PASS/FAIL) data according to the embodiment. However, the selection FAIL number masking circuit 4 may be set every H-FAIL counter 31 and L-FAIL counter 32, so that the failure log data of H-FAIL and L-FAIL may be logged in the failure analysis memory 9, separately.

According to the present invention, some effects will be indicated, as follows.

According to the failure log data logging circuit 1, because the selection FAIL number masking circuit 4 can mask I/O (PASS/FAIL) data after the number of failures counted by the counter 3 becomes equal to the predetermined value, it is possible that the failure log data to be logged in the failure analysis memory is controlled.

Further, because the selector 41 can select the predetermined value voluntarily, it is possible that the failure log data logging circuit 1 logs the effective

failure log data in the failure analysis of the devices, of I/O (PASS/FAIL) data in the failure analysis memory 9, according to the predetermined value selected by the selector 41.

Furthermore, because the H-FAIL counter 31 counts the number of HIGH failures and the L-FAIL counter 32 counts the number of LOW failures, the selection FAIL number masking circuit 4 can mask I/O (PASS/FAIL) data according as the number of HIGH failures or the number of LOW failures, to control the failure log data to be logged in the failure analysis memory 9 according as the failures are HIGH or LOW.

Furthermore, because the counter 3 can count the number of failures of I/O (PASS/FAIL) data of the device under test based on all test patterns, it is possible that the number of failures not logged in the failure analysis memory 9 is displayed on an external display unit or the like. As a result, it is possible that the failure analysis of the device under test is voluntarily carried out in detail.

The entire disclosure of Japanese Patent Application No. Tokugan 2000-137547 filed on May 10, 2000 including specification, claims, drawings and summary are

incorporated herein by reference in its entirety.



What is claimed is:

1. A failure log data logging circuit for logging failure log data of a device under test based on a plurality of test patterns in a failure analysis memory when a IC tester tests the device, the failure log data logging circuit comprising:

a counter for counting a number of failures of I/O (PASS/FAIL) data outputted from an output line of I/O (PASS/FAIL) data of the device under test; and

a masking circuit for masking I/O (PASS/FAIL) data outputted after the number of failures counted by the counter becomes equal to a predetermined value.....

2. A failure log data logging circuit as claimed in claim 1,

wherein the masking circuit comprises a selector circuit which can select the predetermined value voluntarily; and

the failure log data logging circuit logs the failure log data of I/O (PASS/FAIL) data in the failure analysis memory, according to the predetermined value selected by the selector circuit.

3. A failure log data logging circuit as claimed in claim 1,

wherein the counter comprises a first counting member



for counting a number of HIGH failures of I/O (PASS/FAIL) data and a second counting member for counting a number of LOW failures of I/O (PASS/FAIL) data; and

the masking circuit masks I/O (PASS/FAIL) data according as the number of HIGH failures counted by the first counting member becomes equal to the predetermined value or the number of LOW failures counted by the second counting member becomes equal to the predetermined value, to control the failure log data to be logged in the failure analysis memory according as the failures are HIGH or LOW.

4. A failure log data logging circuit as claimed in claim 1, wherein the counter counts a number of failures of I/O (PASS/FAIL) data of the device under test based on all test patterns.