CLAIMS

1. An electronic device, comprising: one or more controllers configured to cause the electronic device to: receive a clock signal having a first frequency; receive, for a chip select training operation, a chip select signal having a pattern including high pulses and low pulses; perform, for a sampling window, the chip select training operation using the clock signal and the chip select signal, wherein the sampling window includes a quantity of pulses of the chip select signal; provide, via a first data in or out (DQ) pin, an output indicating a first result of the chip select training operation for the high pulses of the chip select signal; and provide, via a second DQ pin, an output indicating a second result of the chip select training operation for the low pulses of the chip select signal, wherein the output indicating the second result of the chip select training operation for the low pulses of the chip select signal is not provided to the first DQ pin and the output indicating the first result of the chip select training operation for the high pulses of the chip select signal is not provided to the second DQ pin.

2. The electronic device of claim 1, wherein the one or more controllers, to perform the chip select training operation, are configured to cause the electronic device to: alternate between reading the high pulses and the low pulses on rising edges of the clock signal.

3. The electronic device of claim 2, wherein the one or more controllers, to alternate between reading the high pulses and the low pulses, are configured to cause the electronic device to: read the high pulses on even rising edges of the clock signal; and read the low pulses on odd rising edges of the clock signal.

4. The electronic device of claim 1, wherein the one or more controllers are further configured to cause the electronic device to: determine the quantity of pulses of the chip select signal included in the sampling window.

5. The electronic device of claim 4, wherein the one or more controllers, to determine the quantity of pulses, are configured to cause the electronic device to: receive, from a host device, an indication of the quantity of pulses of the chip select signal included in the sampling window.

6. The electronic device of claim 4, wherein the one or more controllers, to determine the quantity of pulses, are configured to cause the electronic device to: determine the quantity of pulses using chip select signals associated with one or more chip select training operations performed prior to the chip select training operation.

7. The electronic device of claim 1, wherein the one or more controllers, to perform the chip select training operation, are configured to cause the electronic device to: receive an indication that the chip select training operation is enabled; sample the chip select signal for the quantity of pulses of the chip select signal; and refrain from sampling, for the chip select training operation, the chip select signal after the quantity of pulses have been sampled.

8. The electronic device of claim 1, wherein the one or more controllers, to perform the chip select training operation, are configured to cause the electronic device to: detect a failure associated with a high pulse of the chip select signal, wherein the one or more controllers, to provide the indication of the first result, are configured to cause the electronic device to: cause an indication of the failure to be persistently indicated via the first DQ pin for at least the sampling window.

9. The electronic device of claim 1, wherein the one or more controllers, to perform the chip select training operation, are configured to cause the electronic device to: detect a failure associated with a low pulse of the chip select signal, wherein the one or more controllers, to provide the indication of the second result, are configured to cause the electronic device to: cause an indication of the failure to be persistently indicated via the second DQ pin for at least the sampling window.

10. The electronic device of claim 1, wherein the one or more controllers are further configured to cause the electronic device to: reduce, prior to performing the chip select training operation, the first frequency of the clock signal to a second frequency; and receive, in association with reducing the first frequency, an indication that the chip select training operation is enabled.

11. The electronic device of claim 1, wherein the one or more controllers are further configured to cause the electronic device to: reduce, after performing the chip select training operation, the first frequency of the clock signal to a second frequency; and receive, in association with reducing the first frequency, an indication that the chip select training operation is disabled.

12. A method performed by an electronic device, comprising: receiving a clock signal having a first frequency; receiving, for a chip select training operation, a chip select signal having a pattern including high pulses and low pulses; performing, for a sampling window, the chip select training operation using the clock signal and the chip select signal, wherein the sampling window includes a quantity of pulses of the chip select signal; providing, only via a first data in or out (DQ) pin, an output indicating a first result of the chip select training operation for the high pulses of the chip select signal; and providing, only via a second DQ pin, an output indicating a second result of the chip select training operation for the low pulses of the chip select signal, wherein the output indicating the second result of the chip select training operation for the low pulses of the chip select signal is not provided to

the first DQ pin and the output indicating the first result of the chip select training operation for the high pulses of the chip select signal is not provided to the second DQ pin.

13. The method of claim 12, wherein performing the chip select training operation comprises: alternating between reading the high pulses and the low pulses on rising edges of the clock signal.

14. The method of claim 13, wherein alternating between reading the high pulses and the low pulses comprises: reading the high pulses on even rising edges of the clock signal; and reading the low pulses on odd rising edges of the clock signal.

15. The method of claim 12, further comprising: determining the quantity of pulses of the chip select signal included in the sampling window.

16. The method of claim 15, wherein determining the quantity of pulses comprises: receiving, from a host device, an indication of the quantity of pulses of the chip select signal included in the sampling window.

17. The method of claim 15, wherein determining the quantity of pulses comprises: determining the quantity of pulses using chip select signals associated with one or more chip select training operations performed prior to the chip select training operation.

18. The method of claim 12, wherein performing the chip select training operation comprises: receiving an indication that the chip select training operation is enabled; sampling the chip select signal for the quantity of pulses of the chip select signal; and refraining from sampling, for the chip select training operation, the chip select signal after the quantity of pulses have been sampled.

19. The method of claim 12, wherein performing the chip select training operation comprises: detecting a failure associated with a high pulse of the chip select signal, wherein providing the indication of the first result comprises: causing an indication of the failure to be persistently indicated via the first DQ pin for at least the sampling window.

20. The method of claim 12, wherein performing the chip select training operation comprises: detecting a failure associated with a low pulse of the chip select signal, wherein providing the indication of the second result comprises: causing an indication of the failure to be persistently indicated via the second DQ pin for at least the sampling window.

21. The method of claim 12, further comprising: reducing, prior to performing the chip select training operation, the first frequency of the clock signal to a second frequency; and receiving, in association with reducing the first frequency, an indication that the chip select training operation is enabled.

22. The method of claim 12, further comprising: reducing, after performing the chip select training operation, the first frequency of the clock signal to a second frequency; and receiving, in association with reducing the first frequency, an indication that the chip select training operation is disabled.

23. A system comprising: one or more controllers configured to: receive a clock signal having a first frequency; receive, for a chip select training operation, a chip select signal having a pattern including high pulses and low pulses; perform, for a sampling window, the chip select training operation using the clock signal and the chip select signal, wherein the sampling window includes a quantity of pulses of the chip select signal; provide, via a first data in or out (DQ) pin, an output indicating a first result of the chip select training operation for the high pulses of the chip select signal; and provide, via a second DQ pin, an output indicating a second result of the chip select training operation for the low pulses of the chip select signal, wherein the output indicating the second result of the chip select training operation for the low pulses of the chip select signal is not provided to the first DQ pin and the output indicating the first result of the chip select training operation for the high pulses of the chip select signal is not provided to the second DQ pin.

24. The system of claim 23, wherein the one or more controllers, to perform the chip select training operation, are configured to: alternate between reading the high pulses and the low pulses on rising edges of the clock signal.

25. The system of claim 23, wherein the one or more controllers are further configured to: receive, from a host device, an indication of the quantity of pulses of the chip select signal included in the sampling window.

26. The system of claim 23, wherein the one or more controllers, to perform the chip select training operation, are configured to: receive an indication that the chip select training operation is enabled; sample the chip select signal for the quantity of pulses of the chip select signal; and refrain from sampling, for the chip select training operation, the chip select signal after the quantity of pulses have been sampled.

27. The system of claim 23, wherein the one or more controllers, to perform the chip select training operation, are configured to: detect a failure associated with a high pulse of the chip select signal, wherein the one or more controllers, to provide the indication of the first result, are configured to:

cause an indication of the failure to be persistently indicated via the first DQ pin for at least the sampling window.

28. An apparatus, comprising: means for receiving a clock signal having a first frequency; means for receiving, for a chip select training operation, a chip select signal having a pattern including high pulses and low pulses; means for performing, for a sampling window, the chip select training operation using the clock signal and the chip select signal, wherein the sampling window includes a quantity of pulses of the chip select signal; means for providing, via a first data in or out (DQ) pin, an output indicating a first result of the chip select training operation for the high pulses of the chip select signal; and means for providing, via a second DQ pin, an output indicating a second result of the chip select training operation for the low pulses of the chip select signal, wherein the output indicating the second result of the chip select training operation for the low pulses of the chip select signal is not provided to the first DQ pin and the output indicating the first result of the chip select training operation for the high pulses of the chip select signal is not provided to the second DQ pin.

29. The apparatus of claim 28, further comprising: means for determining the quantity of pulses of the chip select signal included in the sampling window.

30. The apparatus of claim 28, further comprising: means for reducing, prior to performing the chip select training operation, the first frequency of the clock signal to a second frequency; and means for receiving, in association with reducing the first frequency, an indication that the chip select training operation is enabled.