

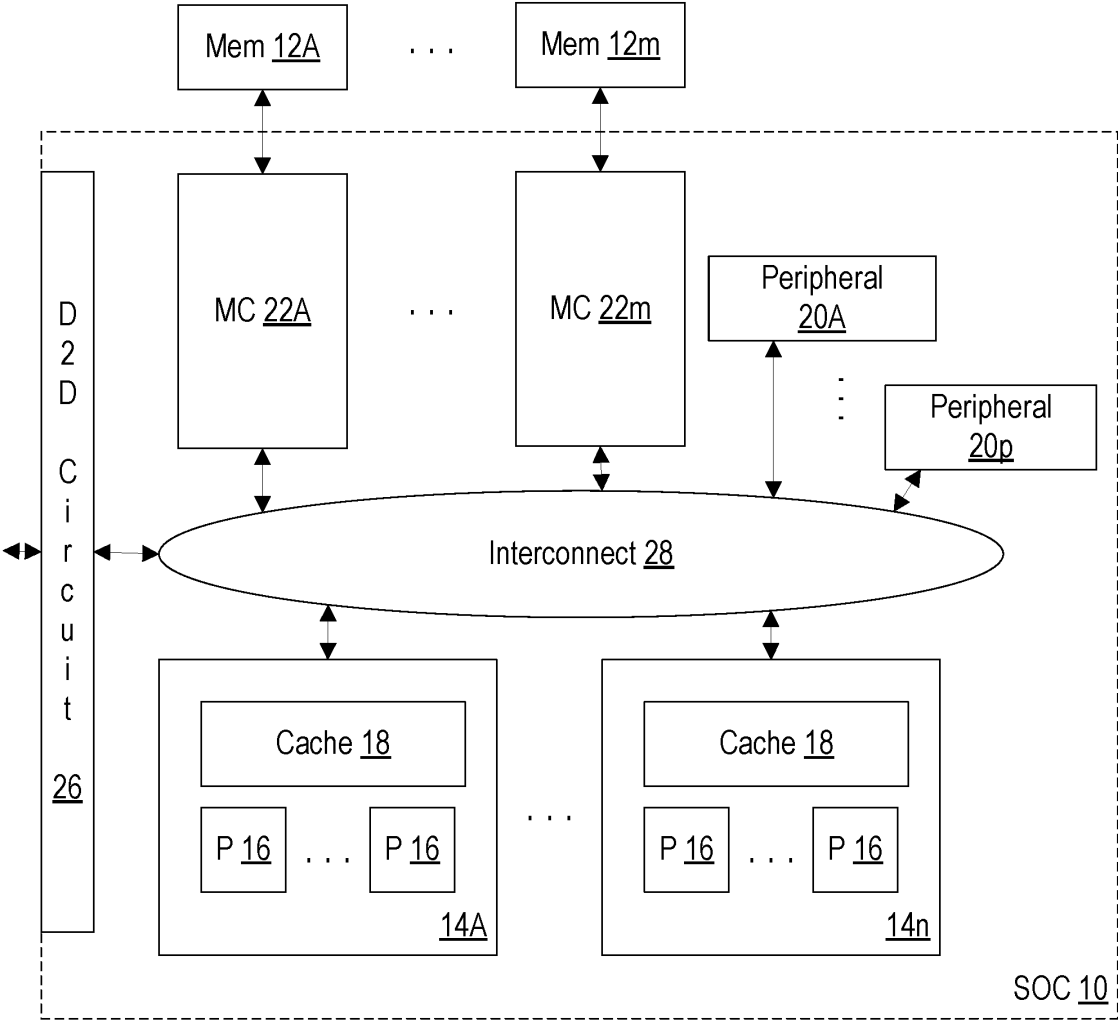


FIG. 1

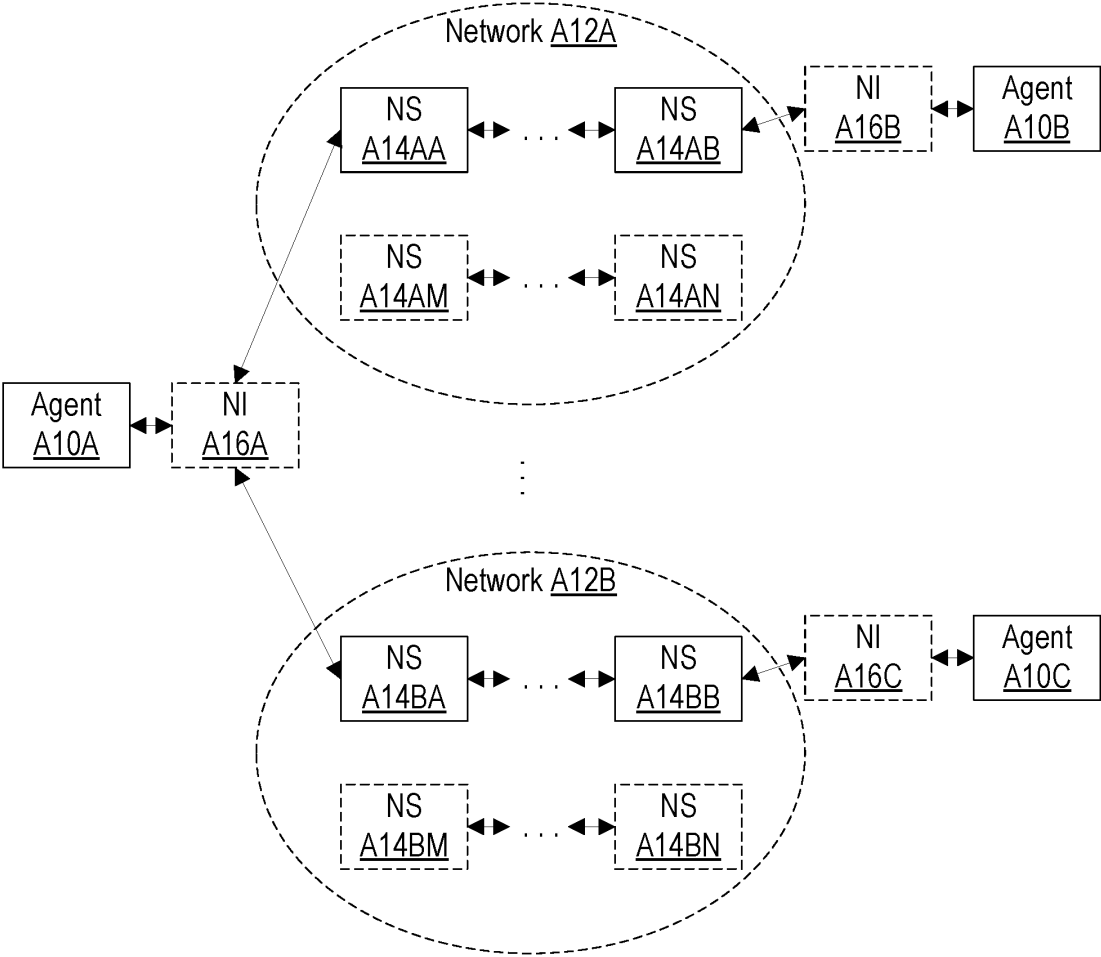


FIG. 2

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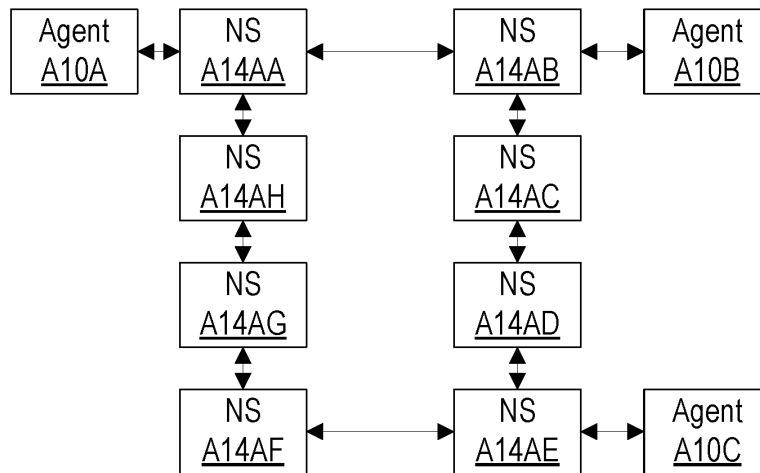


FIG. 3

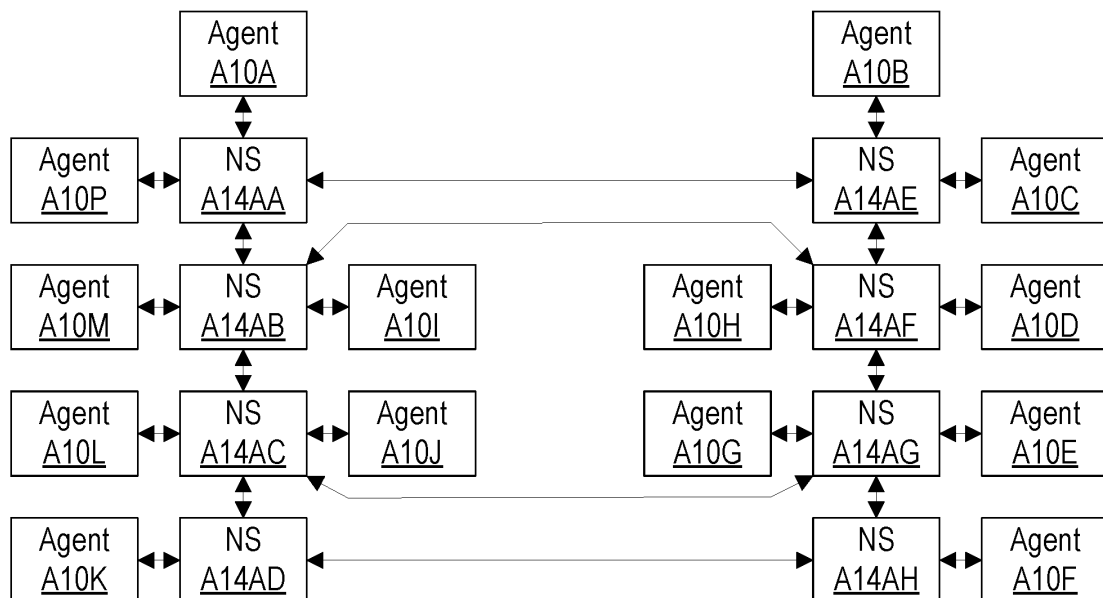


FIG. 4

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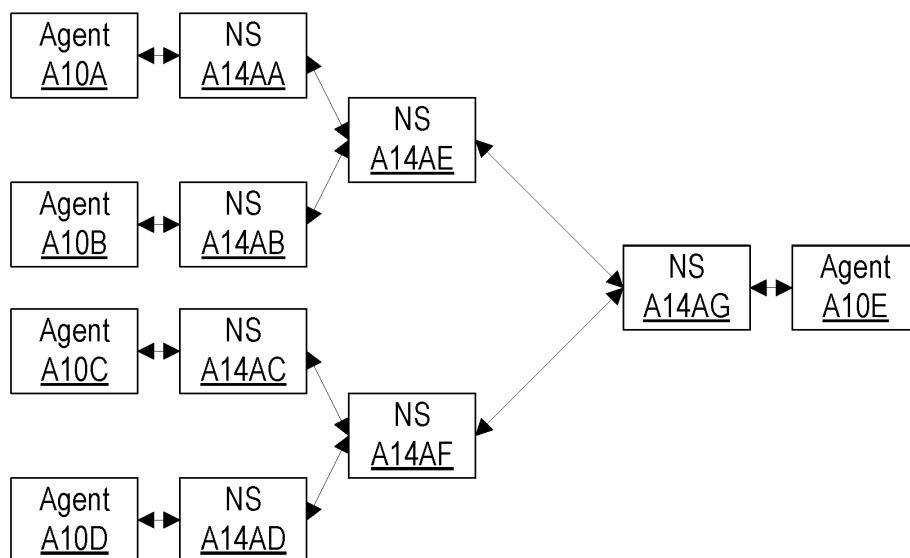


FIG. 5

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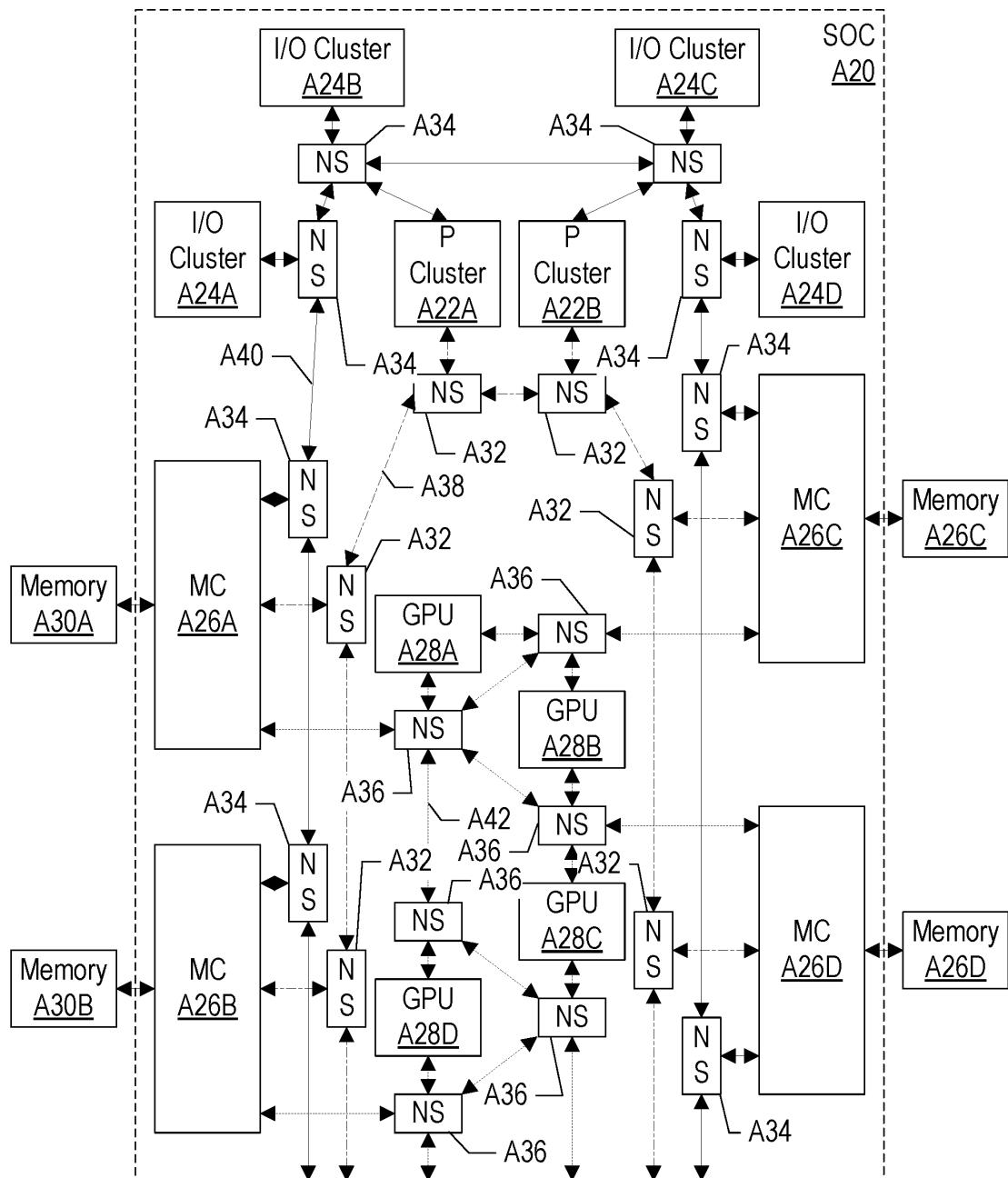


FIG. 6

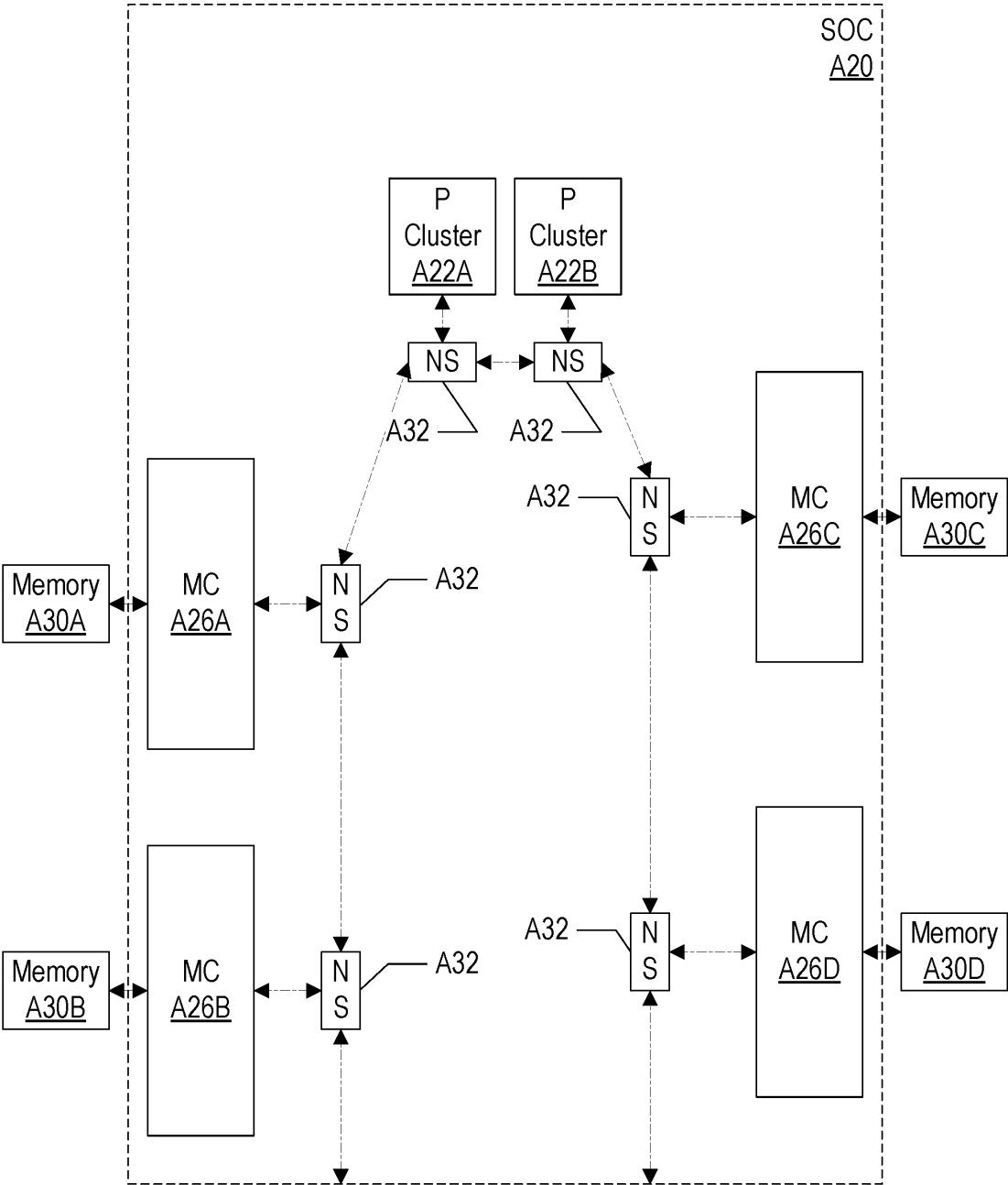


FIG. 7

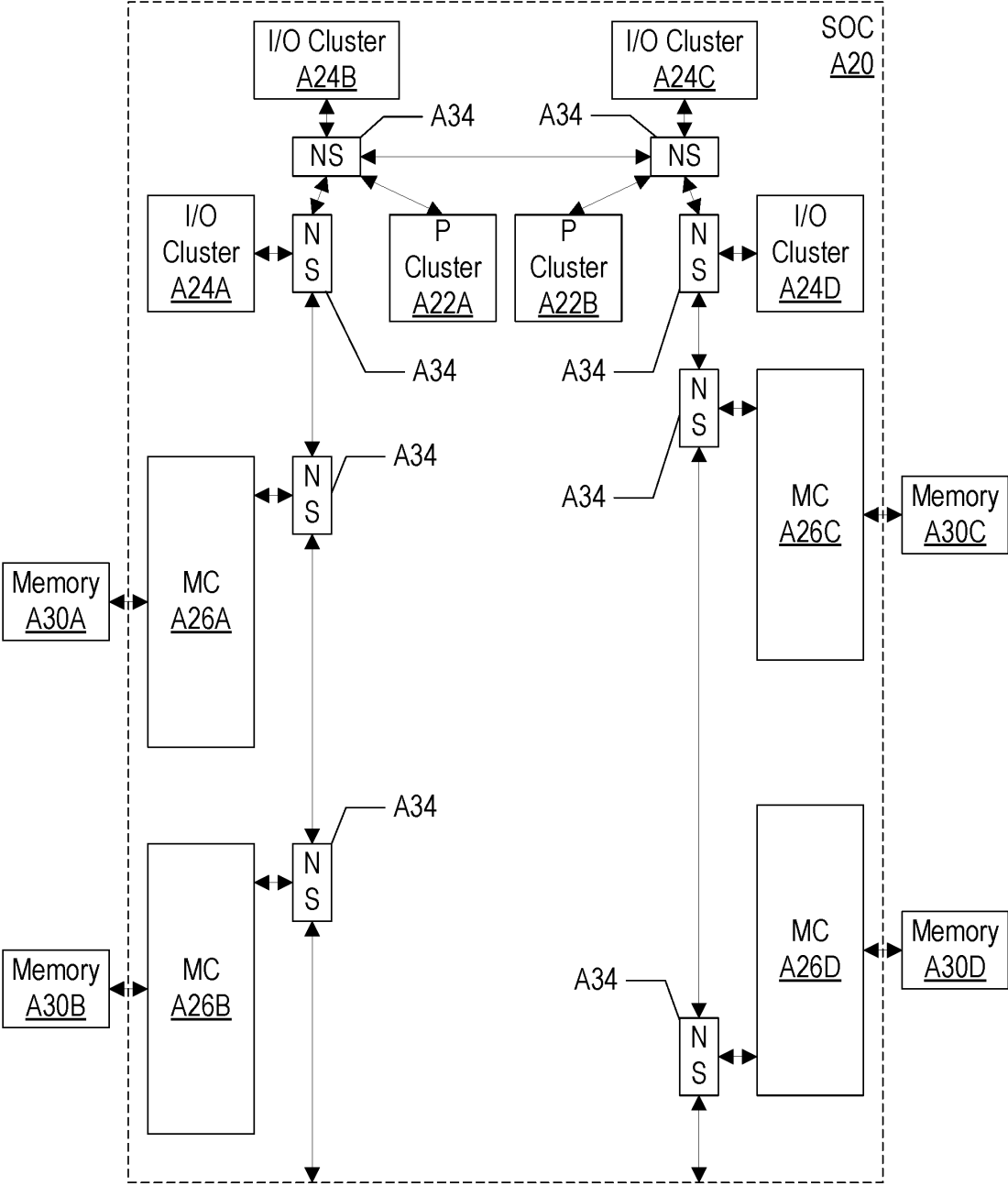


FIG. 8

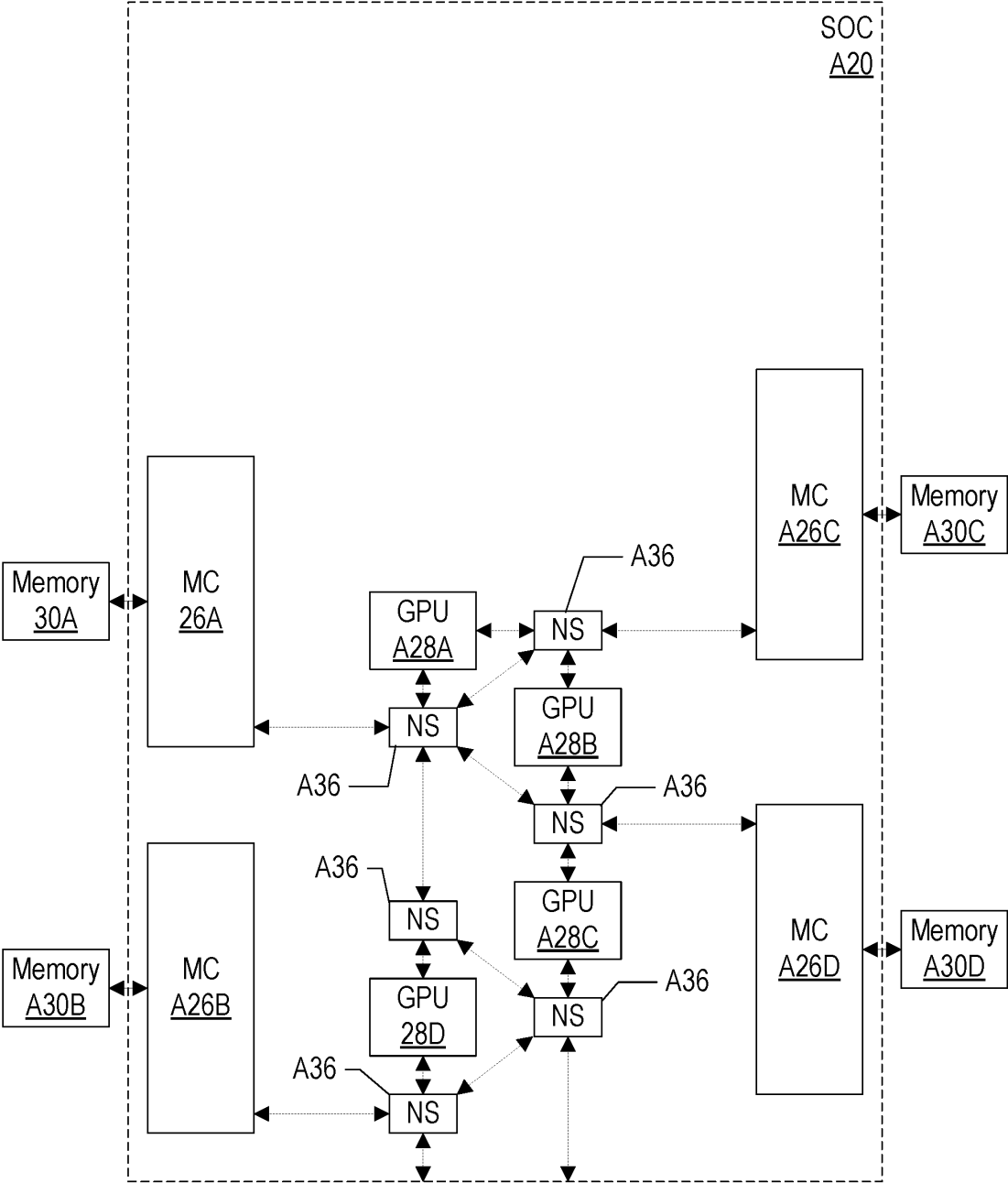


FIG. 9

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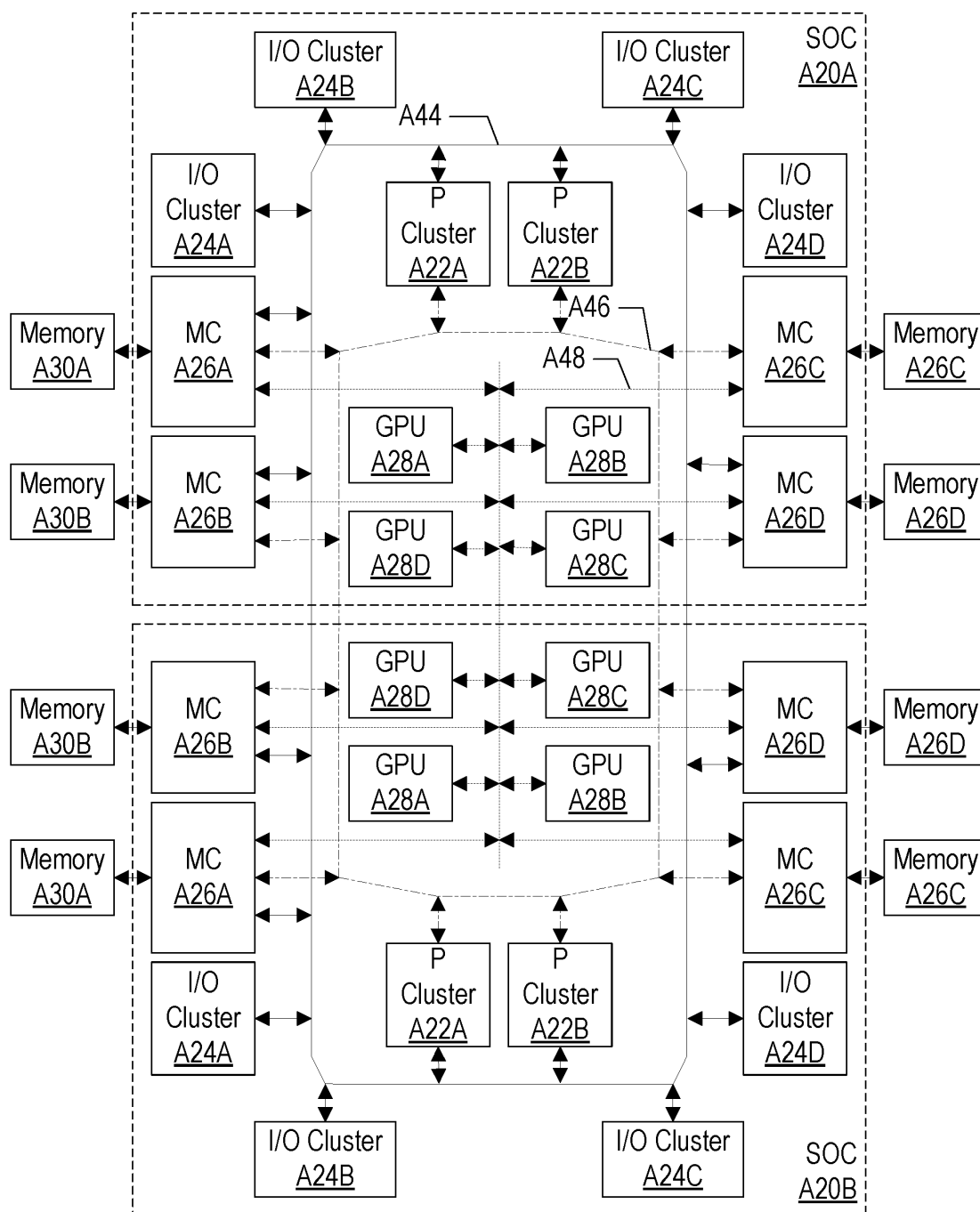


FIG. 10

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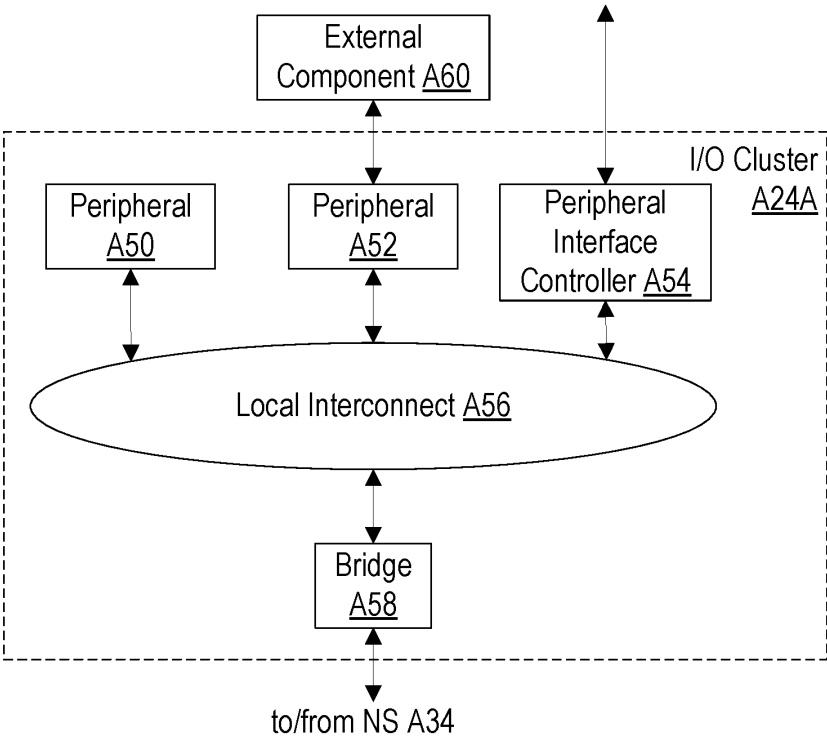


FIG. 11

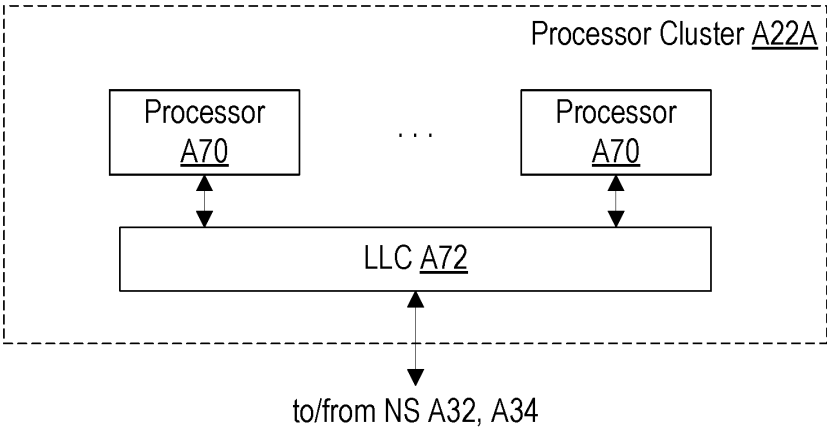


FIG. 12

<u>Virtual Channel</u>	<u>Networks</u>	<u>Type</u>	<u>Networks</u>
Bulk	CPU, I/O, Relaxed	Coherent	CPU, I/O
LLT	CPU, I/O, Relaxed	Non-coherent	Relaxed
RT	I/O	RT	I/O
VCP	I/O	VCP	I/O

A80

A82

FIG. 13

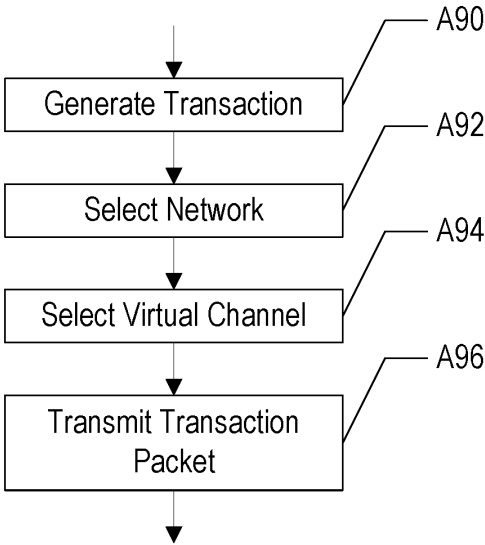


FIG. 14

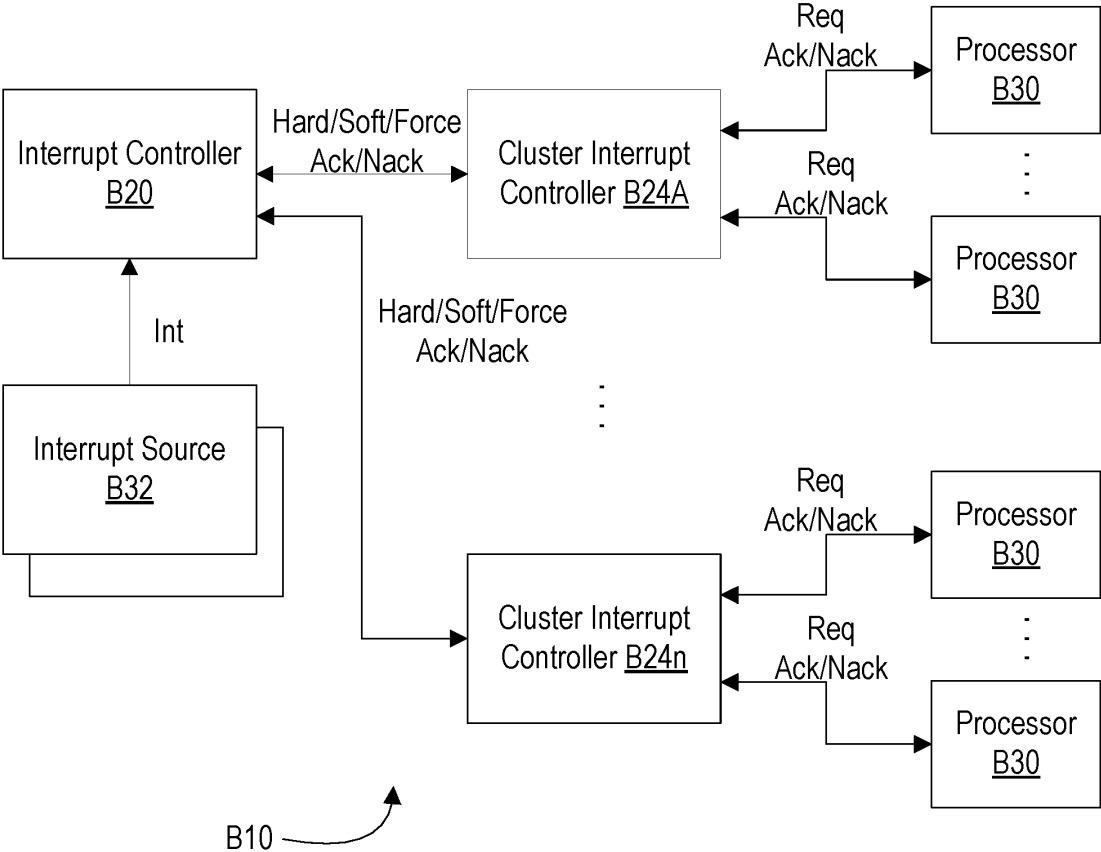


FIG. 15

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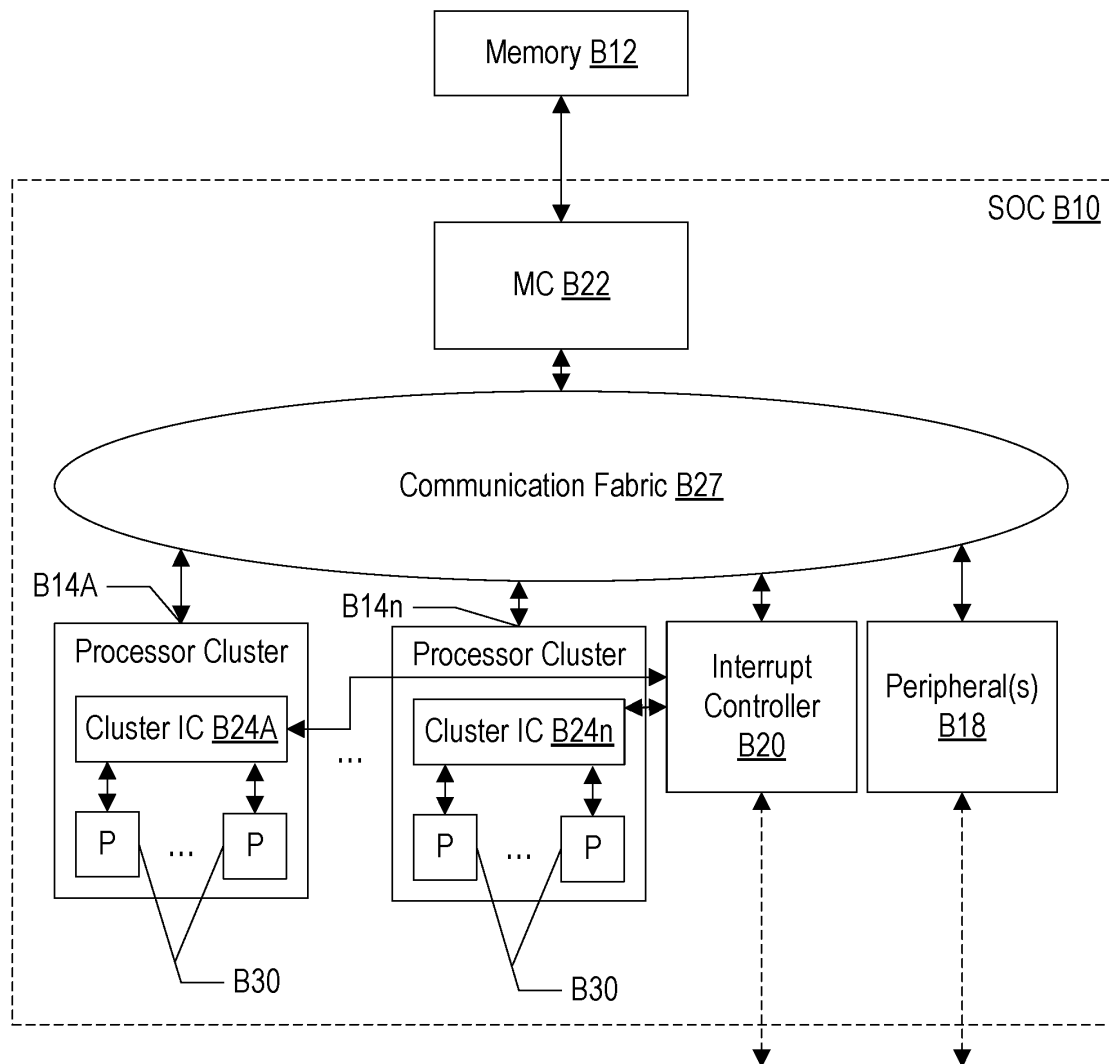


FIG. 16

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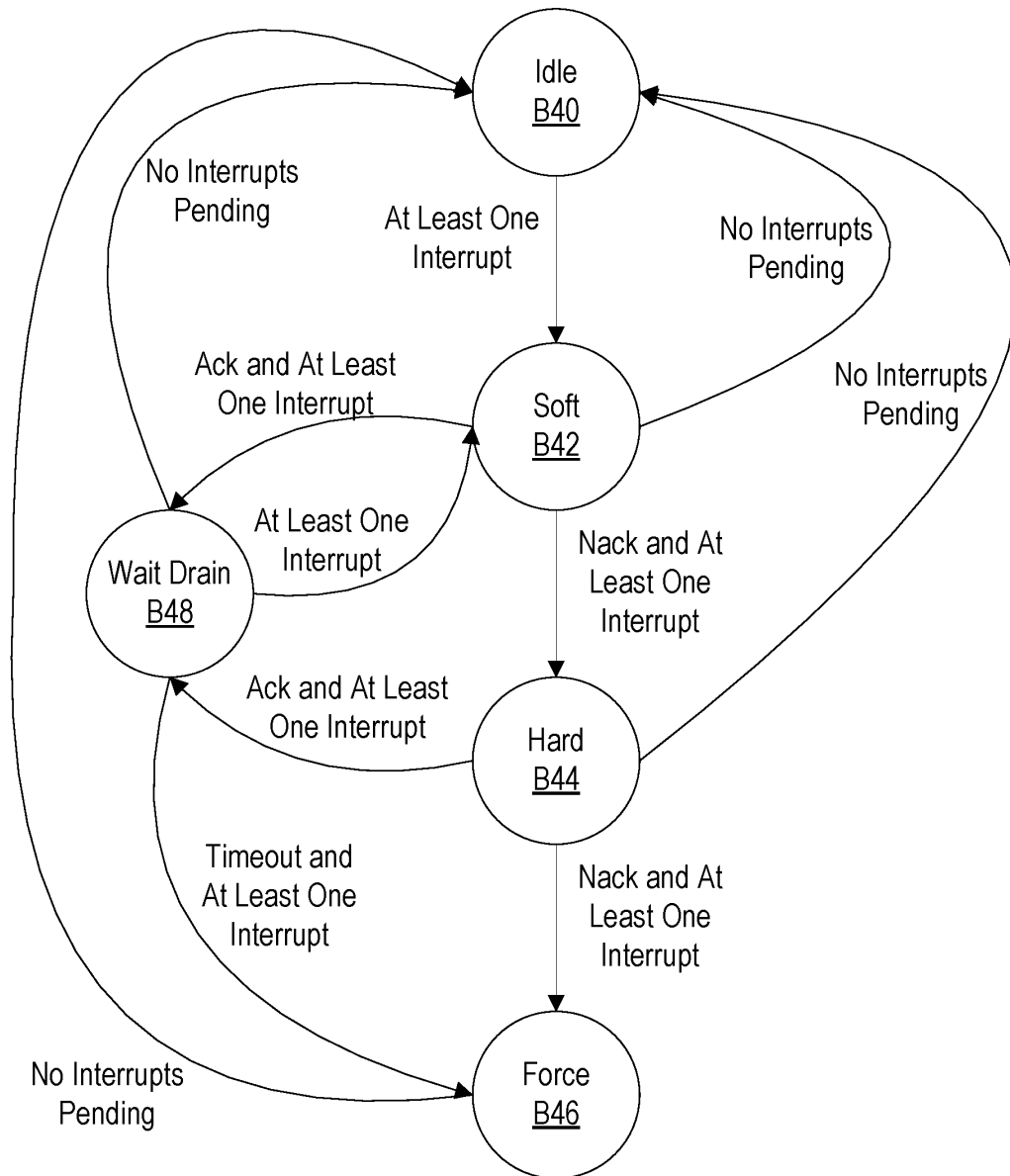


FIG. 17

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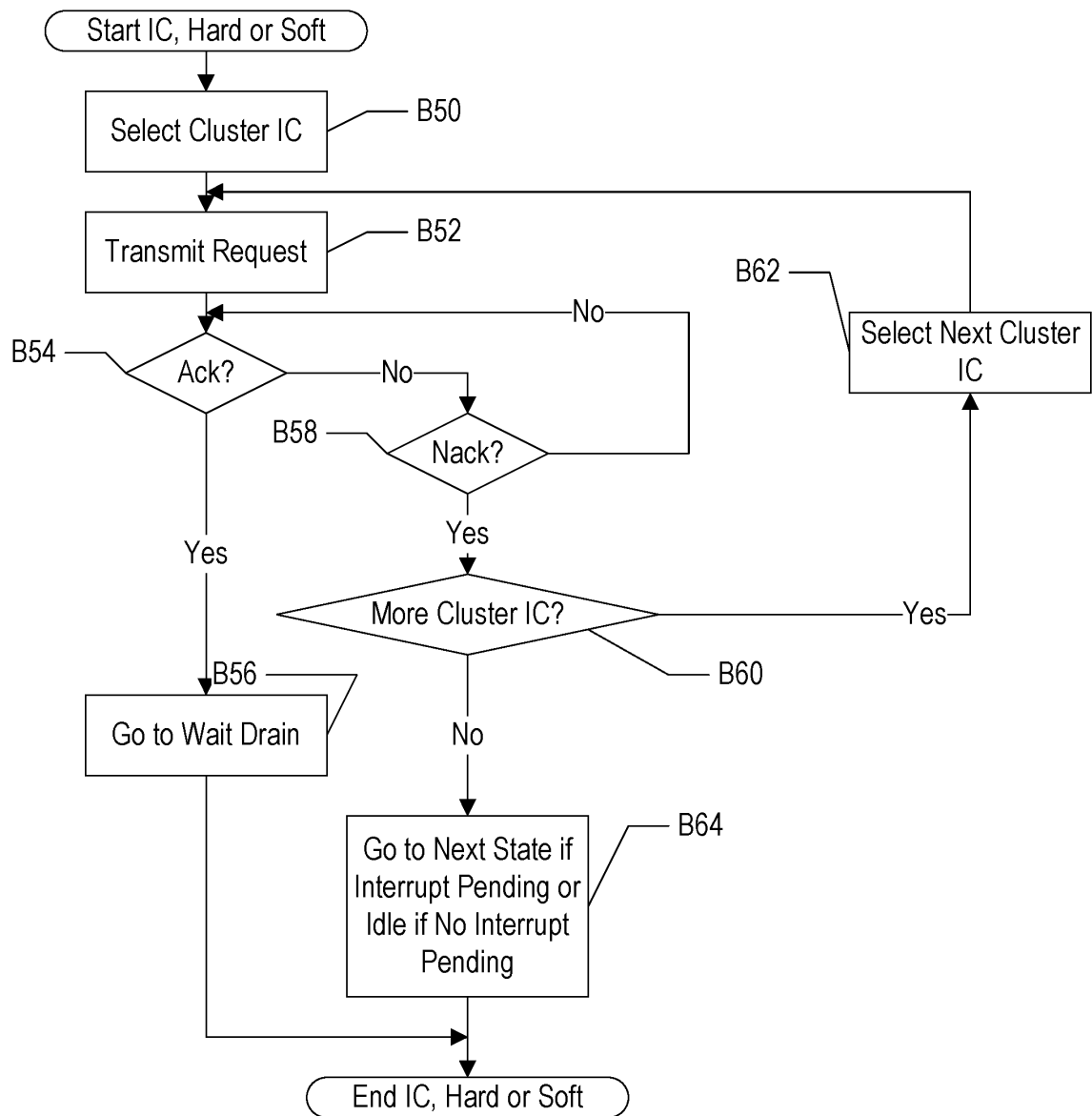


FIG. 18

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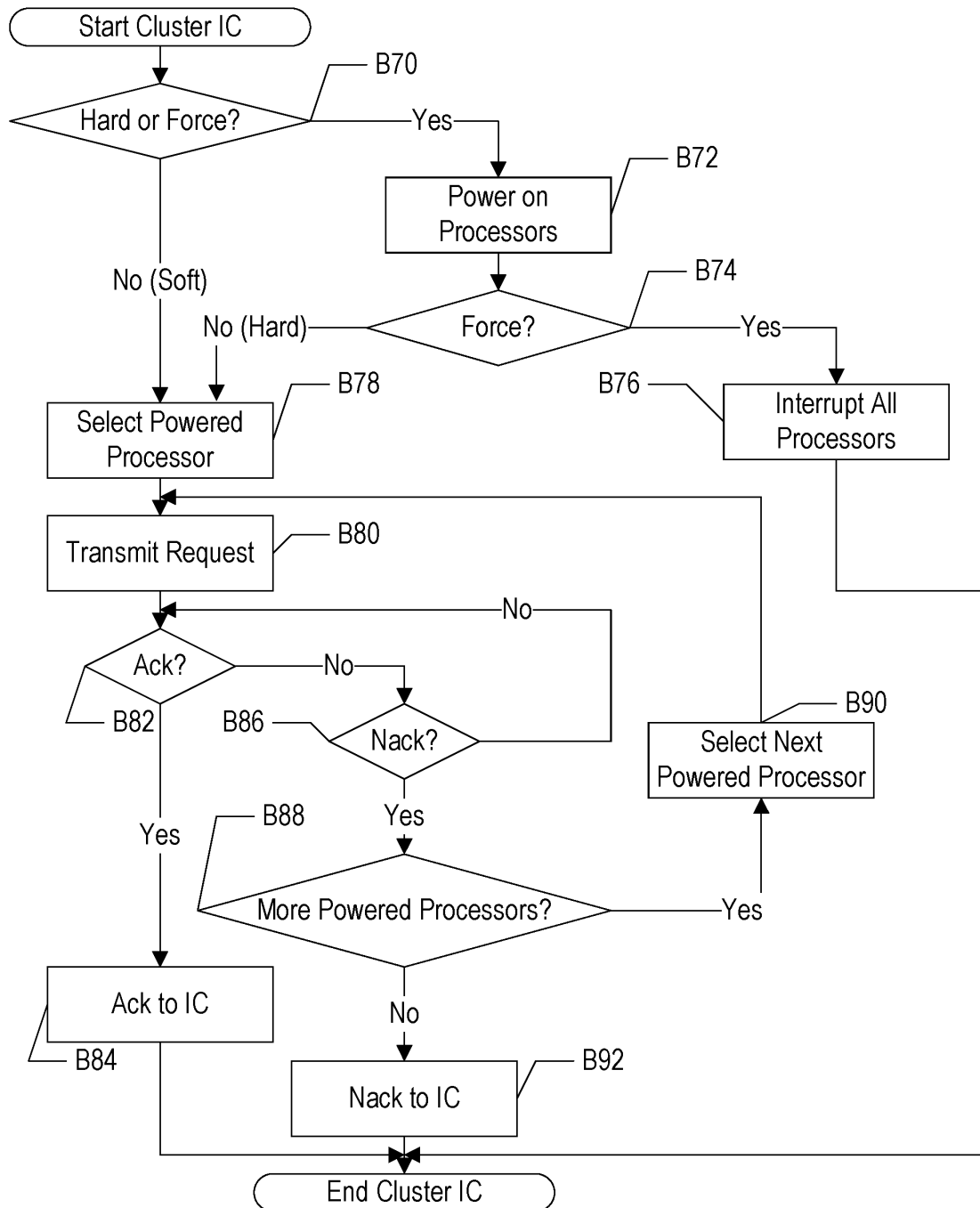


FIG. 19

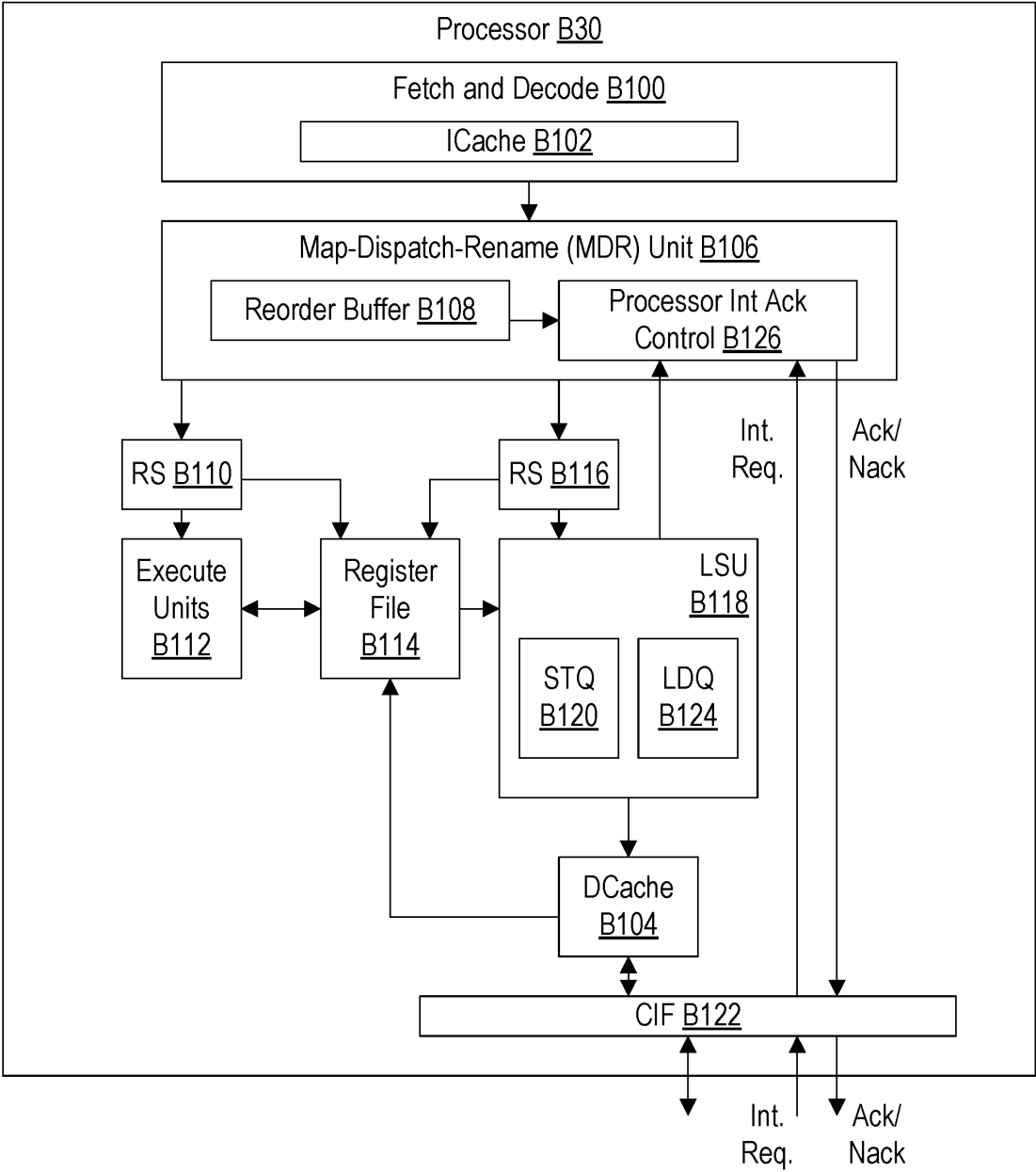


FIG. 20

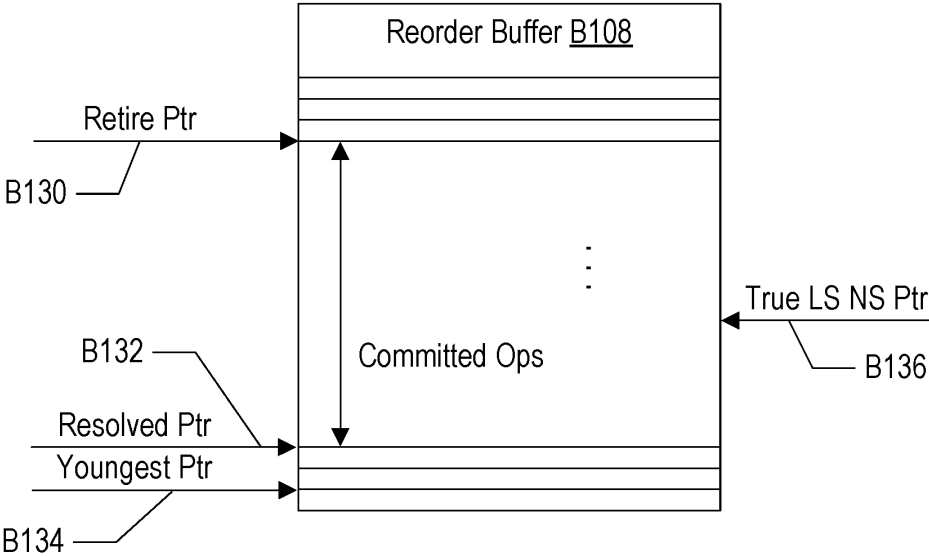


FIG. 21

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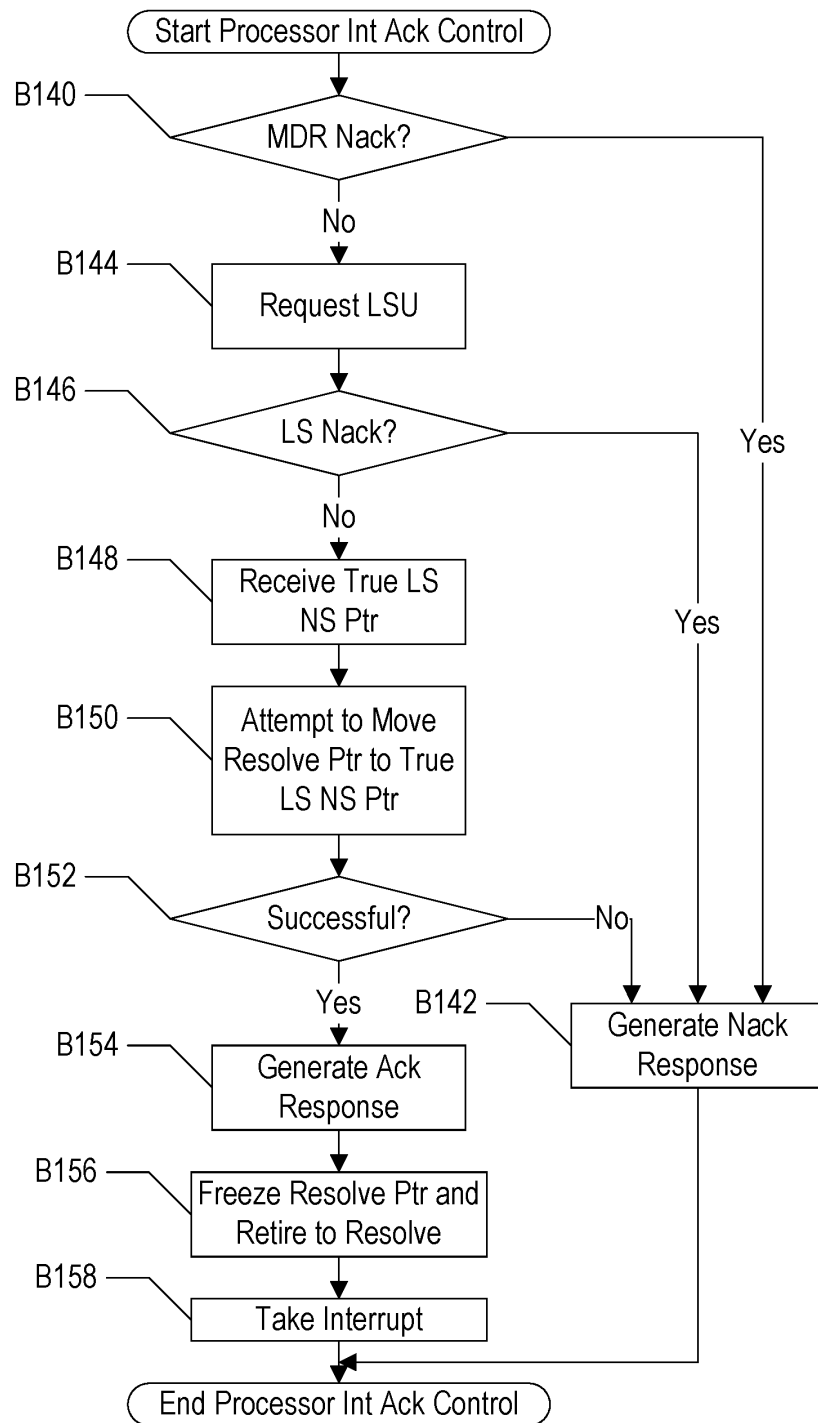


FIG. 22

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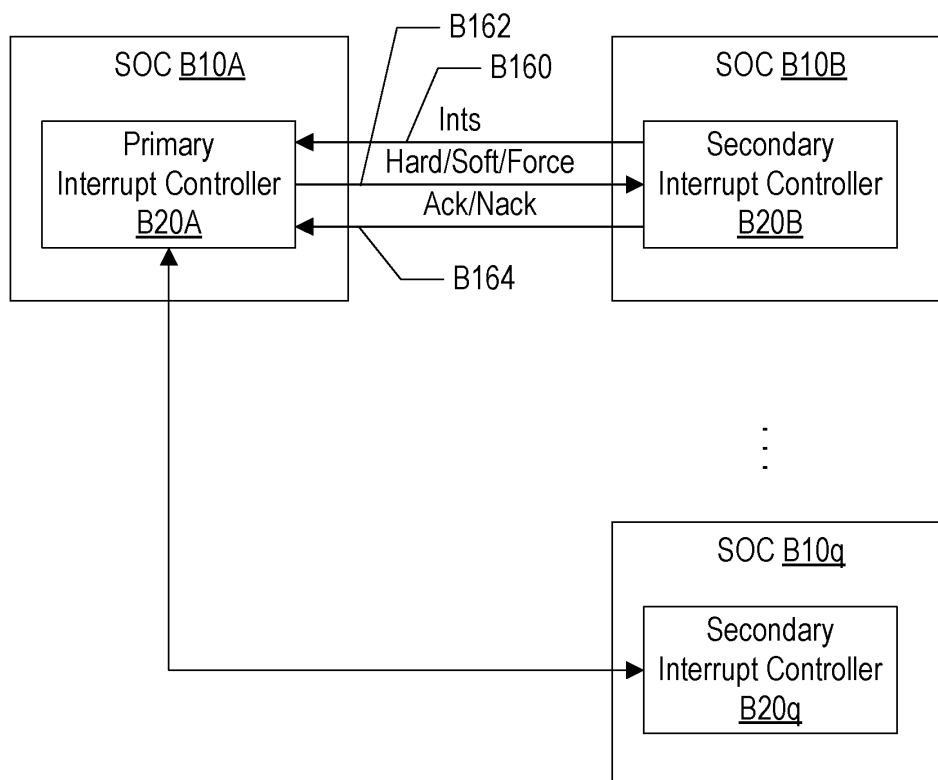


FIG. 23

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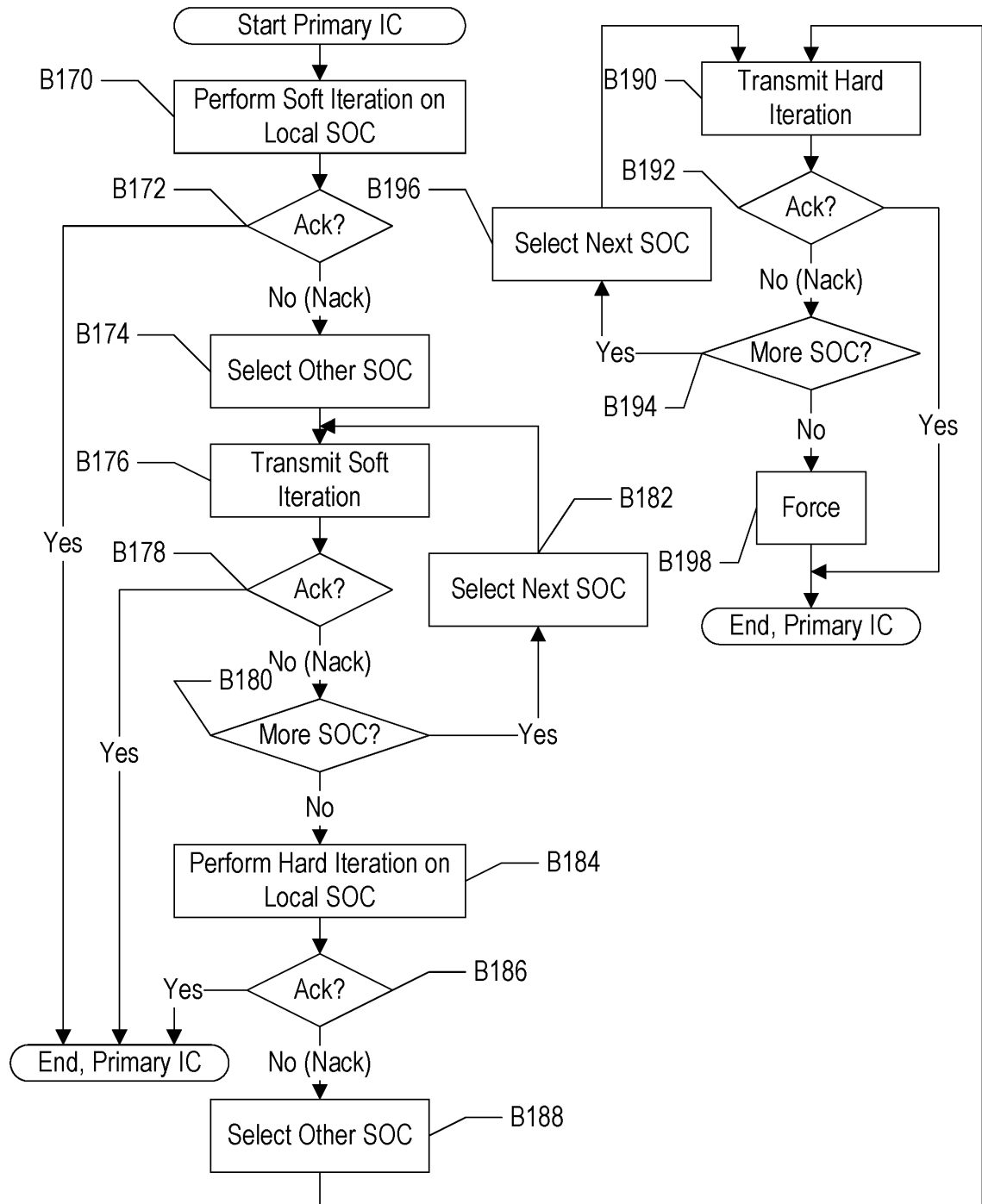


FIG. 24

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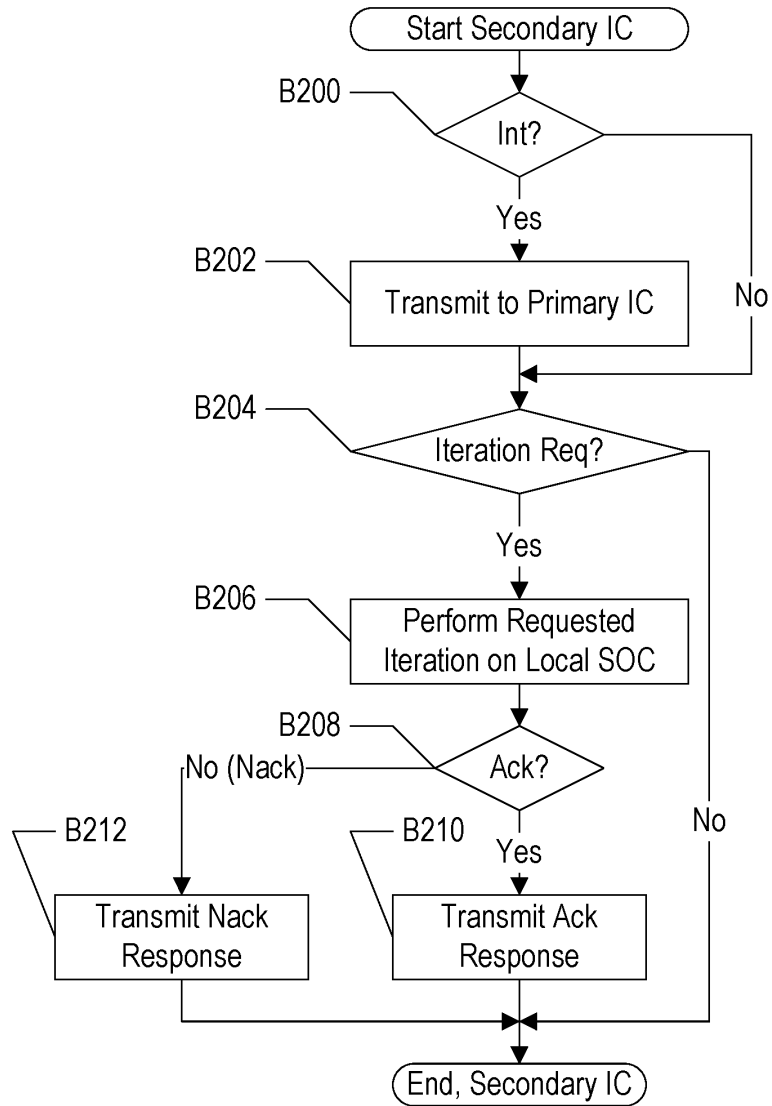


FIG. 25

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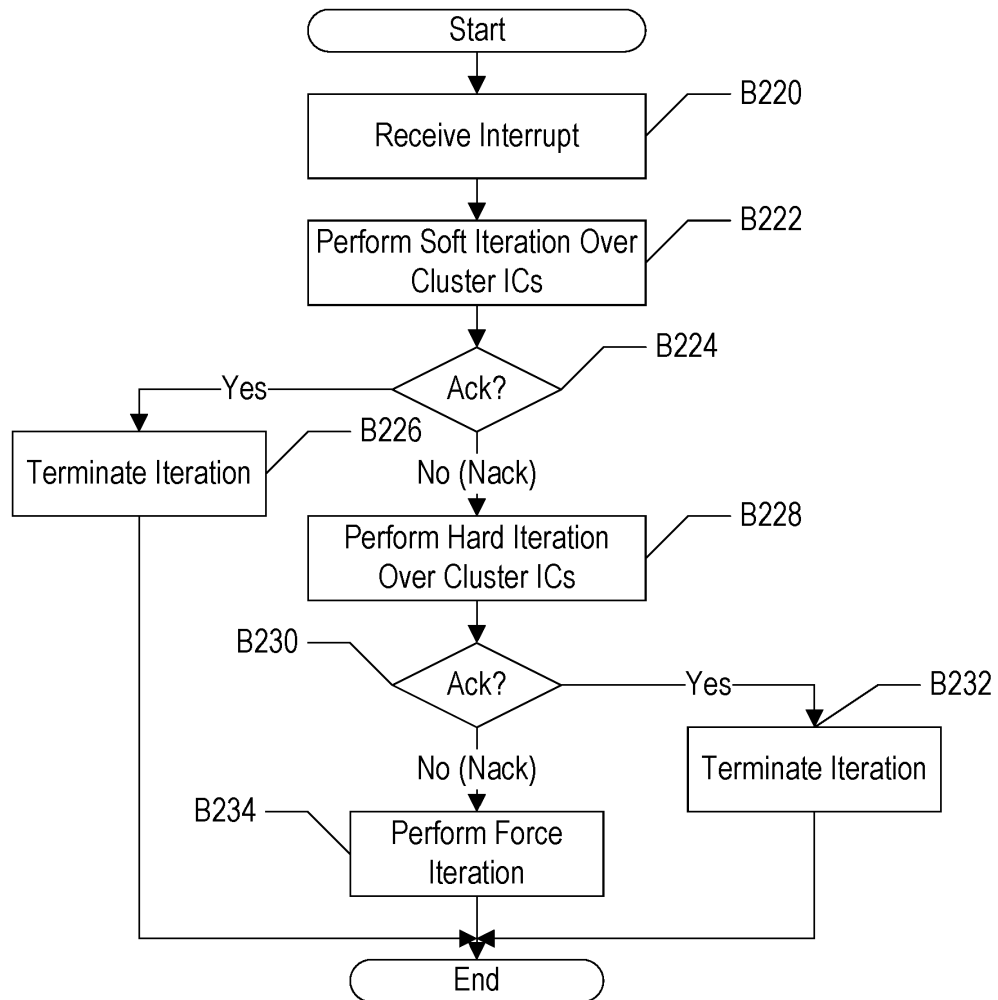


FIG. 26

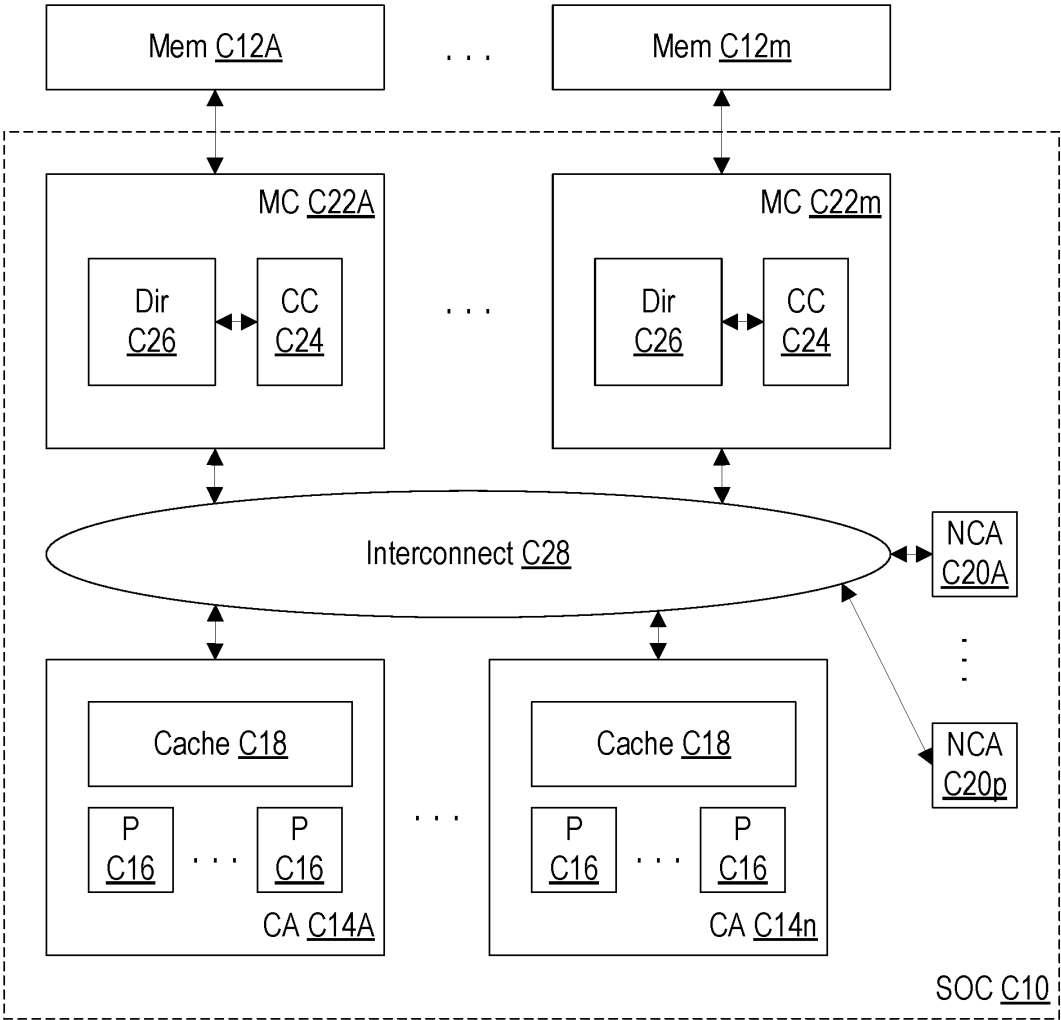


FIG. 27

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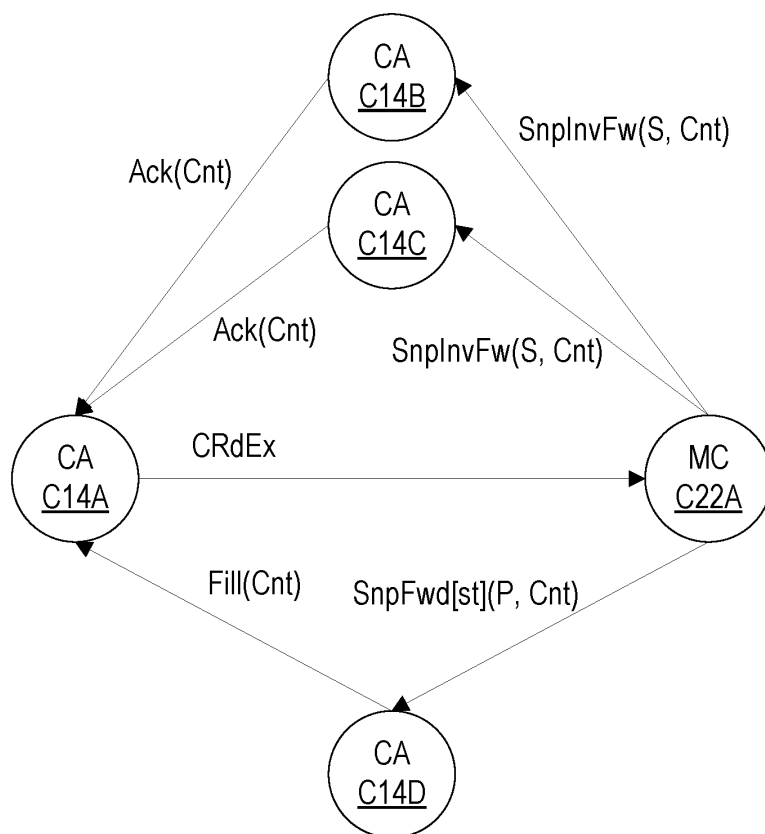


FIG. 28

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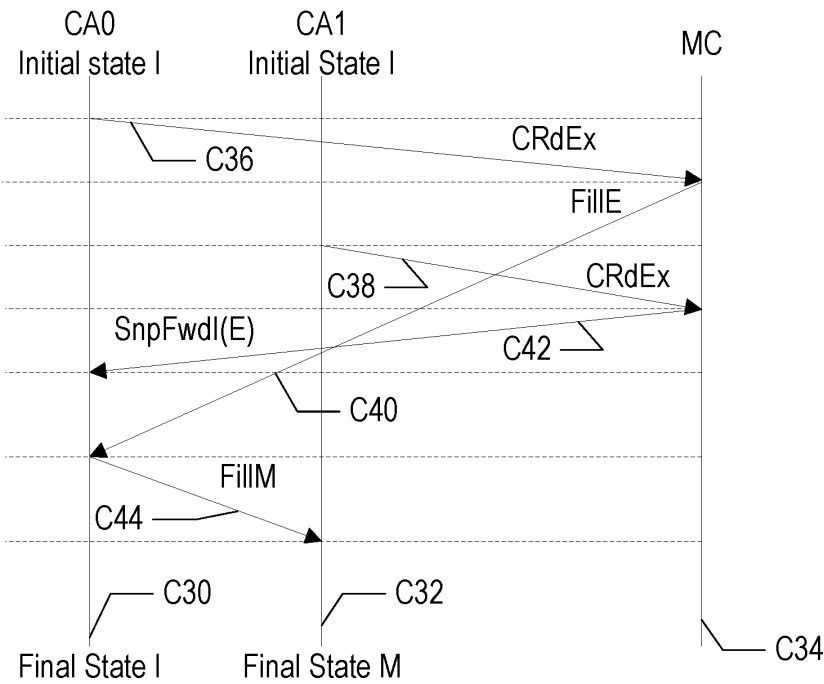


FIG. 29

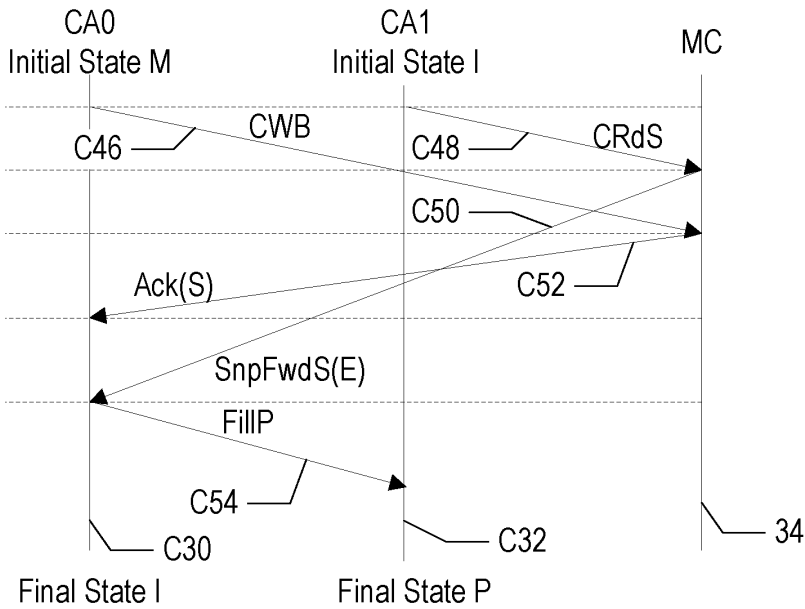


FIG. 30

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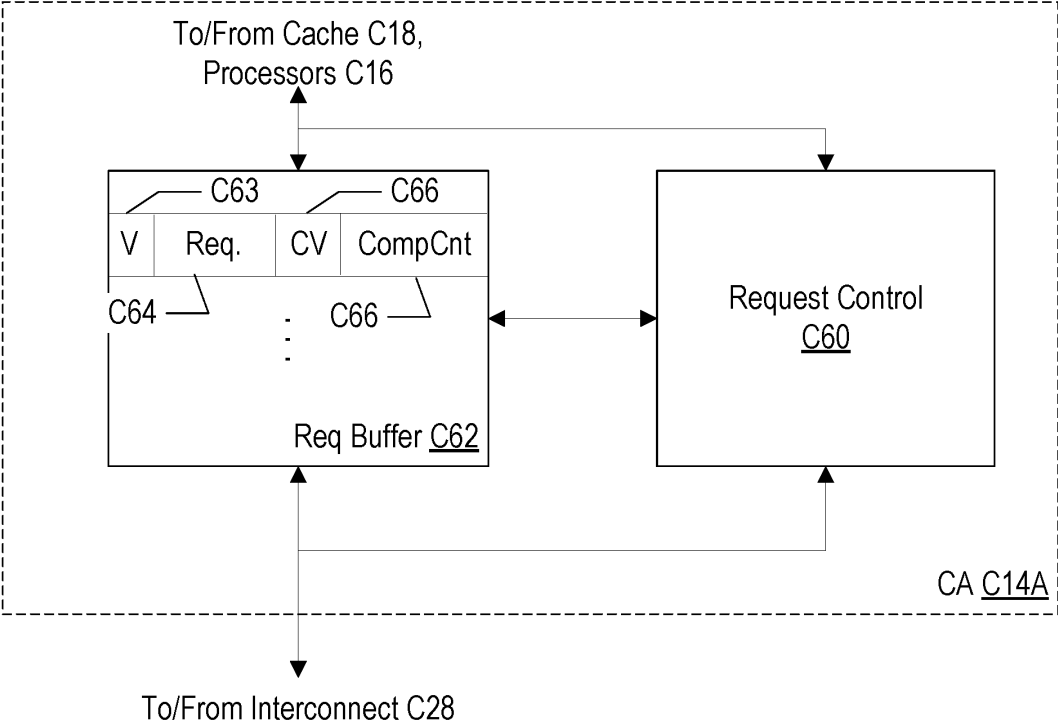


FIG. 31

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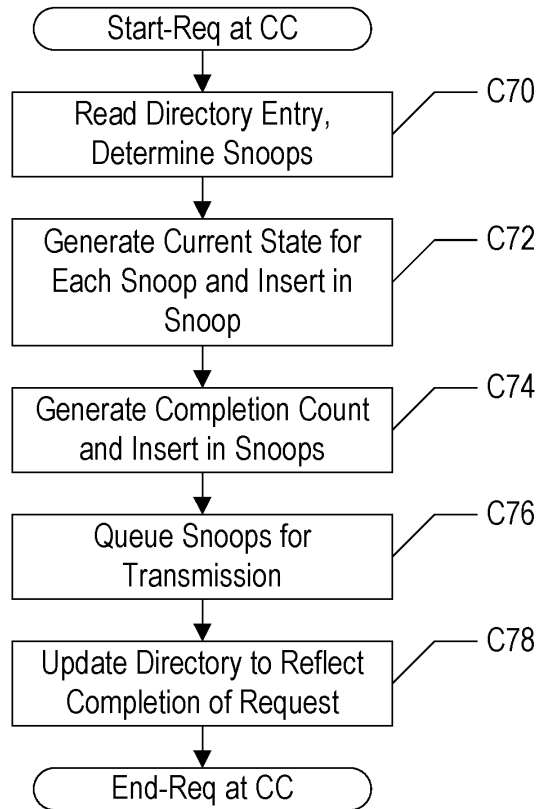


FIG. 32

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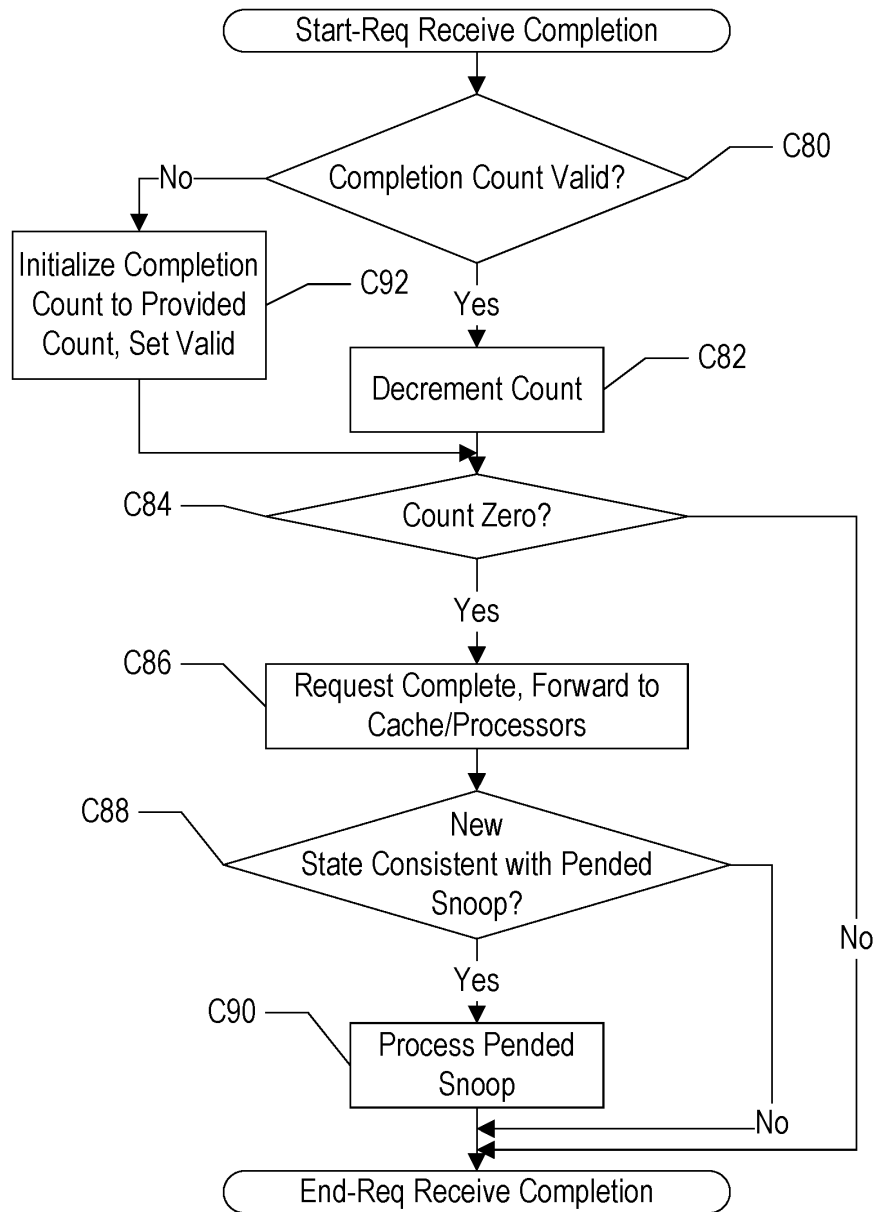


FIG. 33

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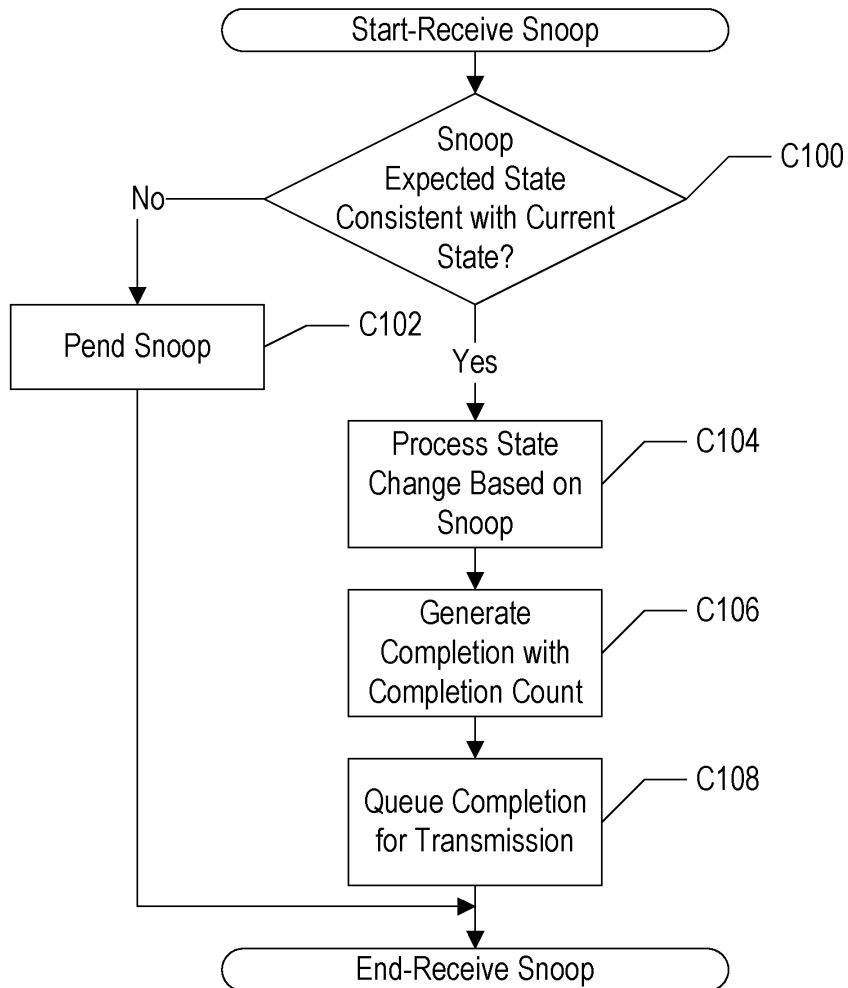


FIG. 34

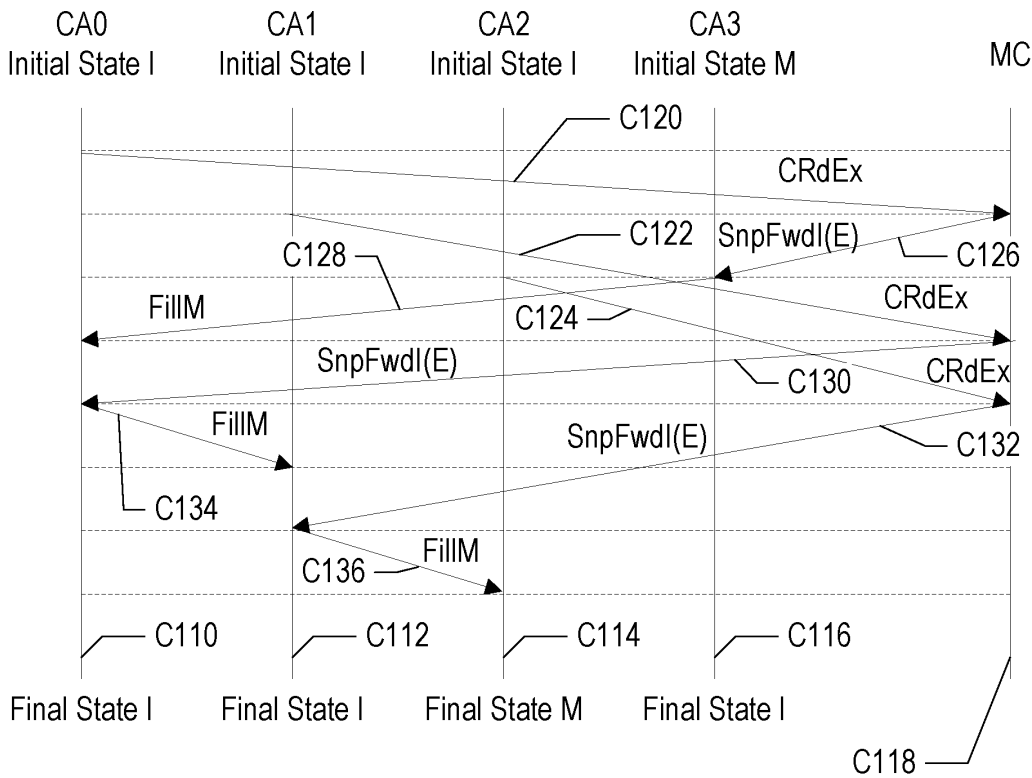


FIG. 35

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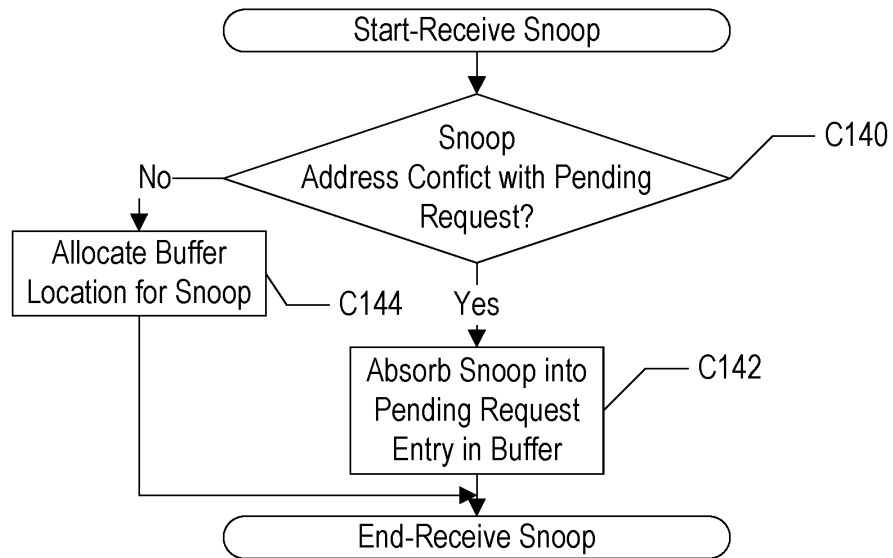


FIG. 36

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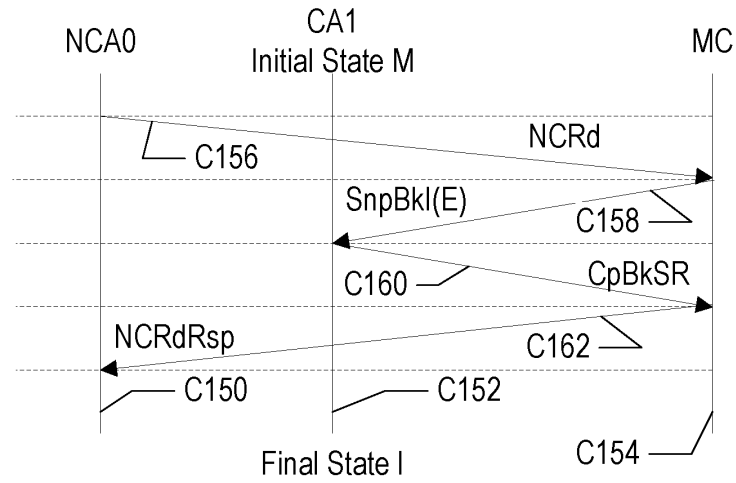


FIG. 37

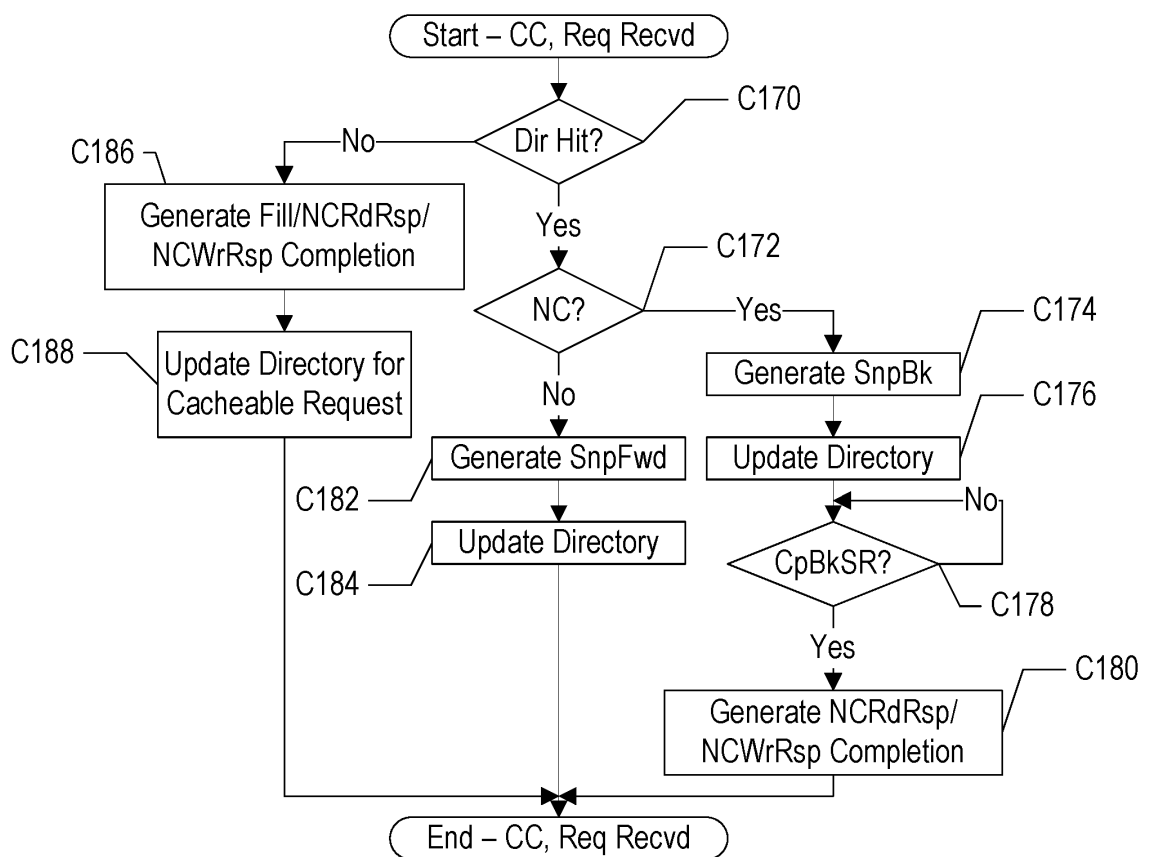


FIG. 38

<u>State</u>	<u>Meaning</u>
M	Dirty Exclusive (modified)
O	Dirty Shared (owned)
E	Clean Exclusive
EnD	Clean Exclusive, No Data
P	Clean Shared Primary
S	Clean Shared Secondary
I	Invalid

C190

FIG. 39

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<u>Message</u>	<u>Meaning</u>
CRdXX	Cacheable Read. XX= requested cache state, may be opportunistic.
CtoE[Cond]	Change to Exclusive. Conditional for Store Conditional Instruction.
CRdE-Only	Cacheable Read Exclusive, to transition to EnD state.
NCRd	Non-Cacheable Read.
NCWr	Non-Cacheable Write.
SnxFwdXX	Snoop, forward data to requestor. XX=state in receiver after snoop.
SnxBkXX	Snoop, return data to memory controller. XX=state in receiver after snoop.
SnplnvFw	Snoop invalidate, completion to requesting agent.
SnplnvBk	Snoop invalidate, completion to coherency controller.
FillXX	Fill Data Completion, XX=state of the block for requestor.
Ack	Acknowledgement Completion.
CWB	Cacheable Write Back to Memory, for eviction.
CpBkSR	Copy back to Memory, for snoop response.
NCWrRsp	Non-Cacheable Write Completion.
NCRdRsp	Non-Cacheable Read Completion.

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FIG. 40

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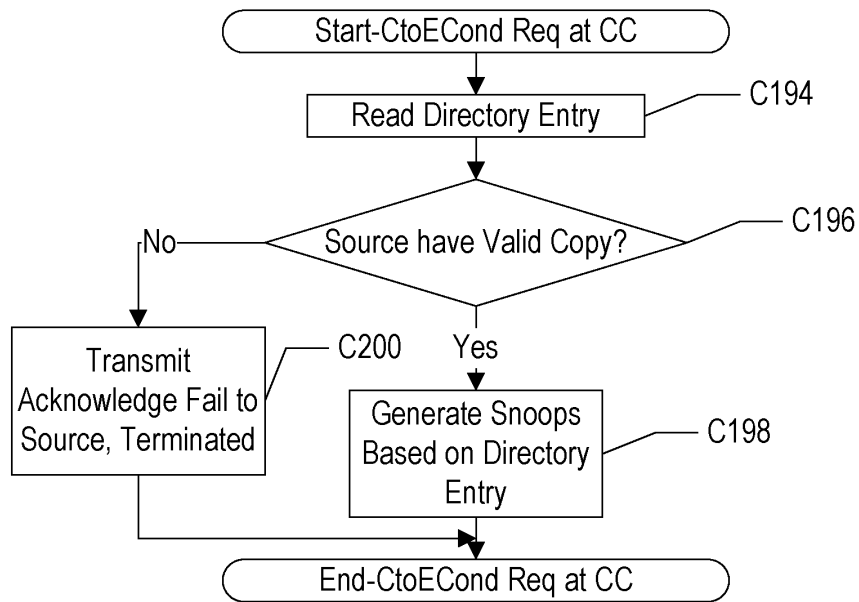


FIG. 41

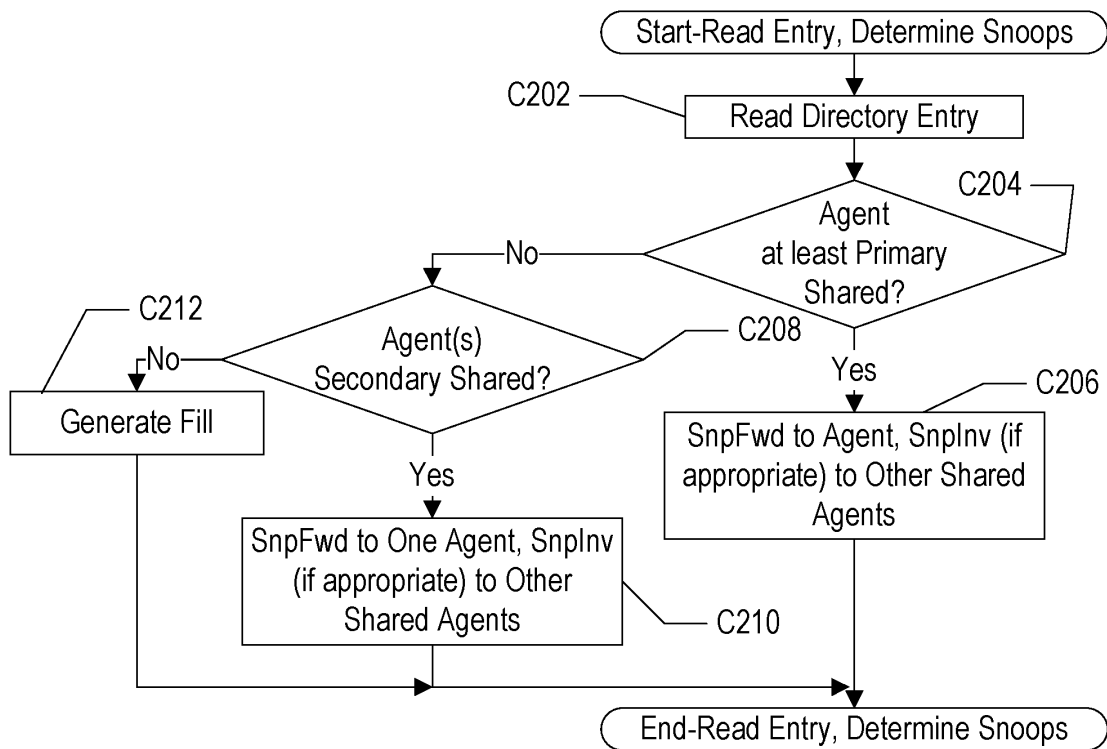


FIG. 42

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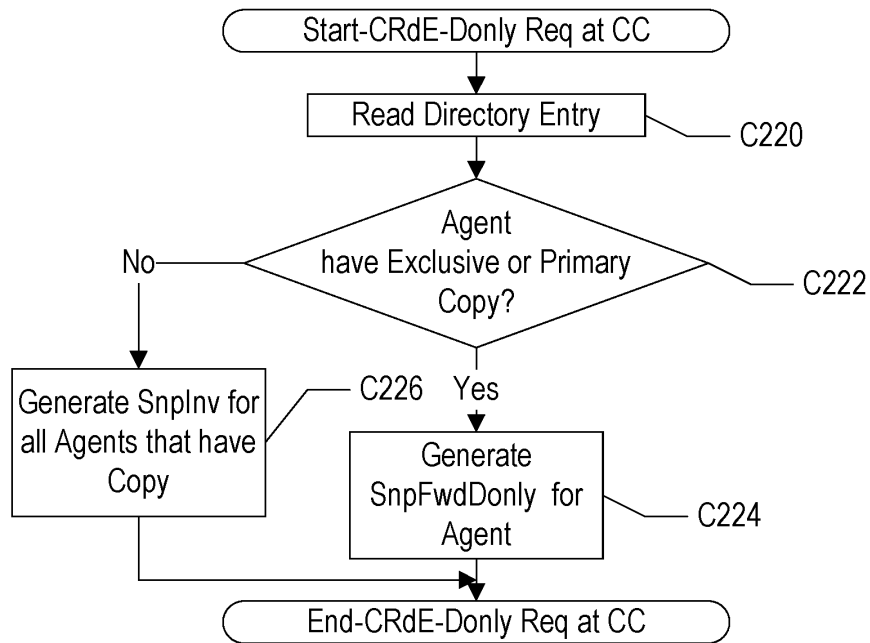


FIG. 43

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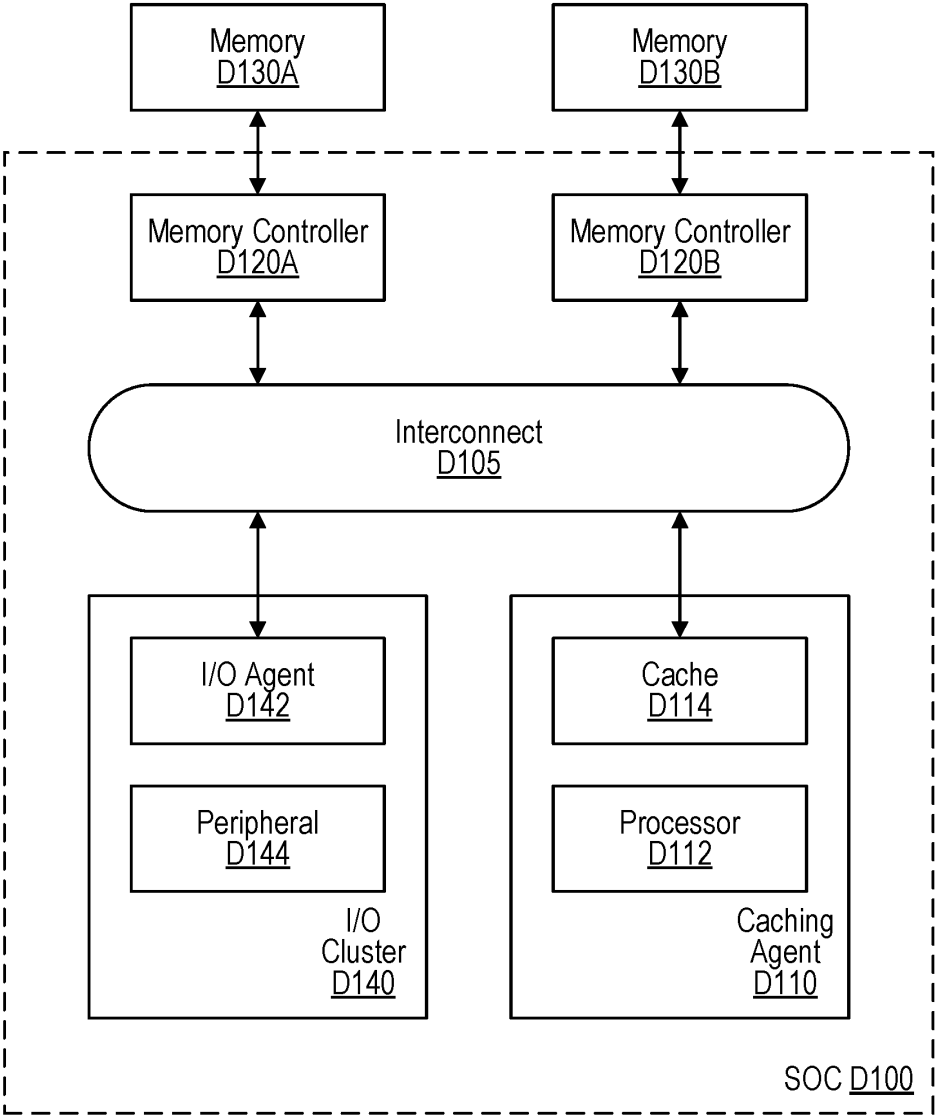


FIG. 44

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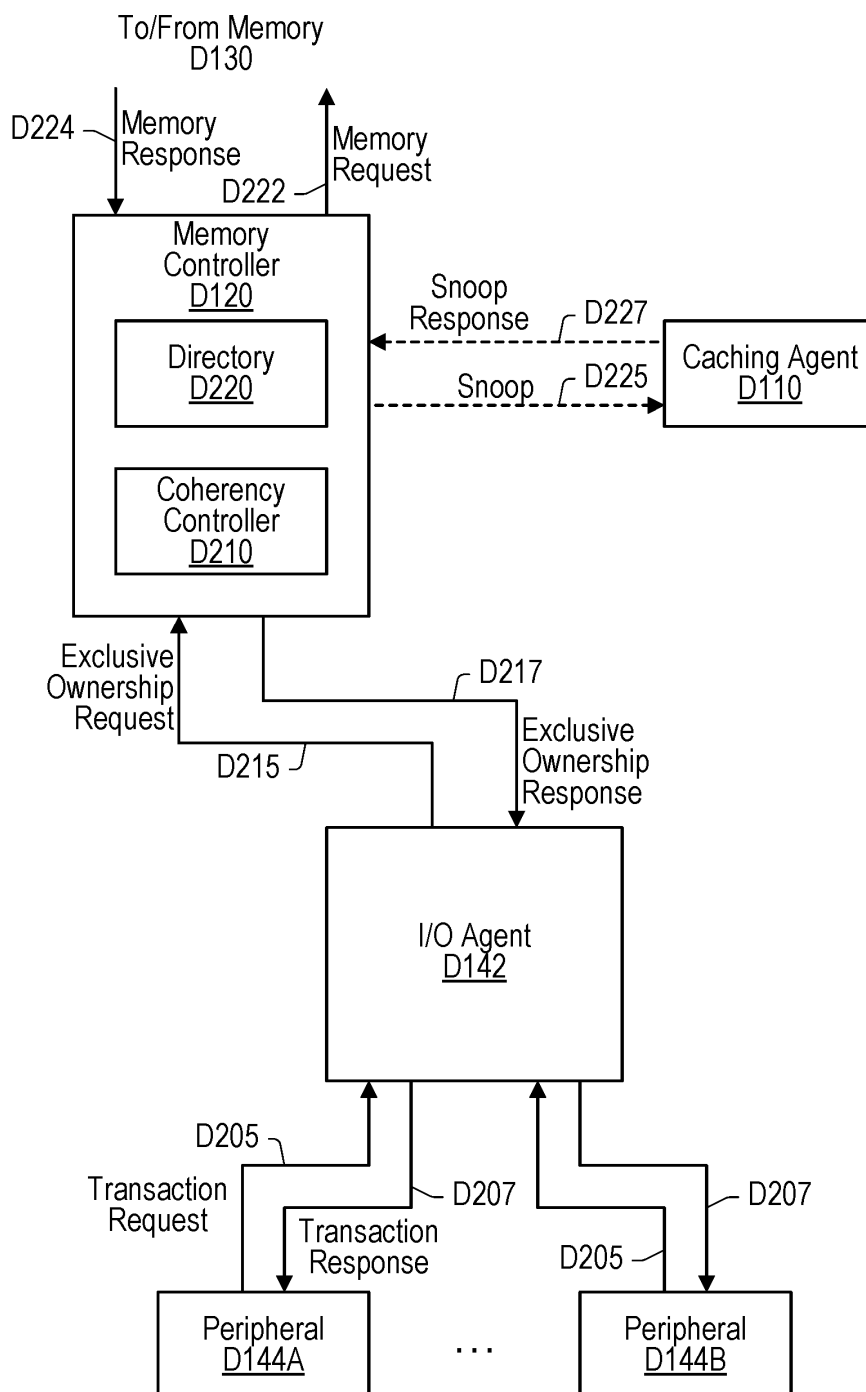


FIG. 45

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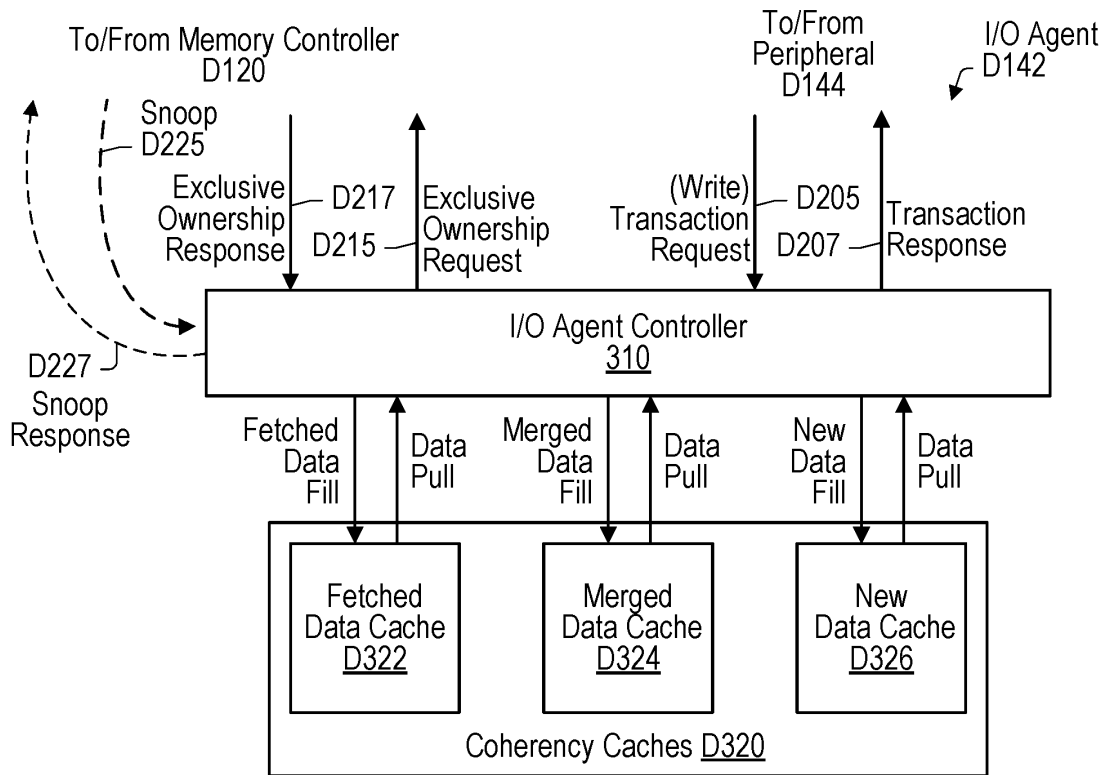


FIG. 46A

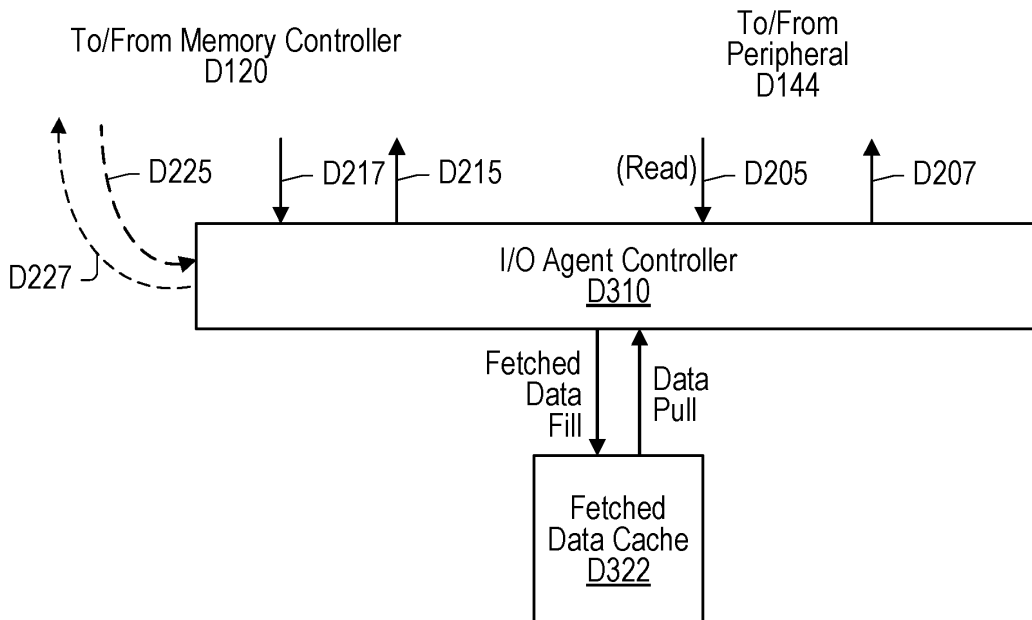


FIG. 46B

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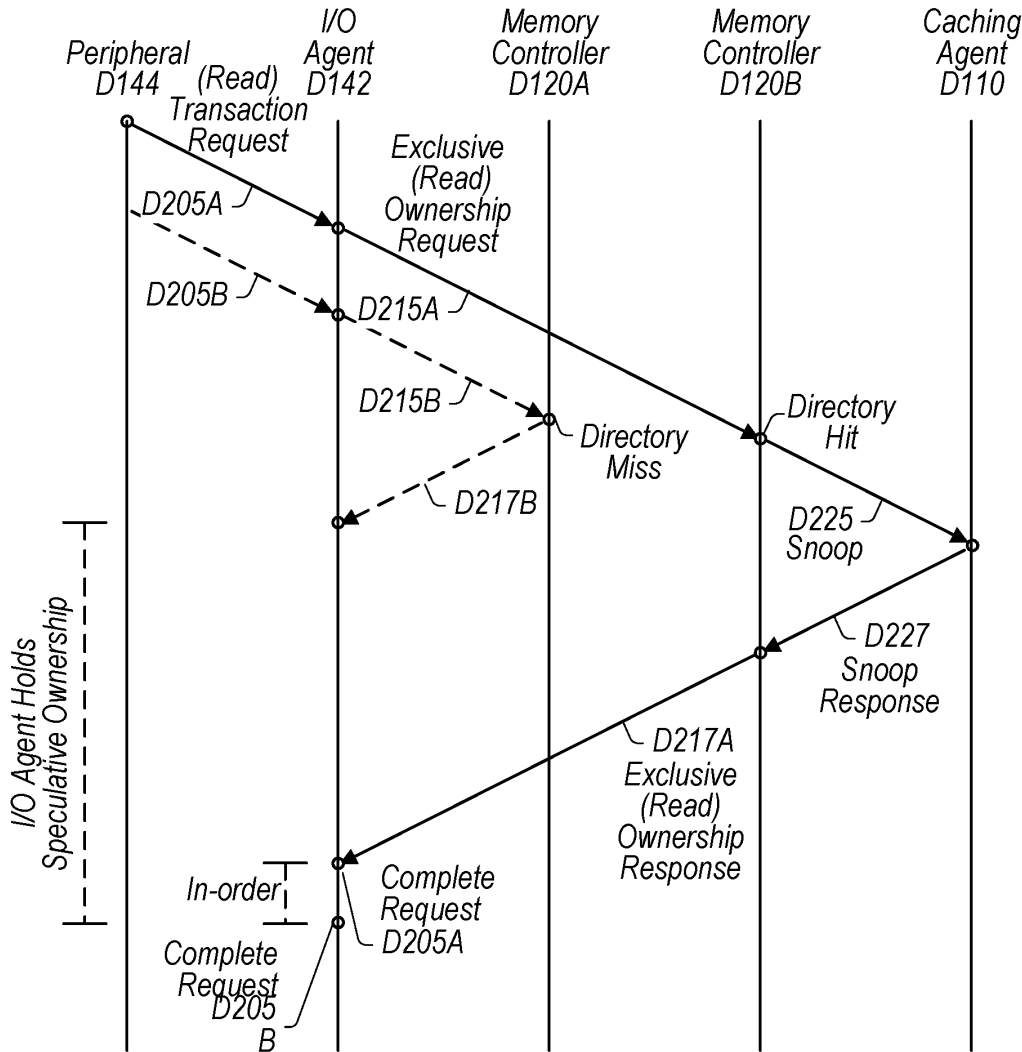
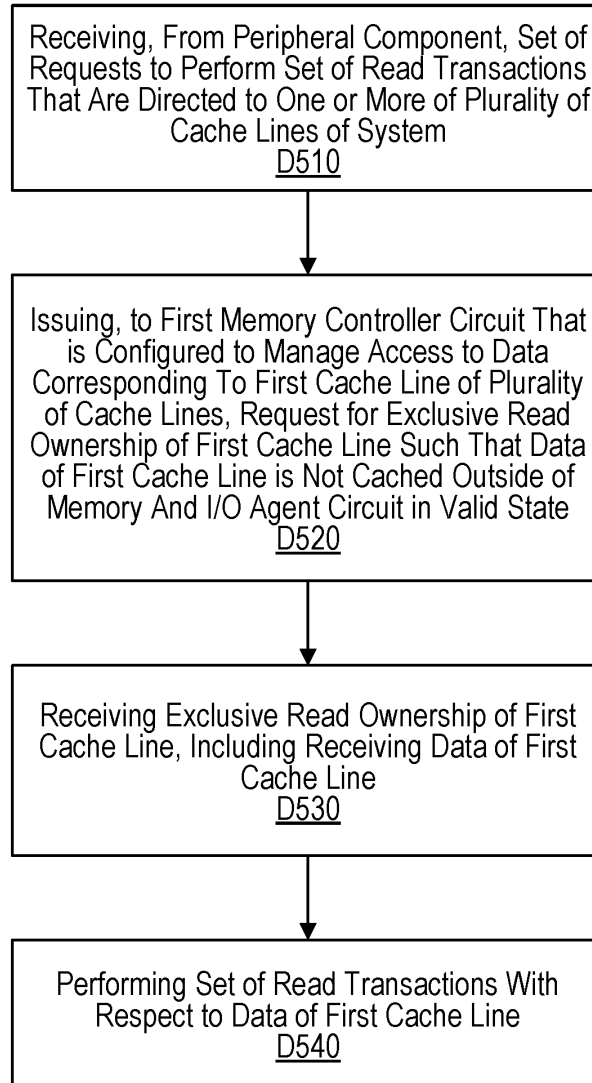


FIG. 47

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D500*FIG. 48*

System E100

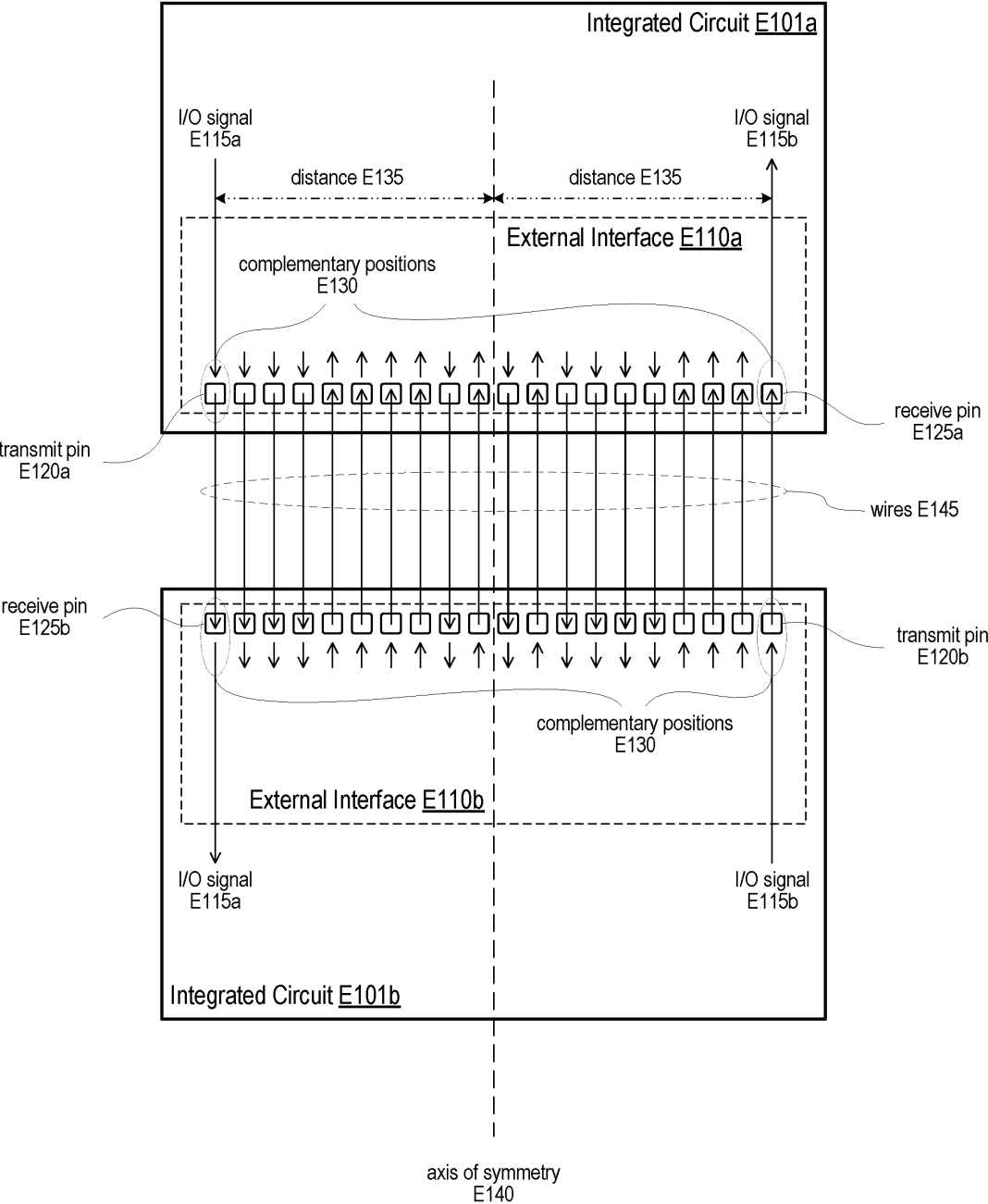


FIG. 49

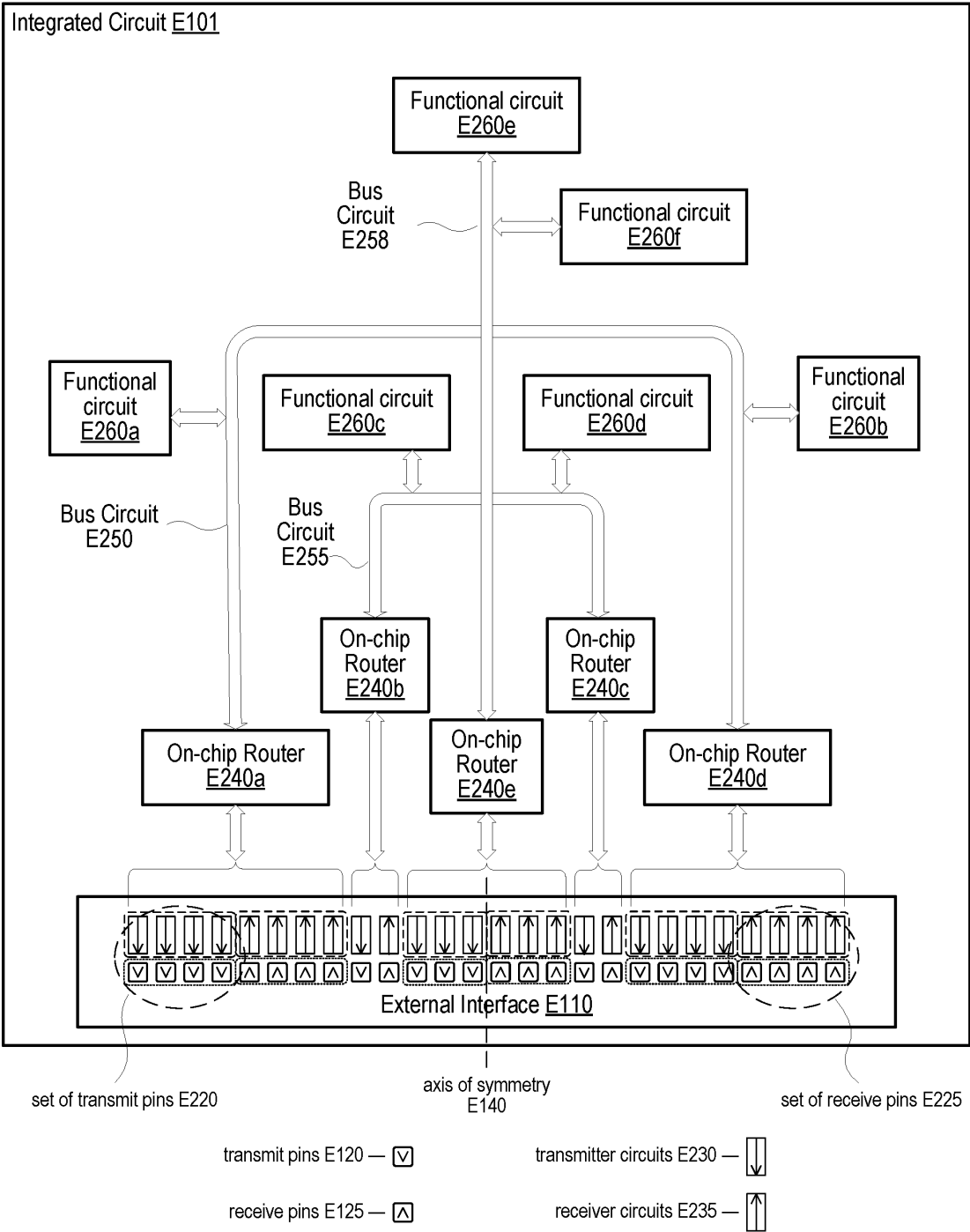


FIG. 50

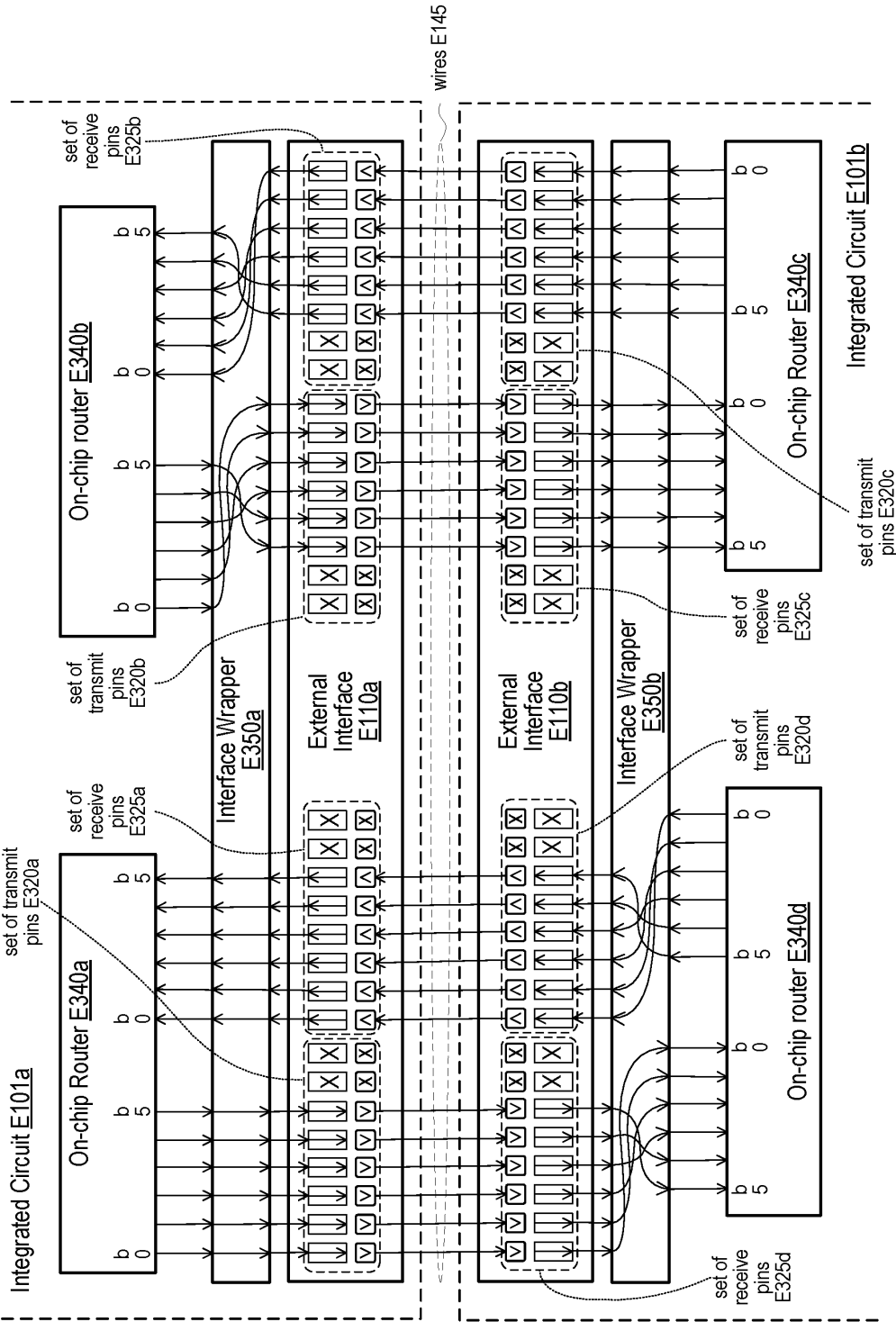


FIG. 51

System E300

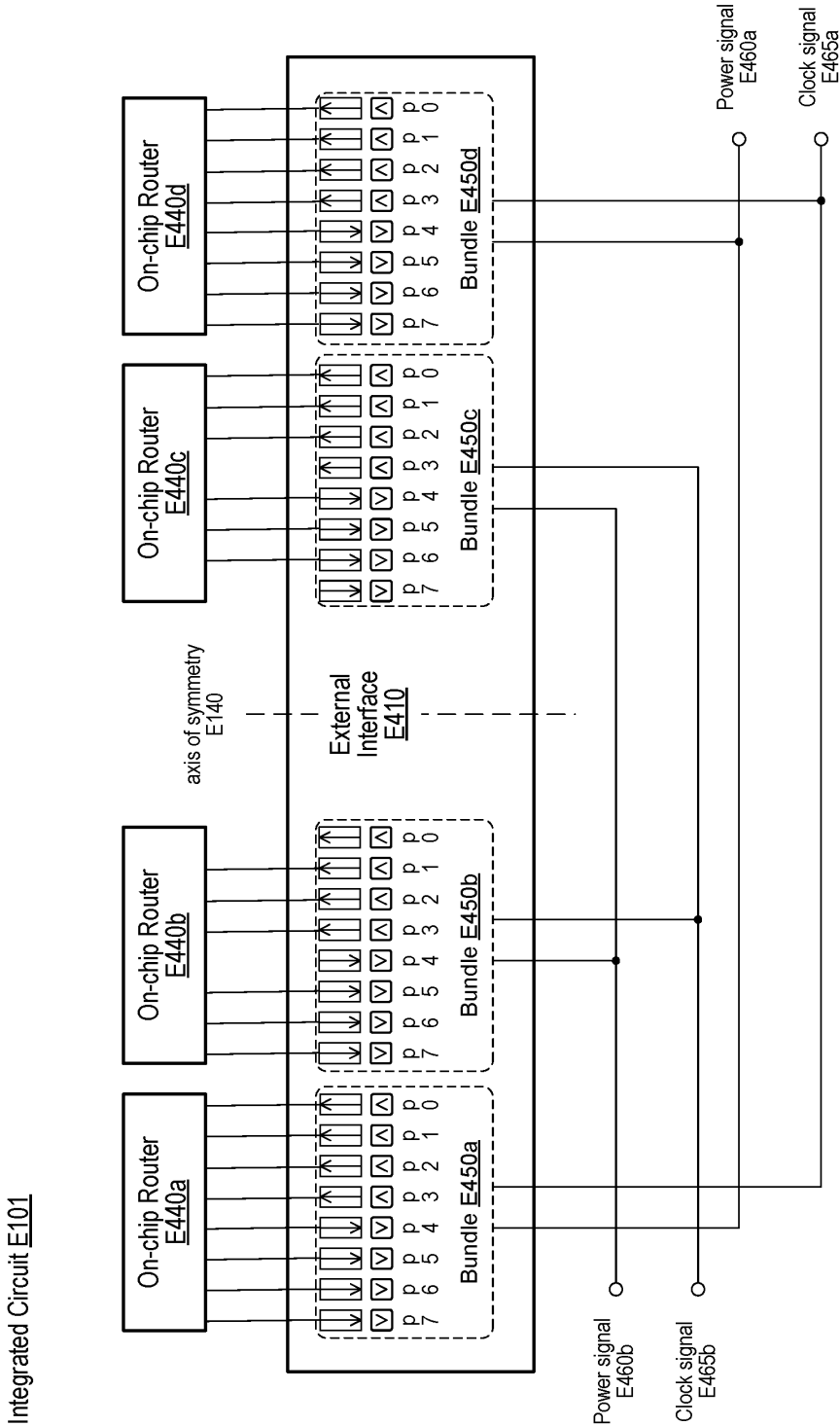


FIG. 52

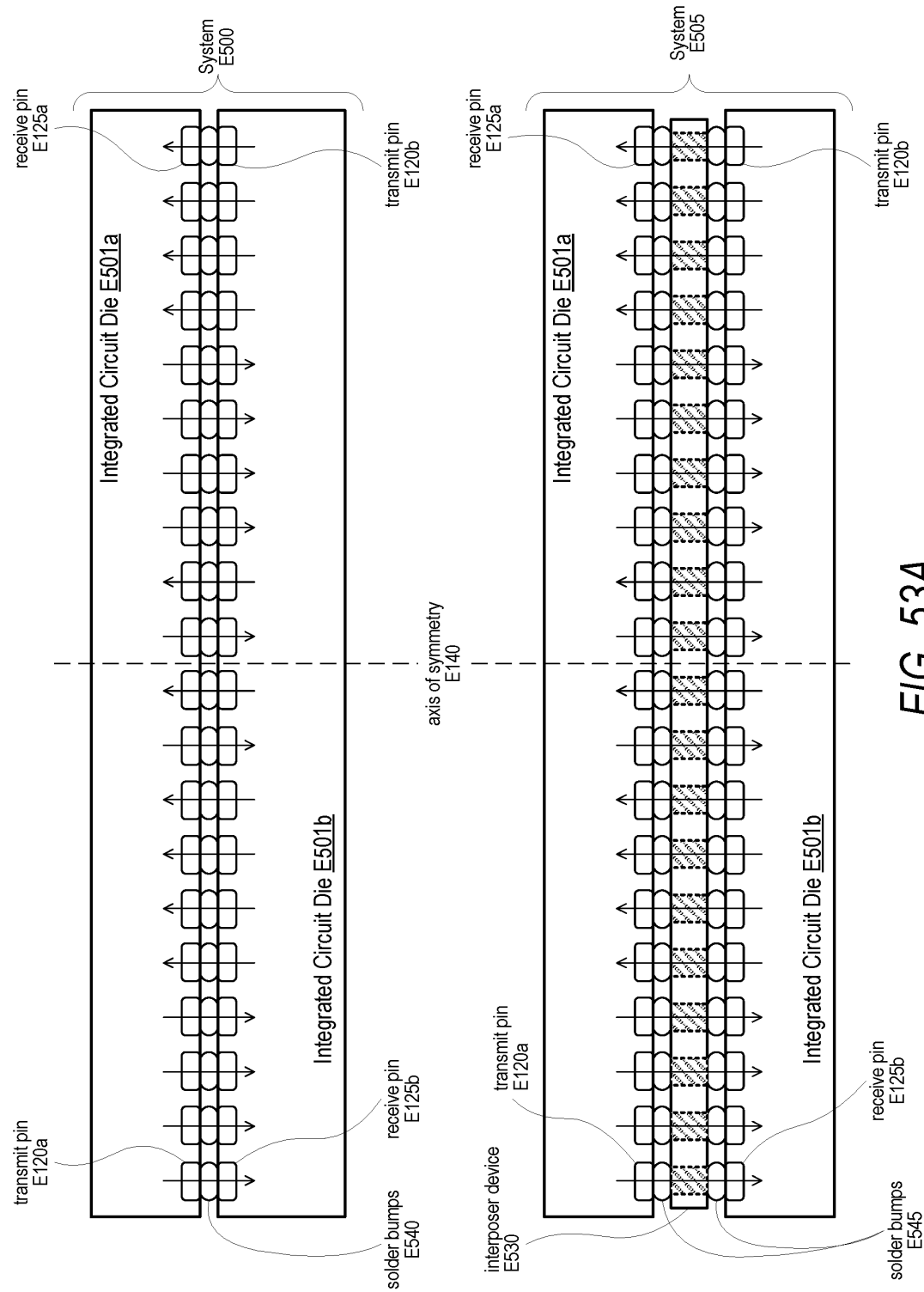


FIG. 53A

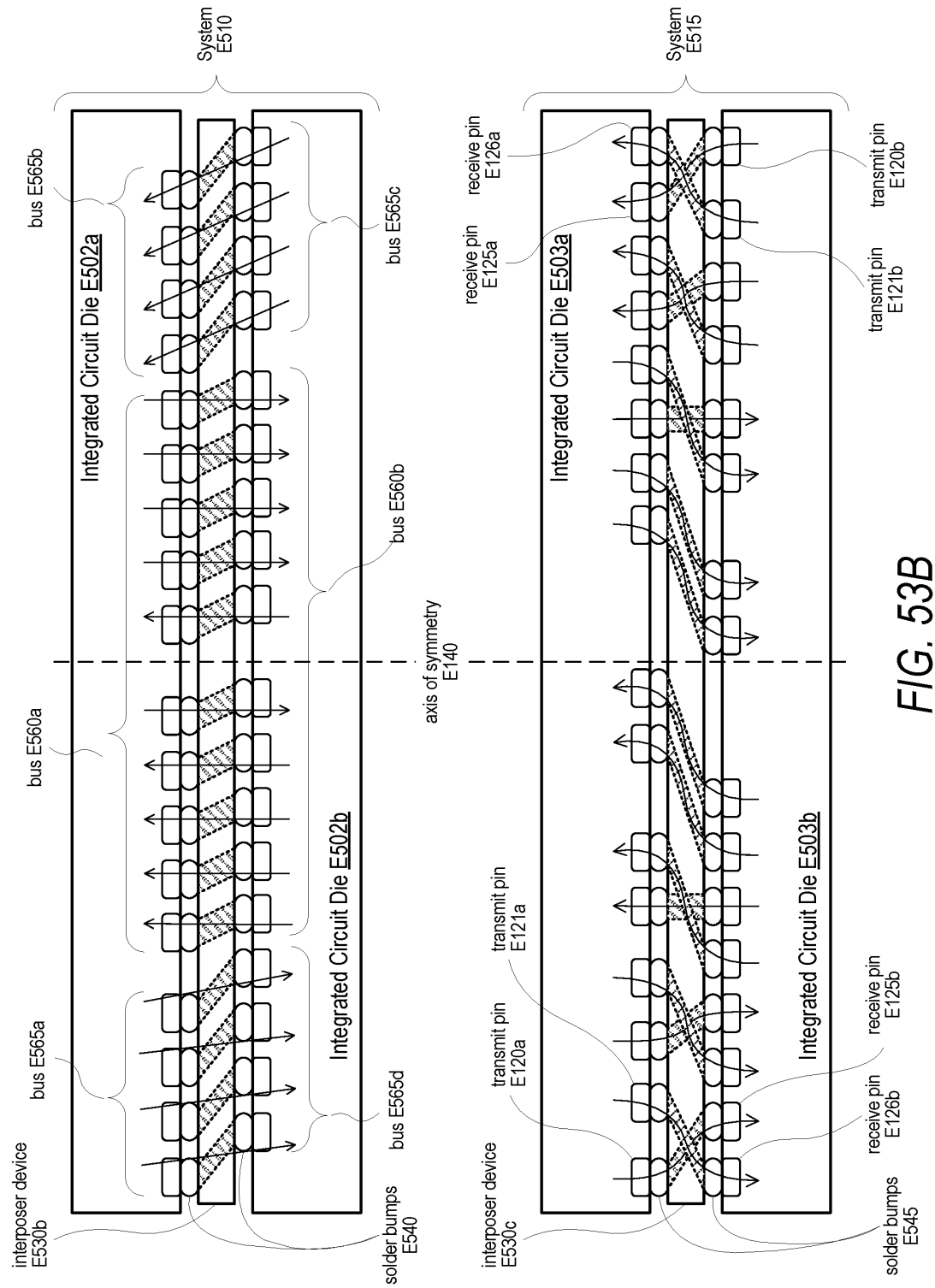
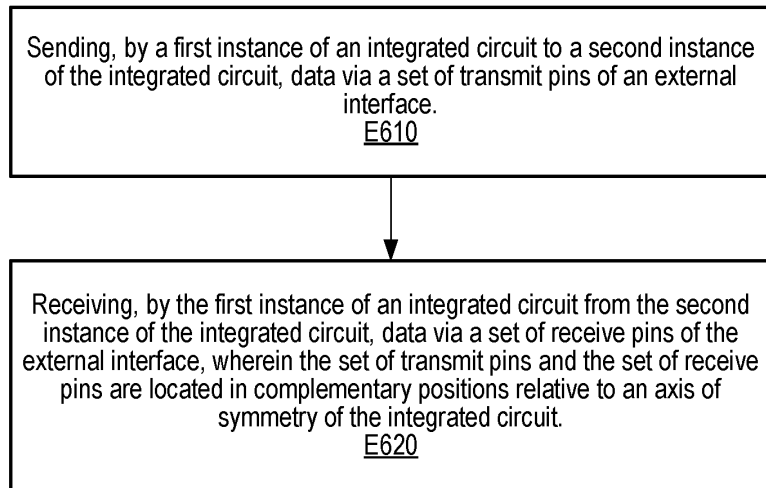


FIG. 53B

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E600*FIG. 54*

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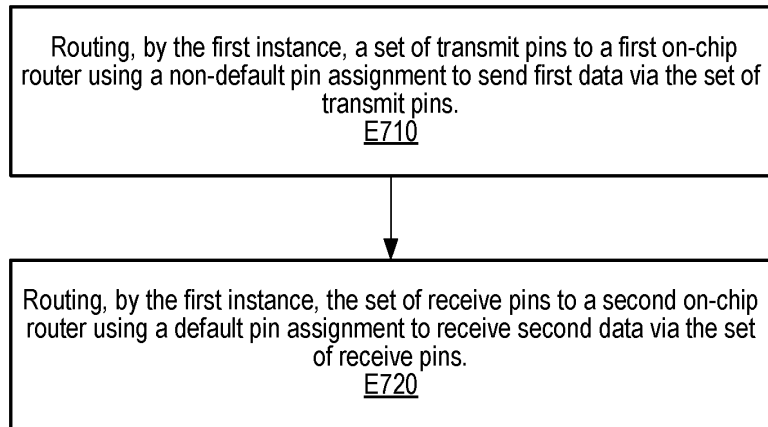
E700

FIG. 55

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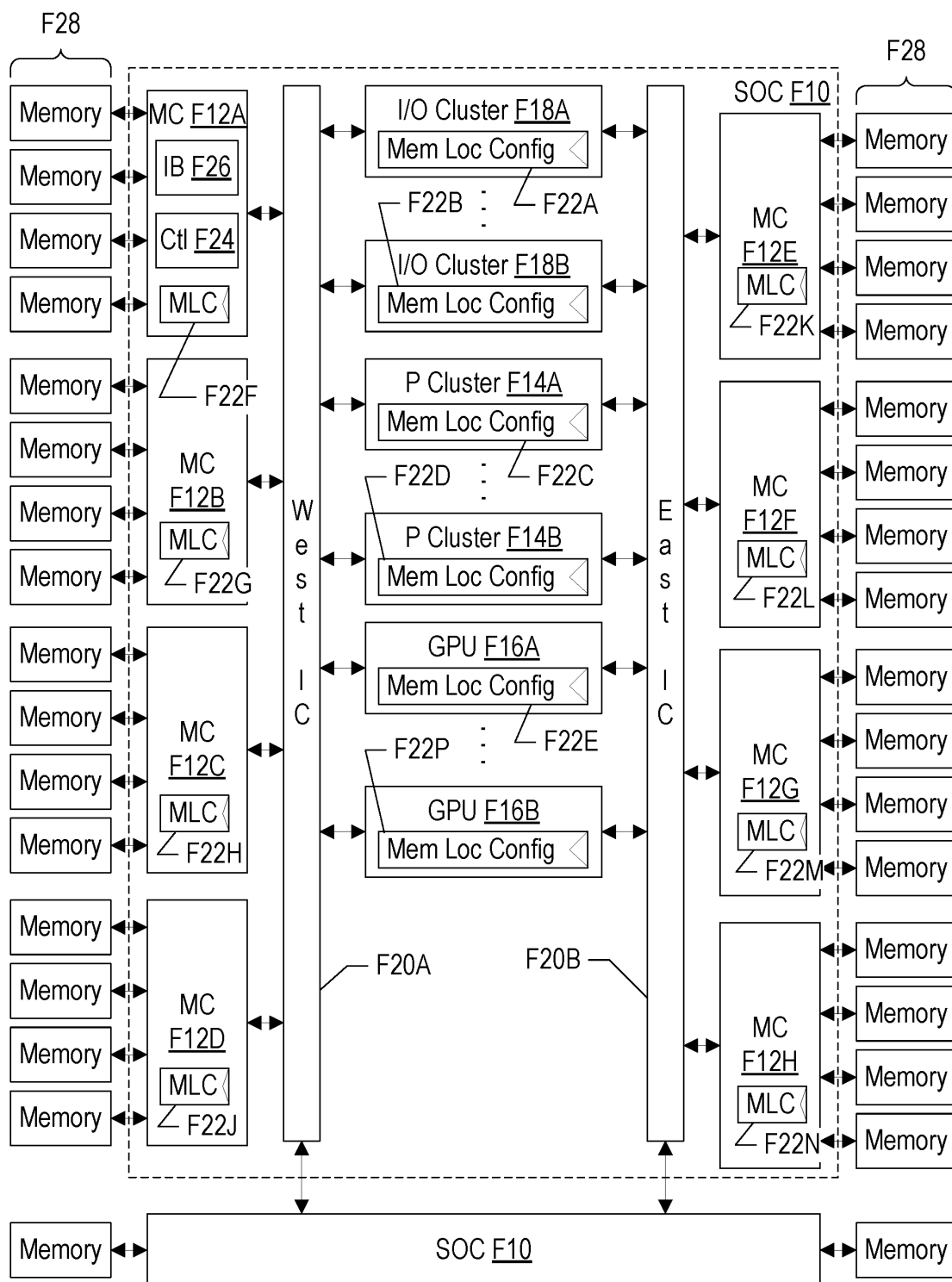


FIG. 56

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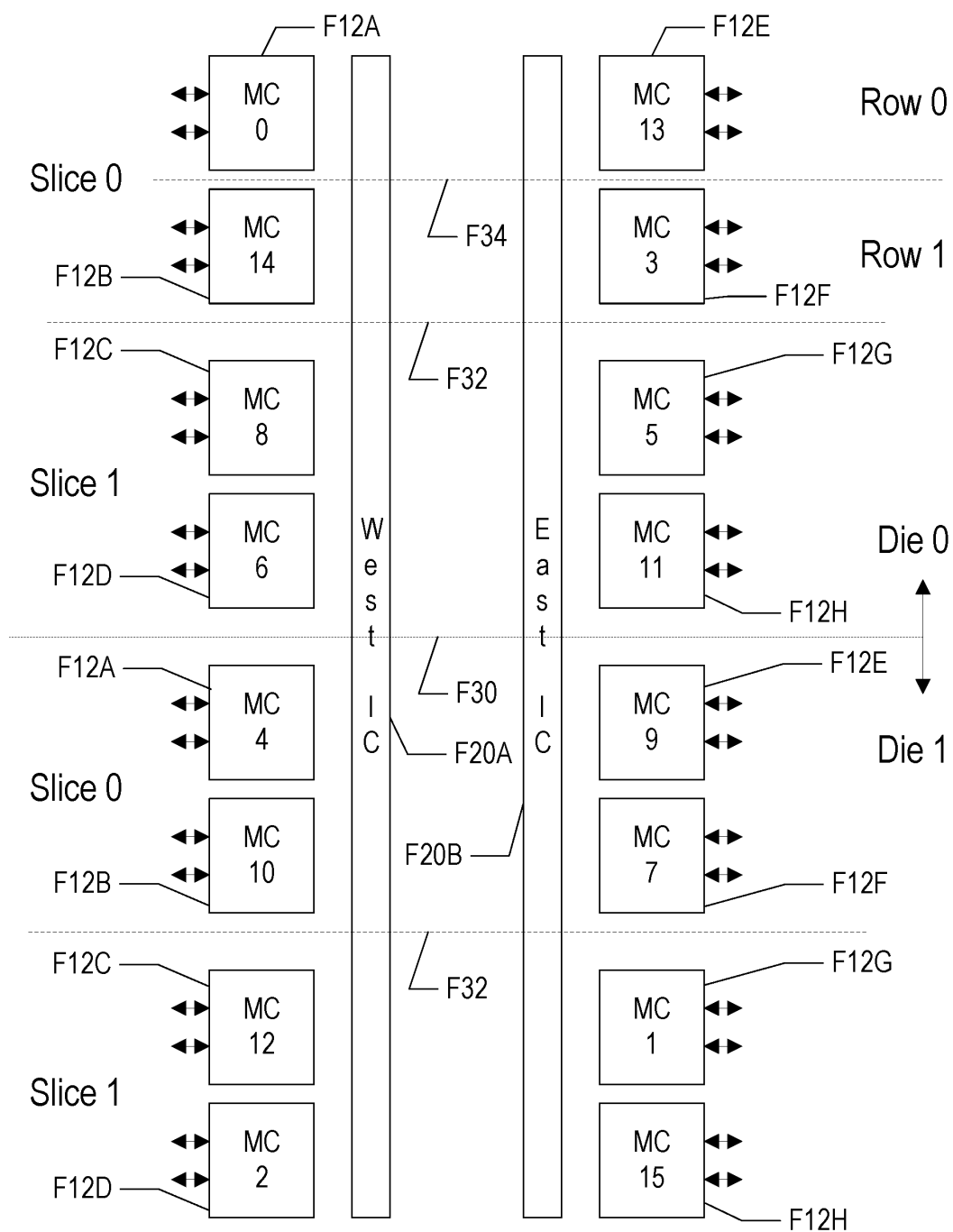


FIG. 57

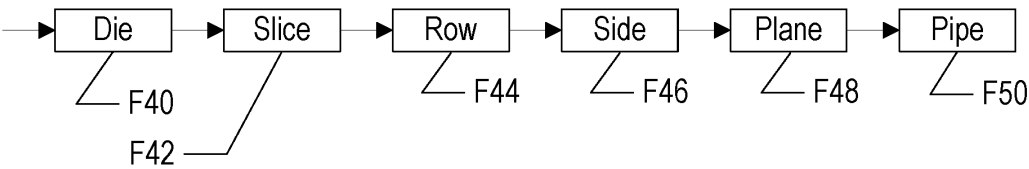


FIG. 58

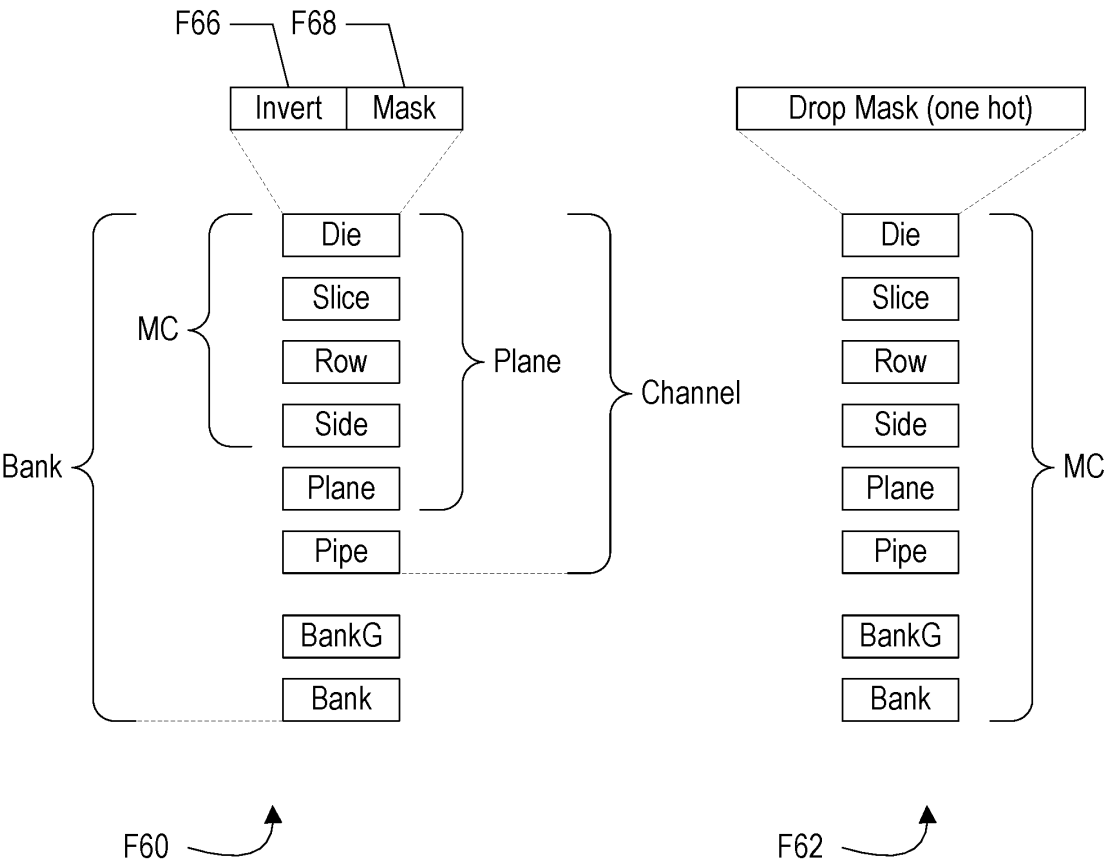


FIG. 59

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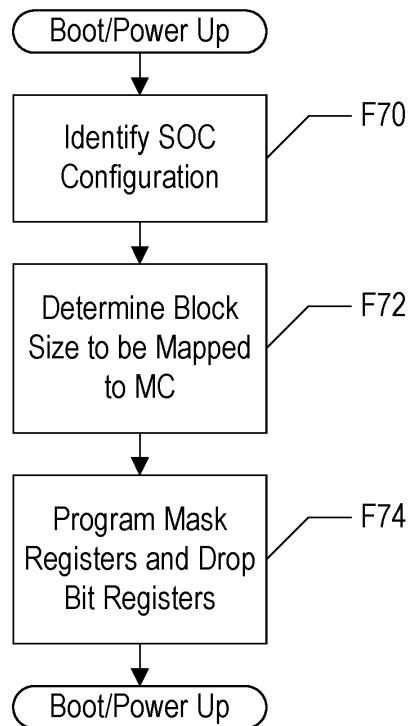


FIG. 60

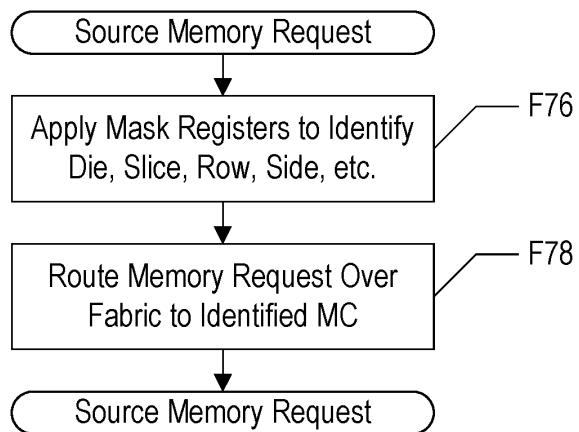


FIG. 61

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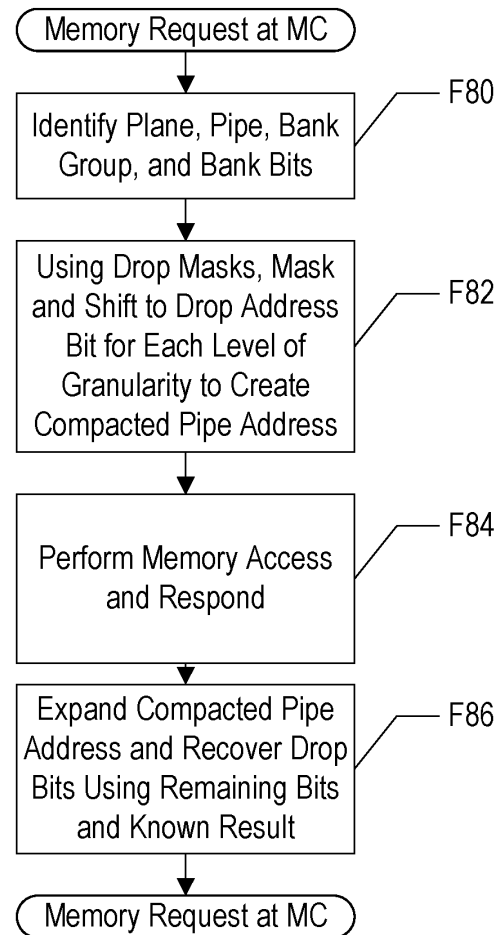


FIG. 62

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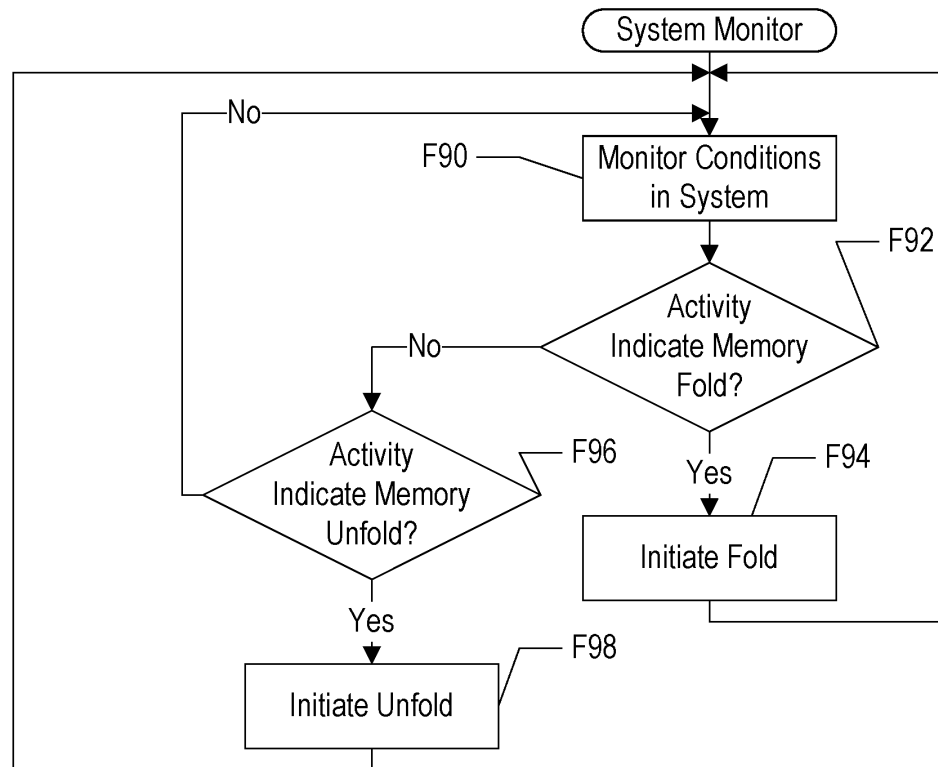


FIG. 63

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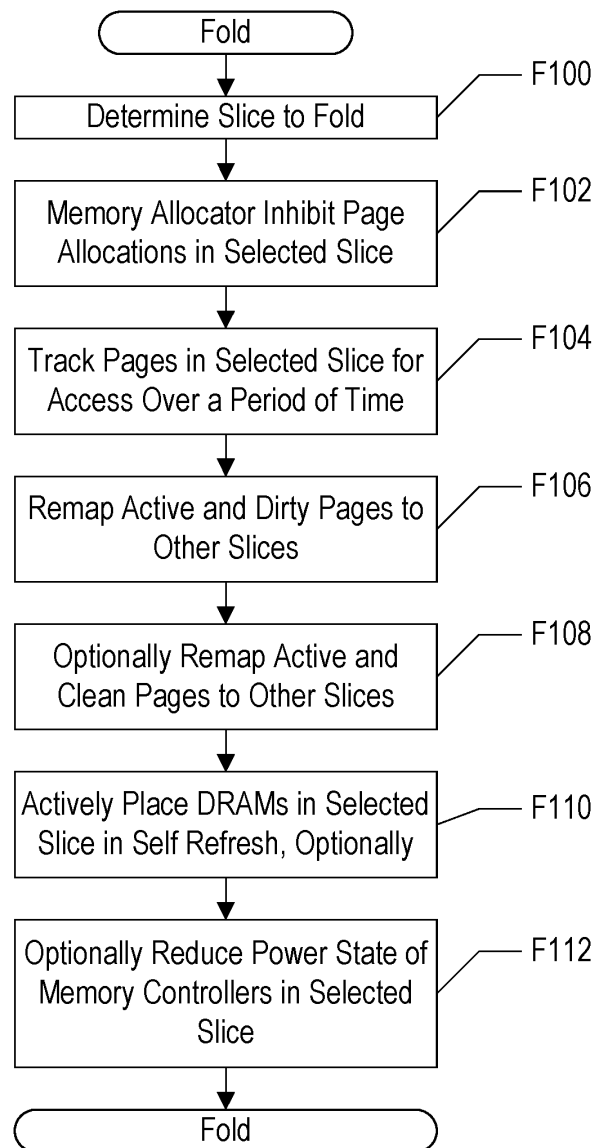


FIG. 64

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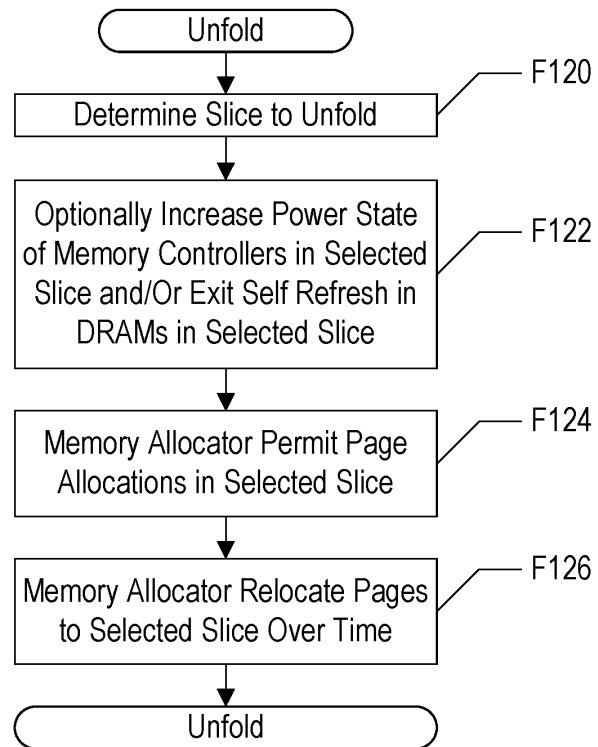


FIG. 65

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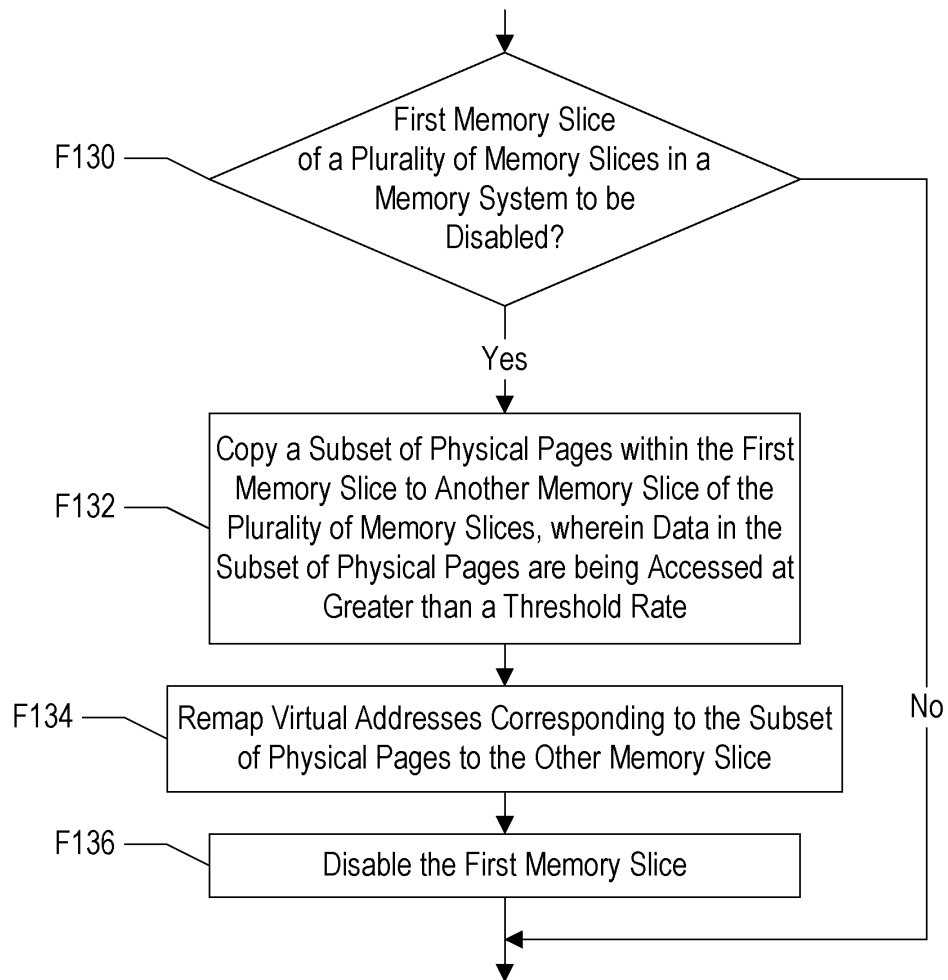


FIG. 66

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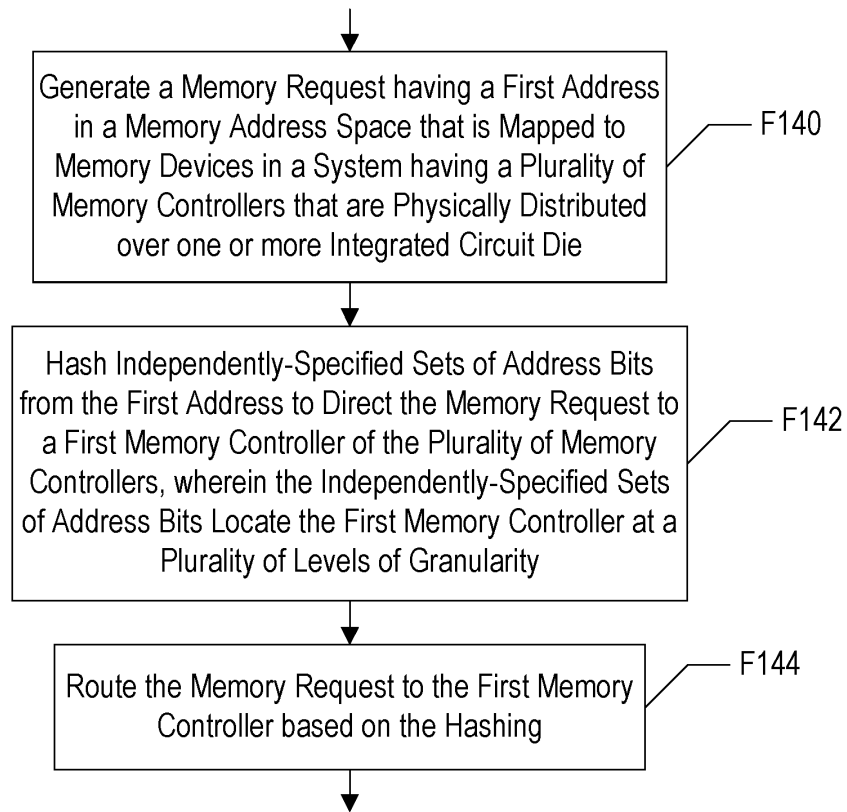


FIG. 67

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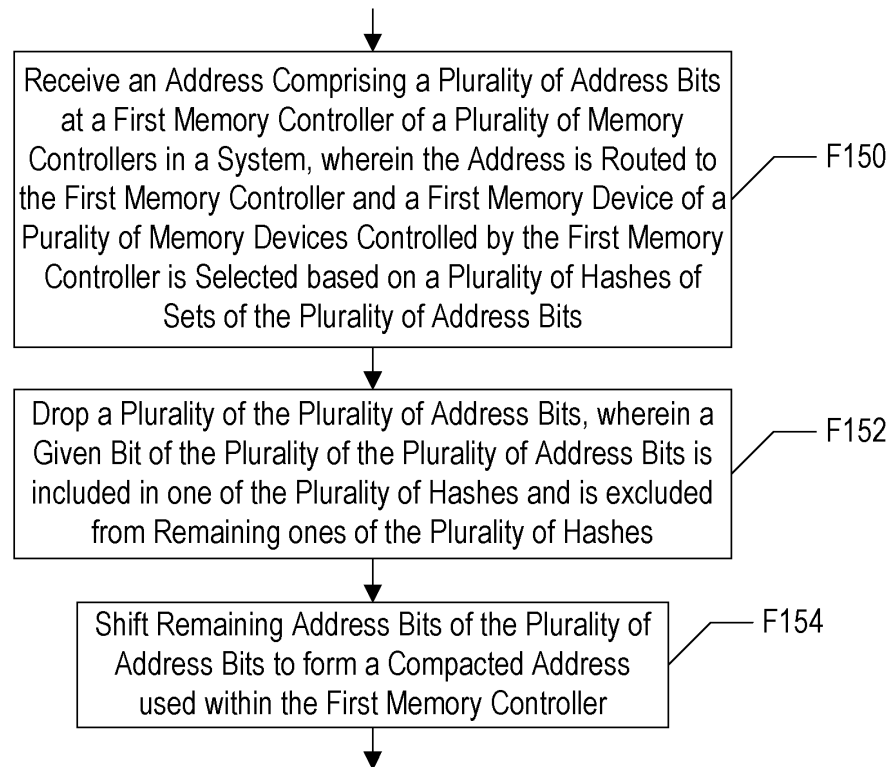


FIG. 68

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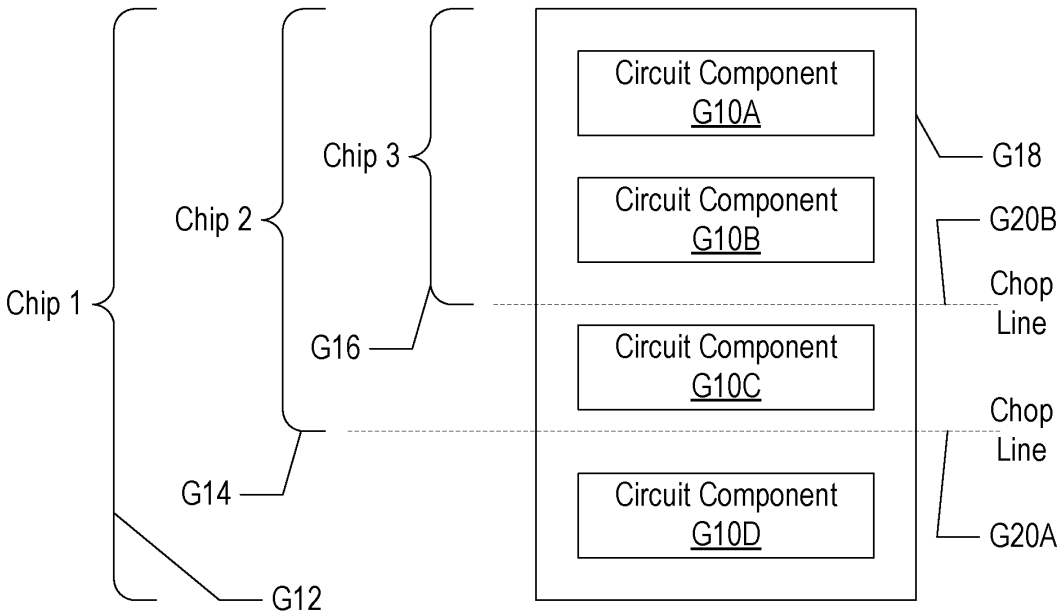


FIG. 69

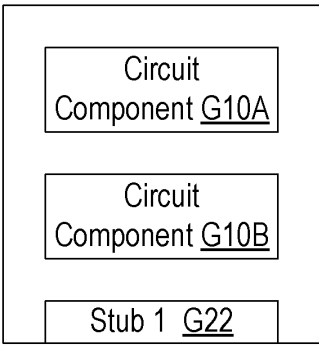


FIG. 70

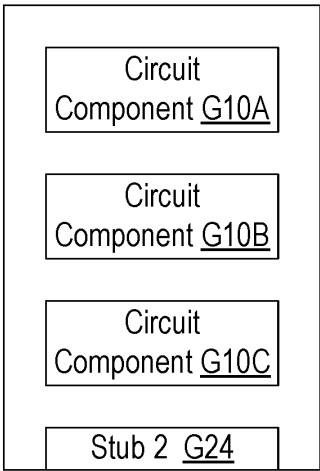


FIG. 71

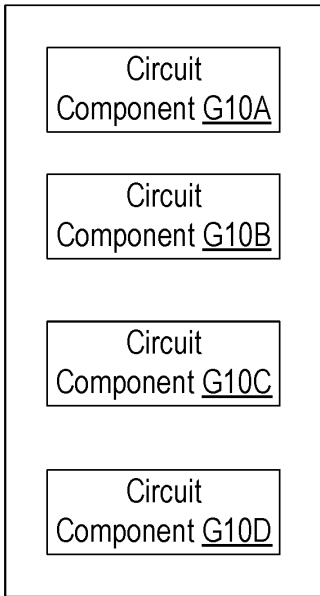


FIG. 72

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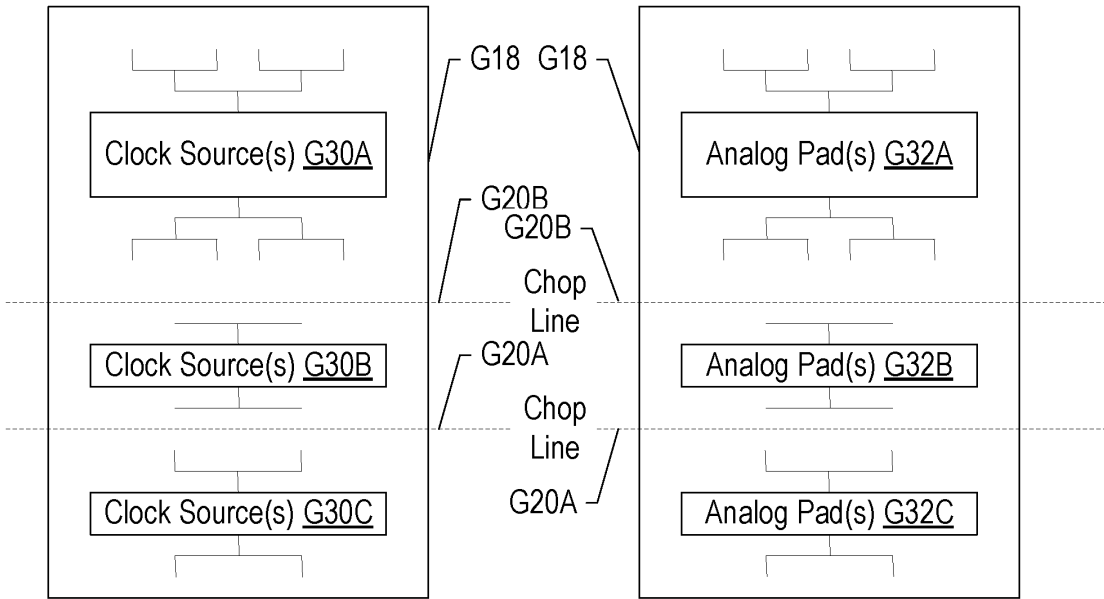


FIG. 73

FIG. 74

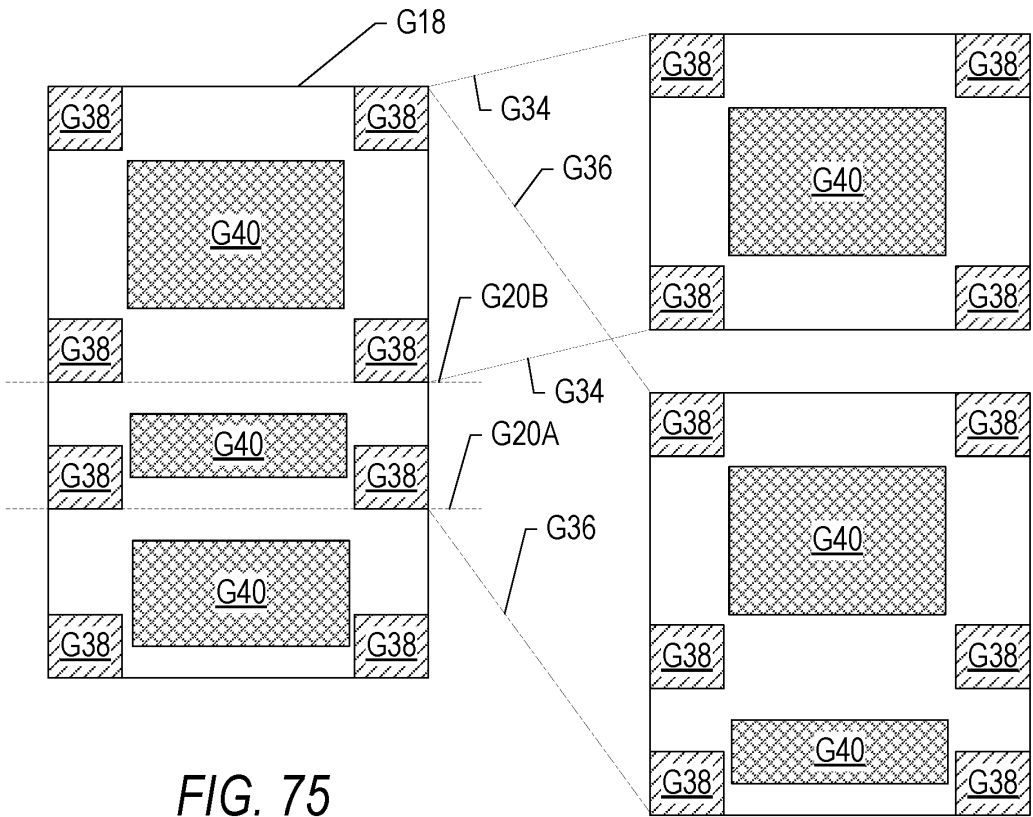


FIG. 75

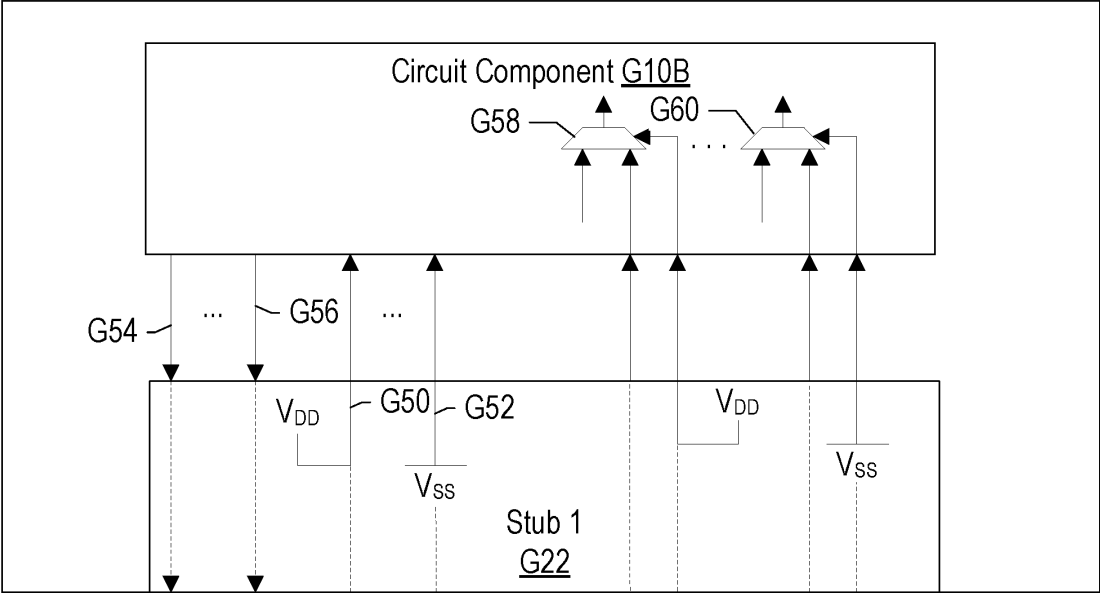


FIG. 76

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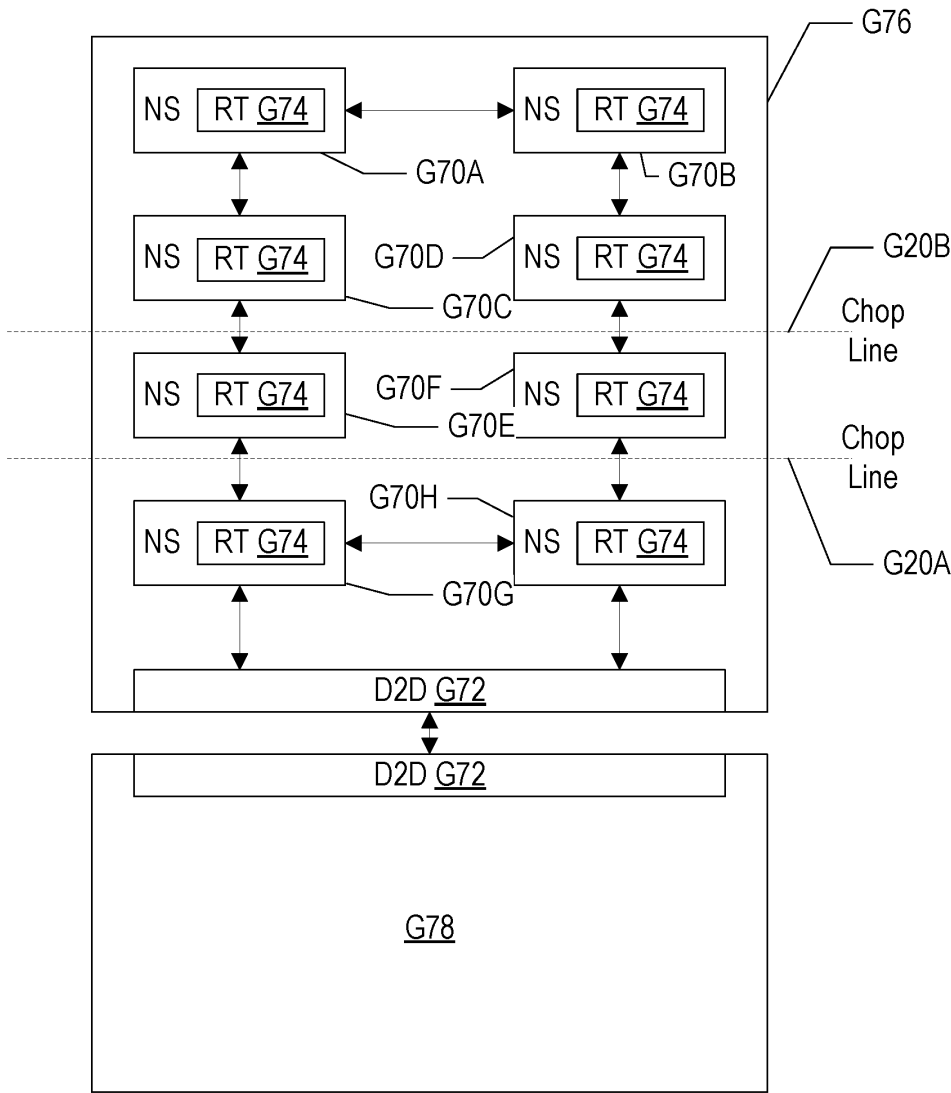


FIG. 77

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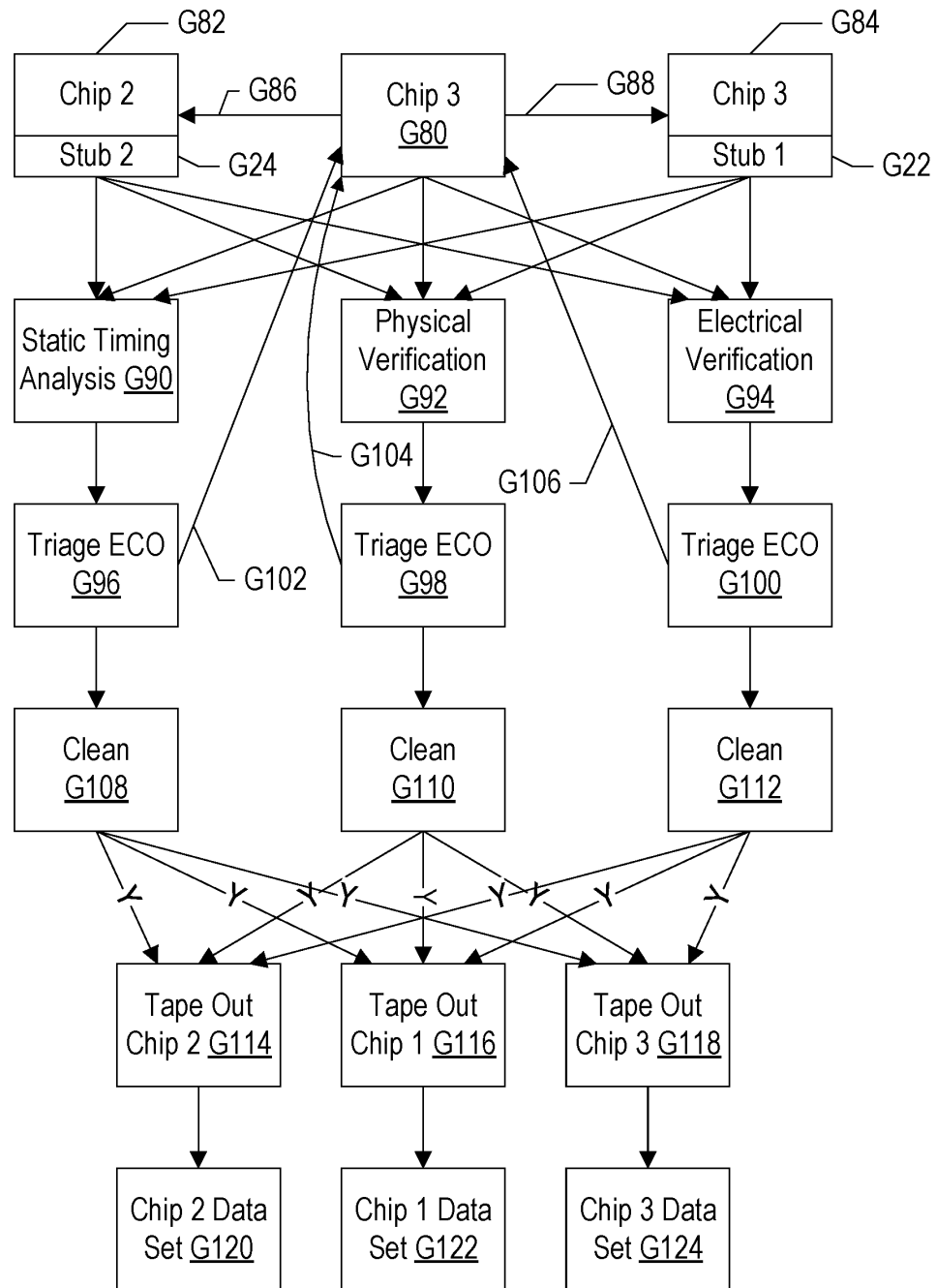


FIG. 78

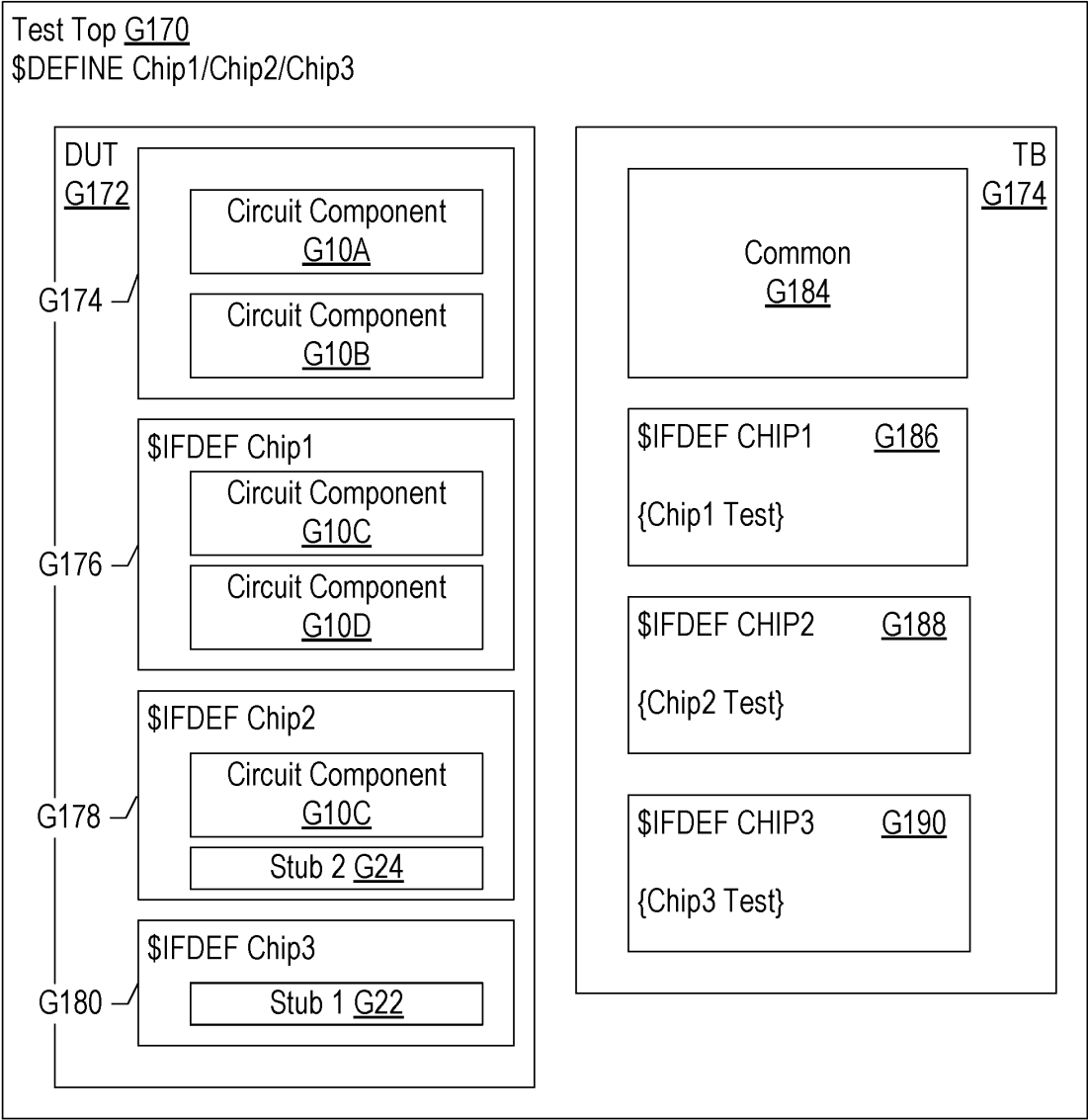


FIG. 79

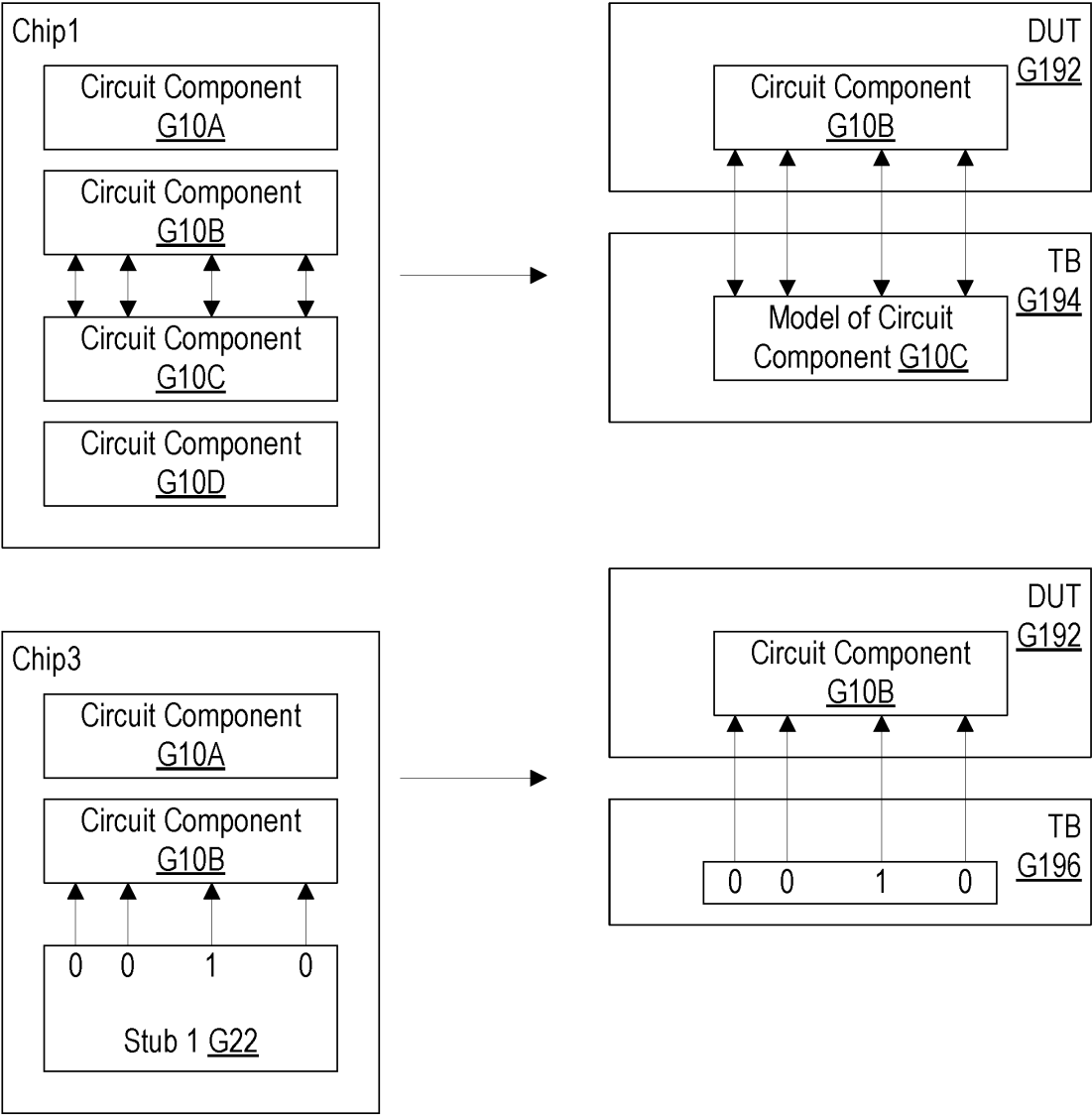


FIG. 80

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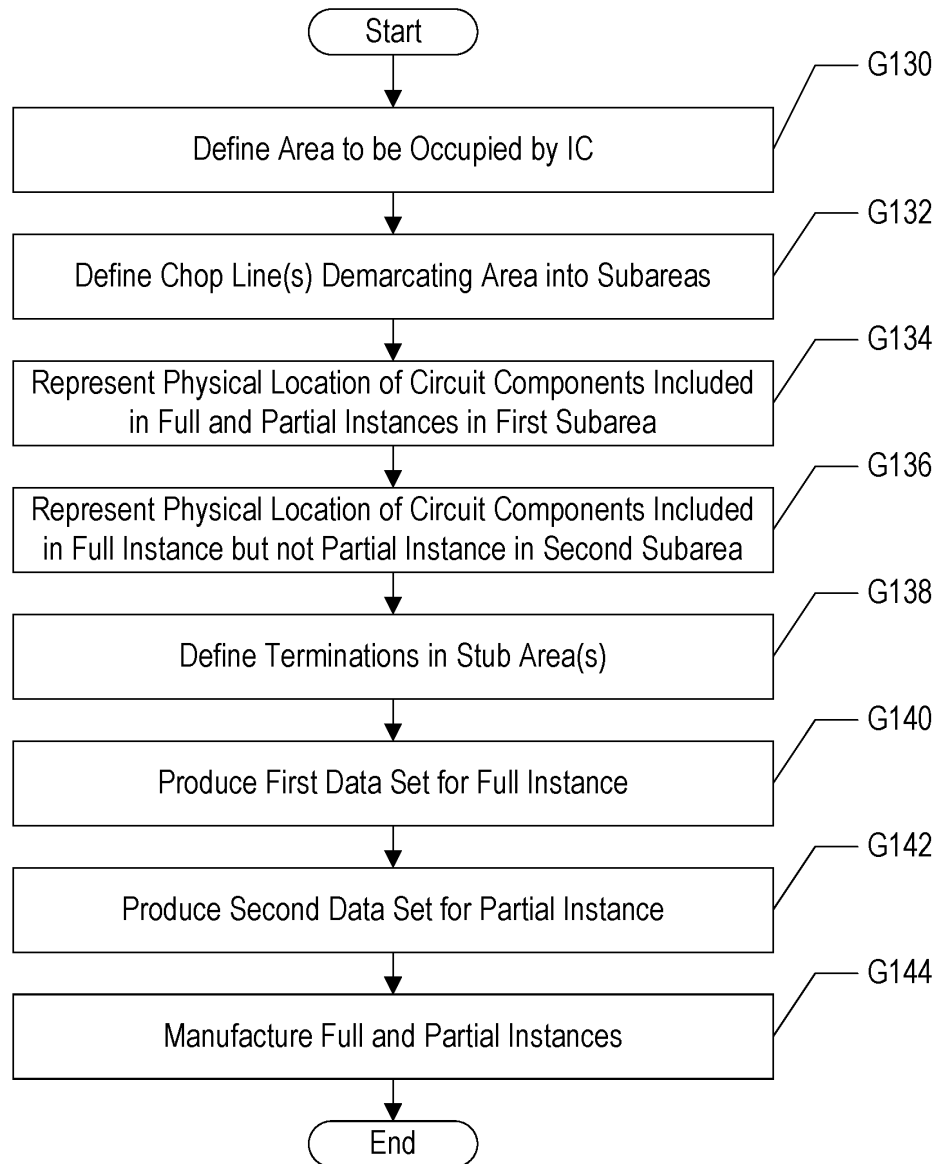


FIG. 81

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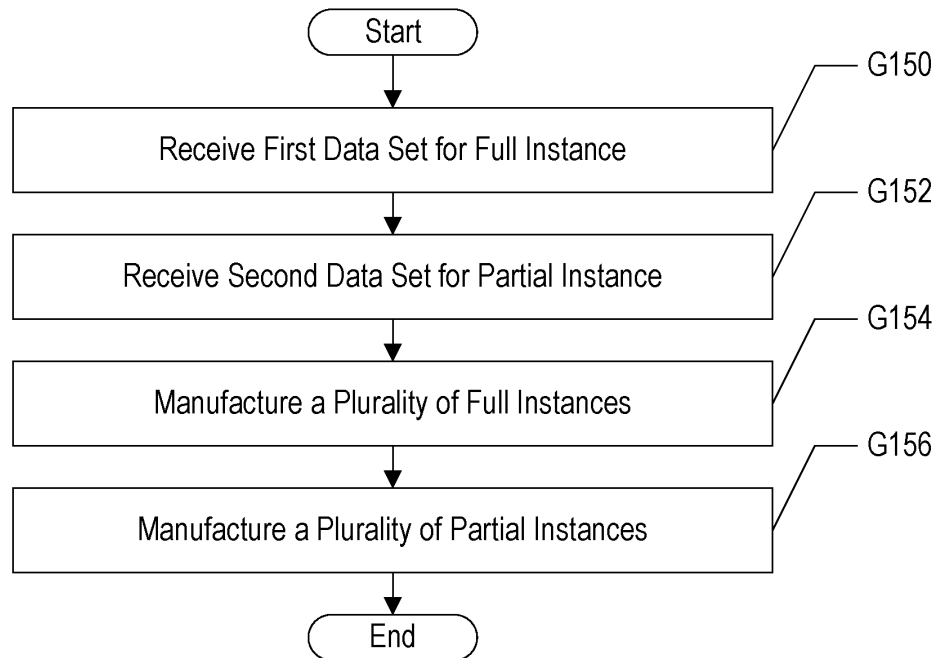


FIG. 82

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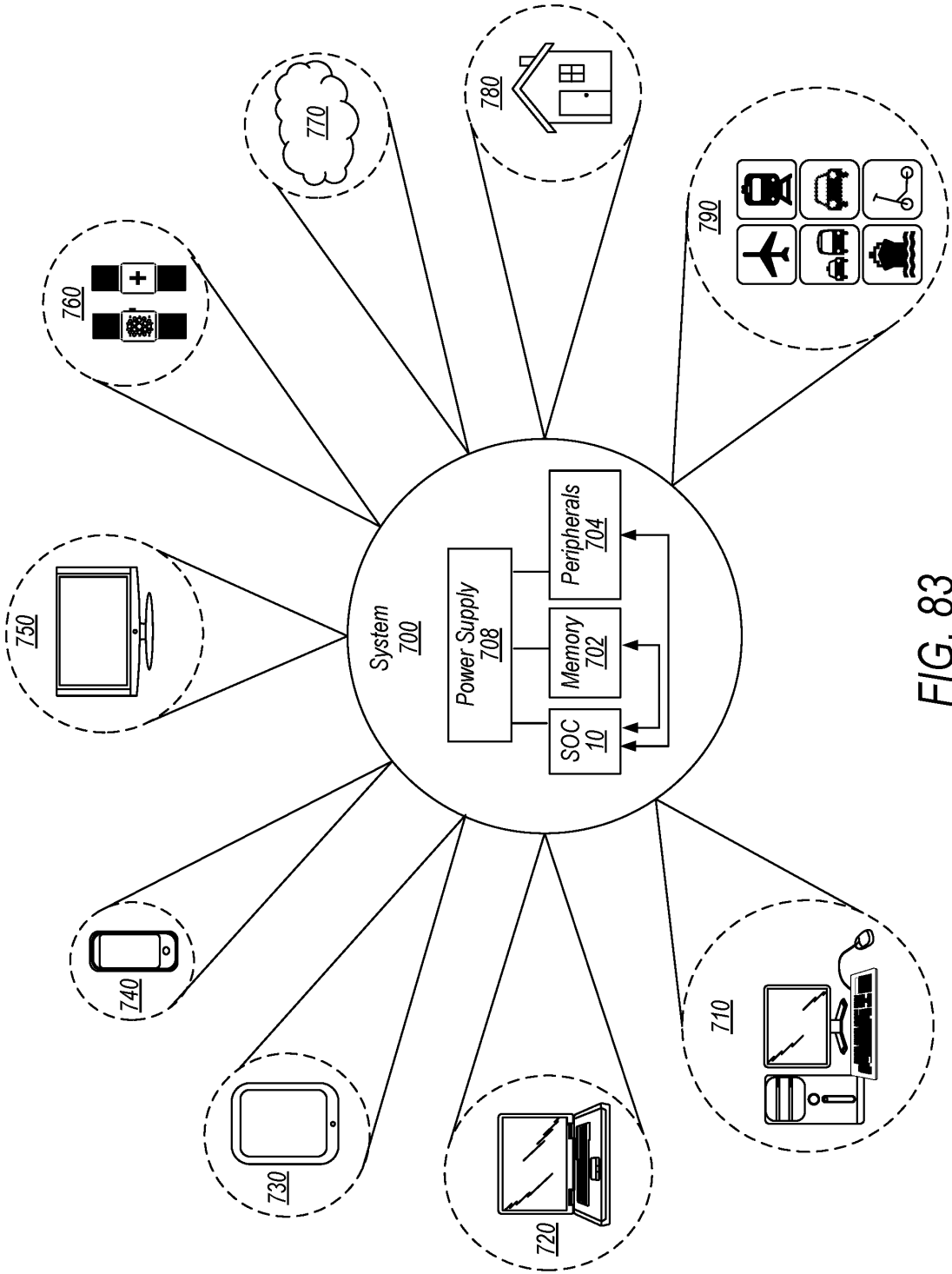


FIG. 83

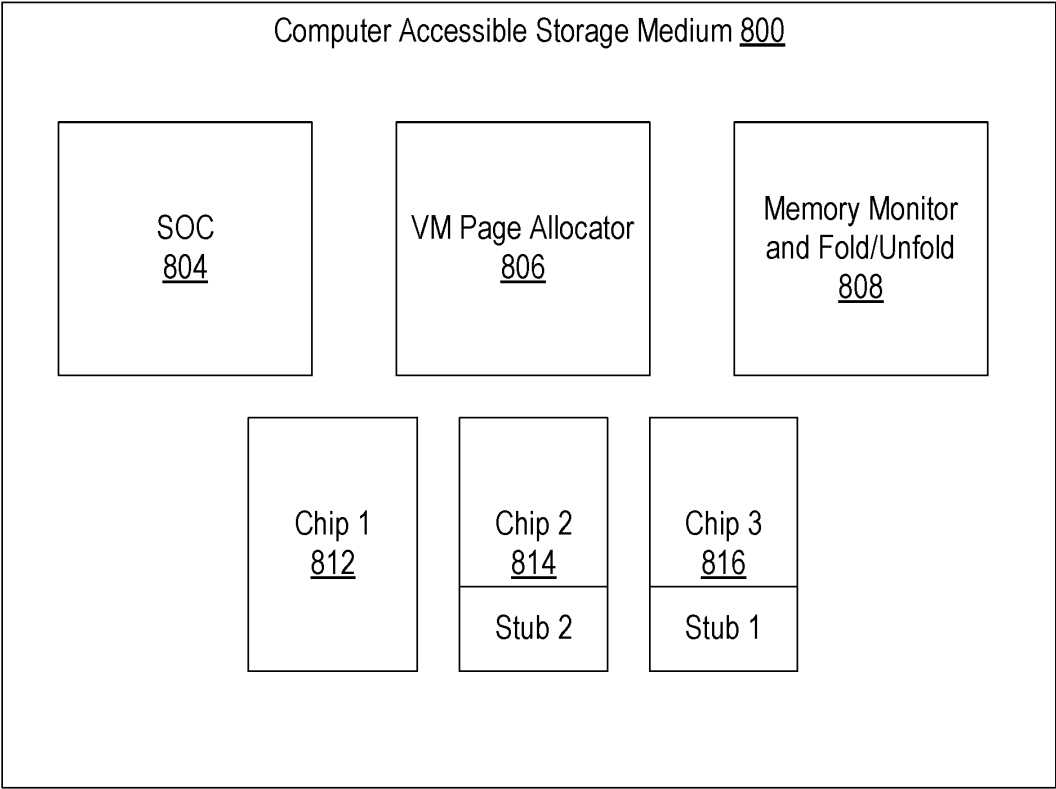


FIG. 84