METHOD OF PLASMA ETCHING LOW-K DIELECTRIC MATERIALS

Field of the Invention

The present invention relates to an improved method for plasma etching organosilicate glass in the fabrication of integrated circuits.

Background of the Invention

A common requirement in integrated circuit fabrication is the etching of openings such as contacts and vias in dielectric materials. The dielectric materials include doped silicon oxide such as fluorinated silicon oxide (FSG), undoped silicon oxide such as silicon dioxide, silicate glasses such as boron phosphate silicate glass (BPSG) and phosphate silicate glass (PSG), doped or undoped thermally grown silicon oxide, doped or undoped TEOS deposited silicon oxide, etc. The dielectric dopants include boron, phosphorus and/or arsenic. The dielectric can overlie a conductive or semiconductive layer such as polycrystalline silicon, metals such as aluminum, copper, titanium, tungsten, molybdenum or alloys thereof, nitrides such as titanium nitride, metal silicides such as titanium silicide, cobalt silicide, tungsten silicide, molydenum silicide, etc.

Various plasma etching techniques for etching openings in silicon oxide are disclosed in U.S. Patent Nos. 5,013,398; 5,013,400; 5,021,121; 5,022,958; 5,269,879; 5,529,657; 5,595,627; 5,611,888; and 5,780,338. The plasma etching can be carried out in medium density reactors such as the parallel plate plasma

reactor chambers described in the '398 patent or the triode type reactors described in the '400 patent or in high density reactors such as the inductive coupled reactors described in the '657 patent. Etching gas chemistries include the oxygen-free, Ar, CHF_3 and optional CF_4 gas mixture described in the '121 and '958 patents, the oxygen-free, fluorine-containing and nitrogen gas mixture described in the '879 patent, the C_4F_8 and CO gas mixture described in the '627 patent, the oxygen and CF_4 gas mixture described in the '400 patent, the oxygen, CF_4 and CH_4 gas mixture described in the '657 patent, and the Freon and neon gas mixture described in the '888 patent.

U.S. Patent No. 5,736,457 describes single and dual "damascene" metallization processes. In the "single damascene" approach, vias and conductors are formed in separate steps wherein a metallization pattern for either conductors or vias is etched into a dielectric layer, a metal layer is filled into the etched grooves or via holes in the dielectric layer, and the excess metal is removed by chemical mechanical planarization (CMP) or by an etch back process. In the "dual damascene" approach, the metallization patterns for the vias and conductors are etched in a dielectric layer and the etched grooves and via openings are filled with metal in a single metal filling and excess metal removal process.

Medium density plasma reactors operate at higher chamber pressures and dissociate etching gas chemistries to a lesser extent than high density plasma reactors. For instance, in medium density plasma reactors, etching gases such as

C_4F_8 dissociate in stages as follows: $C_4F_8 \rightarrow C_2F_8 \rightarrow CF_2 \rightarrow CF+F$. Due to such gradual dissociation, it is possible to achieve a high etch rate of a dielectric layer and a low etch rate of an overlying layer such as a photoresist or underlayer such as an etch stop layer. The ratio of such etch rates is referred to as the "etch selectivity ratio" and the high selectivity ratios obtainable in medium density plasma reactors promote complete etching of contacts, vias and conductor patterns. In contrast, in high density reactors, the instantaneous dissociation of etching gases can lead to low selectivity ratios due to the higher etch rates of the masking layer and etch stop layers. For example, in high density plasma reactors, C_4F_8 dissociates directly to free F and the high content of free F causes such rapid etching of the masking and/or etch stop layers that the etch selectivity ratio is unacceptably low.

A process of plasma etching silicon nitride from a multilayer structure is disclosed in European Patent Publication EP 908940 A2. According to this publication, an etchant gas comprising 4-20 volume % of a fluorocarbon gas, (i.e., CF_4, C_2F_6, C_3F_8), 10-30 volume % of a hydrogen source (i.e, CH_2F_2, CH_3F, H_2), and 40-70 volume % of a weak oxidant (i.e., CO, CO_2, O_2) is excited to form a high density plasma (i.e., above 10^{11} /cm ion density) and the plasma is used to etch a nitride layer located between a silicon substrate and an oxide or photoresist overlayer.

U.S. Patent No. 6,153,514 discloses a method of forming a self-aligned dual damascene structure which includes a lower conductive layer (e.g., copper or copper alloy), a first etch stop layer (e.g., silicon nitride), a first dielectric layer (e.g., low k dielectric material wherein $k<4$), a second etch stop layer (e.g., silicon nitride), a second dielectric layer (e.g., low k dielectric material), a hard mask layer (e.g., silicon nitride), and a photoresist layer patterned to provide the feature to be etched into the second dielectric layer. According to this patent, the nitride hard mask layer is etched with CHF_3/N_2, the second dielectric layer is etched with N_2/H_2O_2 or N_2/H_2, the second etch stop layer is etched with CHF_3/N_2 and the first dielectric layer is etched with $C_4F_8/Ar/O_2/CO$. U.S. Patent No. 5,611,888 discloses a method of plasma etching silicon nitride using a mixture of 10-20 sccm Freon 23 (CHF_3) and 70-110 sccm O_2.

U.S. patent No. 6,156,642 discloses a dual damascene structure wherein a semiconductor substrate includes a bottom metallization layer (e.g., copper), a topping layer (e.g., silicon nitride), a dielectric layer (e.g., silicon oxide or other low k material), a conformal layer (e.g., titanium, titanium nitride, tantalum, tantalum nitride, tungsten nitride) covering sidewalls of a trench and via hole, and a passivation layer (e.g., silicon nitride or silicon carbide). U.S. Patent No. 6,143,641 discloses a dual damascene structure in an integrated circuit structure which includes an intermetal dielectric material (e.g., SiO_2) on an underlying conductive material (e.g., aluminum or copper), an adhesion layer (e.g., Ti, TiN,

Ta) on exposed sidewalls of the dual damascene via structure which is filled with copper, a barrier metal or layer of silicon nitride, and additional layers including a low k dielectric material, silicon dioxide and silicon nitride.

U.S. Patent No. 6,090,304 discloses a method of plasma etching semiconductor substrates in a dual frequency plasma reactor wherein a first radiofrequency (RF) source is coupled to a top showerhead electrode through an RF matching network and a bottom electrode (on which a semiconductor wafer is supported) is coupled to a second RF source through a second matching network.

U.S. Patent No. 5,786,276 discloses a chemical downstream etching technique intended to be selective to silicon nitride over silicon oxide using a $CH_3F/CF_4/O_2$ recipe and a $CH_2F_2/CF_4/O_2$ recipe.

As device geometries become smaller and smaller, the need for high etch selectivity ratios is even greater in order to achieve plasma etching of deep and narrow openings in dielectric layers such as organosilicate glass. Accordingly, there is a need in the art for a plasma etching technique which provides high etch selectivity ratios and/or which achieves deep and narrow openings. Further, it would be highly desirable to achieve such opening geometries without bowing of the sidewalls of the openings.

Summary of the Invention

The invention provides a process for plasma etching a organosilicate glass layer with selectivity to an overlying and/or underlying dielectric layer, comprising the steps of introducing the semiconductor substrate into a plasma etching chamber, supplying an oxygen-free etching gas to the chamber and energizing the etching gas into a plasma state, and etching openings in the organosilicate glass layer by contacting exposed portions of the organosilicate glass layer with the plasma. The etching gas includes at least one nitrogen reactant, at least one fluorocarbon reactant, and an optional inert carrier gas, the fluorocarbon reactant and nitrogen reactant being supplied to the chamber at flow rates such that the fluorocarbon reactant flow rate is less than the nitrogen reactant flow rate.

According to one aspect of the invention, the underlying and/or overlying dielectric layer comprises a doped or undoped oxide film a silicon nitride film, a silicon carbide film, or combination thereof. The openings can comprise grooves corresponding to a conductor pattern, via openings or contact openings. The openings can be etched in the underlying and/or overlying dielectric layers so as to have an aspect ratio of at least 3:1. The etching gas can include a hydrogen-containing and/or a hydrogen-free fluorocarbon reactant represented by $C_xF_yH_z$ wherein x is at least 1, y is at least 1 and z is equal to or greater than 0. For example, the fluorocarbon reactant can be selected from the group of C_4F_8, C_5F_8,

C_4F_6 and/or CH_2F_2. The semiconductor substrate can include an electrically conductive or semiconductive layer such as a metal-containing layer selected from the group consisting of Al, Al alloys, Cu, Cu alloys, Ti, Ti alloys, doped or undoped polycrystalline or single crystal silicon, TiN, TiW, Mo, silicides of Ti, W, Co and/or Mo or alloys thereof, etc.

The process of the invention can etch openings which are 0.30μm, especially 0.25μm or smaller sized openings using a fluorocarbon reactant which comprises $C_xF_yH_z$ wherein x is 1 to 5, y is 1 to 8 and z is 0 to 3. As an example, the fluorocarbon reactant can comprise a hydrogen-free fluorocarbon represented by C_nF_m wherein n is 4 or more and m is 6 or more and an optional hydrogen-containing fluorocarbon reactant represented by $C_xF_yH_z$ wherein x is 1 or more, y is 1 or more and z is at least 1. The optional carrier gas can be selected from the group consisting of Ar, He, Ne, Kr, Xe or mixtures thereof. In a single wafer plasma etch chamber for processing 200 mm wafers, the fluorocarbon gas flow rate can be 2.5 to 15% of the nitrogen gas flow rate. For example, the fluorocarbon reactant can be supplied at a flow rate of 3 to 30 sccm, the nitrogen reactant can be supplied to the plasma reactor at a flow rate of 50 to 300 sccm, the fluorocarbon reactant can be supplied to the plasma reactor at a flow rate of 15 to 100 sccm, and the optional carrier gas can be supplied to the plasma reactor at a flow rate of 10 to 500 sccm. As an example, C_5F_8, N_2 and Ar can be supplied at flow rates of 10 to 25 sccm, 50 to 300 sccm, and 50 to 300 sccm. In another

example, C_4F_8, CF_2H_2, N_2 and Ar can be supplied at flow rates of 2 to 20 sccm, 2 to 30 sccm, 50 to 300 sccm, and 50 to 300 sccm. During the etching step, the plasma reactor is preferably maintained at a vacuum pressure of 5 to 500 mTorr, preferably 150 to 250 mTorr in the case of a medium density plasma reactor. The etching step can be followed by additional etching steps and subsequent filling of the openings with metal. The method of the invention can also include steps of forming a photoresist layer on the substrate, patterning the photoresist layer to form a plurality of openings followed by etching a metallization pattern of conductor lines, via or contact openings in the overlying oxide layer.

Brief Description of the Drawings

Figures 1a-d show schematic representations of a via-first dual-damascene structure which can be etched according to the process of the invention, Figure 1a showing a pre-etch condition, Figure 1b showing a post-etch condition in which a via has been etched, Figure 1c showing the structure re-patterned for a trench etch and Figure 1d showing a post-etch condition in which the trench has been etched;

Figures 2a-d show schematic representations of a trench-first dual-damascene structure which can be etched according to the process of the invention, Figure 2a showing a pre-etch condition, Figure 2b showing a post-etch condition in which a trench has been etched, Figure 2c showing the structure re-

patterned for a via etch and Figure 2d showing a post-etch condition in which the via has been etched;

Figures 3a-b show schematic representations of a self-aligned dual-damascene structure which can be etched according to the process of the invention, Figure 3a showing a pre-etch condition and Figure 3b showing a post-etch condition in which a trench and a via have been etched;

Figure 4 shows a schematic representation of an inductively coupled high density plasma reactor which can be used to carry out the process of the invention; and

Figure 5 shows a schematic representation of a medium density parallel plate plasma reactor which can be used to carry out the process of the invention.

Detailed Description of the Invention

The invention provides a semiconductor manufacturing process wherein openings can be plasma etched in organosilicate glass layers while providing desired selectivity to underlying and/or overlying oxide layers such as silicon dioxide, silicon nitride, silicon carbide and photoresist materials. Such selectivity is of great interest in the manufacture of damascene structures wherein one or more organosilicate glass layers are incorporated in a multilayer structure. During manufacture of such structures, features such as contacts, vias, conductor lines, etc. are etched in dielectric materials such as oxide and organosilicate glass layers

in the manufacture of integrated circuits. The invention overcomes a problem with prior etching techniques wherein the selectivity between the organosilicate glass etch rate and the underlying and/or overlying dielectric/photoresist layers was too low for commercial applications. Such selectivity problems are solved by utilizing an etching gas chemistry which reduces the etch rates of the dielectric/photoresist layers.

According to one aspect of the invention, a single or dual-damascene etch process is provided wherein organosilicate glass can be etched with 0.25 μm or smaller geometry to an etch depth of at least 1.8 μm with an organosilicate glass:photoresist etch selectivity of greater than 5:1. The process can provide a low or reversed RIE lag, which can allow multi-level dielectric etch applications and enable the fabrication of dual-damascene devices.

Figures 1 a-d show schematics of how a via-first dual-damascene structure can be etched in accordance with the invention. Figure 1a shows a pre-etch condition wherein an opening 10 corresponding to a via is provided in a photoresist masking layer 12 which overlies a stack of a first dielectric layer 14 such as silicon oxide, a first stop layer 16 such as silicon nitride, a second dielectric layer 18 such as silicon oxide, a second stop layer 20 such as silicon nitride, and a substrate 22 such as a silicon wafer. Figure 1b shows the structure after etching wherein the opening 10 extends through the dielectric layers 14, 18 and first stop layer 16 to the second stop layer 20. Figure 1c shows the structure

after re-patterning the masking layer for a trench 24. Figure 1d shows the structure after etching wherein the first dielectric layer 14 is etched down to the first stop layer 16.

Figures 2 a-d show schematics of how a trench-first dual-damascene structure can be etched in accordance with the invention. Figure 2a shows a pre-etch condition wherein an opening 30 corresponding to a trench is provided in a photoresist masking layer 32 which overlies a stack of a first dielectric layer 34 such as silicon oxide, a first stop layer 36 such as silicon nitride, a second dielectric layer 38 such as silicon oxide, a second stop layer 40 such as silicon nitride, and a substrate 42 such as a silicon wafer. Figure 2b shows the structure after etching wherein the opening 30 extends through the dielectric layer 34 to the first stop layer 36. Figure 2c shows the structure after re-patterning the masking layer for a via 44. Figure 2d shows the structure after etching wherein the second dielectric layer 38 is etched down to the second stop layer 40.

Figures 3 a-b show schematics of how a dual-damascene structure can be etched in a single step in accordance with the invention. Figure 3a shows a pre-etch condition wherein an opening 50 corresponding to a trench is provided in a photoresist masking layer 52 which overlies a stack of a first dielectric layer 54 such as silicon oxide, a first stop layer 56 such as silicon nitride, a second dielectric layer 58 such as silicon oxide, a second stop layer 60 such as silicon nitride, and a substrate 62 such as a silicon wafer. In order to obtain etching of

vias through the first stop layer 56 in a single etching step, first stop layer 56 includes an opening 64. Figure 2b shows the structure after etching wherein the opening 50 extends through the dielectric layer 54 to the first stop layer 56 and the opening 64 extends through the second dielectric 58 to the second stop layer 60. Such an arrangement can be referred to as a "self-aligned dual-damascene" structure.

The process of the invention is applicable to etching of various dielectric layers such as doped silicon oxide such as fluorinated silicon oxide (FSG), undoped silicon oxide such as silicon dioxide, spin-on-glass (SOG), silicate glasses such as boron phosphate silicate glass (BPSG) and phosphate silicate glass (PSG), doped or undoped thermally grown silicon oxide, doped or undoped TEOS deposited silicon oxide, low-k dielectrics including organic polymer materials, etc. The dielectric dopants include boron, phosphorus and/or arsenic. The dielectric can overlie a conductive or semiconductive layer such as polycrystalline silicon, metals such as aluminum, copper, titanium, tungsten, molybdenum or alloys thereof, nitrides such as titanium nitride, metal silicides such as titanium silicide, cobalt silicide, tungsten silicide, molydenum silicide, etc.

The plasma can be produced in various types of plasma reactors. Such plasma reactors typically have energy sources which use RF energy, microwave energy, magnetic fields, etc. to produce a medium to high density plasma. For instance, a high density plasma could be produced in a transformer coupled plasma

(TCP™) available from LAM Research Corporation which is also called inductively coupled plasma reactor, an electron-cyclotron resonance (ECR) plasma reactor, a helicon plasma reactor, or the like. An example of a high flow plasma reactor which can provide a high density plasma is disclosed in commonly owned U.S. Patent No. 5,820,261, the disclosure of which is hereby incorporated by reference. The plasma can also be produced in a parallel plate etch reactor such as the dual frequency plasma etch reactor described in commonly owned U.S. Patent No. 6,090,304, the disclosure of which is hereby incorporated by reference.

The process of the invention can be carried out in an inductively coupled plasma reactor such as reactor 100 shown in Figure 4. The reactor 100 includes an interior 102 maintained at a desired vacuum pressure by a vacuum pump connected to an outlet 104 in a lower wall of the reactor. Etching gas can be supplied to a showerhead arrangement be supplying gas from gas supply 106 to a plenum 108 extending around the underside of a dielectric window 110. A high density plasma can be generated in the reactor by supplying RF energy from an RF source 112 to an external RF antenna 114 such as a planar spiral coil having one or more turns outside the dielectric window 110 on top of the reactor. The plasma generating source can be part of a modular mounting arrangement removably mounted in a vacuum tight manner on the upper end of the reactor.

A semiconductor substrate 116 such as a wafer is supported within the reactor on a substrate support 118 such as a cantilever chuck arrangement

removably supported by a modular mounting arrangement from a sidewall of the reactor. The substrate support 118 is at one end of a support arm mounted in a cantilever fashion such that the entire substrate support/support arm assembly can be removed from the reactor by passing the assembly through an opening in the sidewall of the reactor. The substrate support 118 can include a chucking apparatus such as an electrostatic chuck 120 and the substrate can be surrounded by a dielectric focus ring 122. The chuck can include an RF biasing electrode for applying an RF bias to the substrate during an etching process. The etching gas supplied by gas supply 106 can flow through channels between the window 110 and an underlying gas distribution plate 124 and enter the interior 102 through gas outlets in the plate 124. The reactor can also include a heated liner 126 extending conically from the plate 124 .

The process of the invention can also be carried out in a parallel plate plasma reactor such as reactor 200 shown in Figure 5. The reactor 200 includes an interior 202 maintained at a desired vacuum pressure by a vacuum pump connected to an outlet 204 in a wall of the reactor. Etching gas can be supplied to a showerhead electrode by supplying gas from gas supply 206. A medium density plasma can be generated in the reactor by supplying RF energy from RF sources 212 to the showerhead electrode and a bottom electrode or the showerhead electrode can be electrically grounded and RF energy at two different frequencies can be supplied to the bottom electrode.

In one embodiment, the invention provides a process for plasma etching 0.3 μm and smaller high aspect ratio features such as conductor lines, vias and contacts including self aligned contacts (SAC) in dielectric layers on semiconductor substrates. In the process, a gas mixture containing fluorocarbon, oxygen and optional gases such as a carrier gas (e.g., argon) is energized in a plasma etch reactor into a plasma state such that the fluorocarbon and the oxygen reactant are at least partially dissociated. During the etching process, the dielectric layer is etched by the fluorine and the carbon reacts with some free F to thereby reduce the etch rate of the masking and/or stop etch layers. The oxygen is effective in providing a desired level of selectivity between the etch rates of the dielectric material being etched and an underlayer such as silicon nitride and/or an overlayer such as a photoresist while at the same time balancing polymer build-up sufficiently to protect sidewalls of etched features while avoiding pinch-off and etch stop problems due to excessive polymer build-up. Etch stop is especially problematic during plasma etching of deep and narrow openings in dielectric materials such as silicon oxide using gas chemistries which form too much polymer, i.e., polymer-build-up in the opening prevents further etching of the silicon oxide. In the process of the invention, the polymer build-up can be reduced by the synergistic effect of breaking up the polymer with the oxygen in the etching gas mixture. Further, in order to preserve the critical dimension(CD) of the etched feature, the oxygen removes enough of

the polymer build-up on the sidewalls of the etched openings to avoid excessive build-up of polymer on the sidewalls which otherwise could cause "pinch-off" of the etched openings and thus prevent complete etching of the opening to the desired depth.

According to the invention, oxygen is added in an amount effective to control the etch rate selectivity ratio of the etching gas chemistry. That is, when using an etching gas containing oxygen and one or more fluorocarbon gases, the oxygen is effective to scavenge free F dissociated from the fluorocarbon in the plasma. Such free F attacks layers such as the masking and etch stop layers resulting in low etch rate selectivity. However, by supplying oxygen at a suitable level it is possible to scavenge a sufficient amount of the free F to thereby increase the selectivity ratio. The oxygen is preferably supplied to the plasma etching reactor in amounts effective to scavenge free F and prevent etch stop by reacting with polymer at the bottom of the etched openings. For a medium density plasma reactor, the advantageous effects of the invention can be achieved by supplying the oxygen reactant and fluorocarbon reactant to the plasma etching reactor at a flow rate ratio of oxygen reactant to fluorocarbon reactant of 1.5 or less.

The etching gas mixture may optionally include other gases such as nitrogen and/or an inert carrier gas. Argon is an especially useful inert carrier gas which aids fluorine in attacking dielectric materials such as silicon oxide. However, other inert gases such as He, Ne, Kr and/or Xe can be used as the inert

carrier gas. In order to maintain low pressure in the plasma etching reactor, the amount of carrier gas introduced into the reactor can be at low flow rates. For instance, for a medium to high density plasma reactor, argon can be supplied into the reactor in amounts of 25 to 300 sccm. The carrier gas preferably aids the dielectric etch rate, e.g., the oxide etching rate can be increased due to sputtering of the oxide.

The fluorocarbon preferably comprises $C_xF_yH_z$ wherein x is at least 1, y is at least 1 and z is 0 or above, e.g., CF_4, C_3F_6, C_3F_8, C_5F_8, C_4F_8, C_2F_6, CH_2F_5, C_2HF_5, CH_3F, CH_2F_2, etc. Although hydrogen containing fluorocarbons are quite polymerizing, the degree of polymerizing can be controlled to achieve deep and narrow openings through the use of a synergistic combination of the oxygen reactant and the fluorocarbon reactant. The amount of fluorocarbon gas to be supplied to the plasma reactor should be sufficient to achieve the desired degree of polymerizing. As an example, oxygen and fluorocarbon reactants can each be supplied at flow rates of 5 to 100 sccm, preferably 15 to 50 sccm, and more preferably 20 to 40 sccm. As an example, for 0.25 μm diameter contact openings, the oxygen reactant flow rate can range from 10 to 50 sccm when $C_xF_yH_z$ is supplied at 10 to 50 sccm, and argon, if supplied, can range from 50 to 500 sccm. It will be apparent to those skilled in the art that the flow rates of the various gases will depend on factors such as the type of plasma reactor, the power settings, the vacuum pressure in the reactor, the dissociation rate for the plasma source, etc.

The process of the invention is useful for obtaining extremely high aspect ratios of at least 5:1, the process being especially useful for obtaining aspect ratios up to 10:1 for openings smaller than 0.3 μm, preferably as small as 0.18 and below. For example, it is possible to obtain substantially straight walls for 0.25 μm diameter openings at depths greater than 2.1 μm. In order to provide anisotropic etching, it is beneficial to supply an RF bias to the semiconductor substrate by the substrate support. For instance, an RF biasing electrode in the substrate support can be supplied with power on the order of 50 to 1000 Watts to adequately RF bias 6, 8 or even 12 inch wafers.

The reactor pressure is preferably maintained at a level suitable for sustaining a plasma in the reactor. In general, too low a reactor pressure can lead to plasma extinguishment whereas in a high density etch reactor too high a reactor pressure can lead to the etch stop problem. For high density plasma reactors, the reactor is preferably at a pressure below 30 mTorr, more preferably below 10 mTorr. For medium density plasma reactors, the reactor is preferably at a pressure above 30 mTorr, more preferably above 80 mTorr. Due to plasma confinement at the semiconductor substrate undergoing etching, the vacuum pressure at the substrate surface may be higher than the vacuum pressure setting for the reactor.

The substrate support supporting the semiconductor substrate undergoing etching preferably cools the substrate enough to prevent burning of any photoresist

on the substrate, e.g., maintain the substrate below 140° C. In high and medium density plasma reactors, it is sufficient to cool the substrate support to a temperature of -20 to 40° C. The substrate support can include a bottom electrode for supplying an RF bias to the substrate during processing thereof and an ESC for clamping the substrate. For example, the substrate can comprise a silicon wafer which is electrostatically clamped and cooled by supplying helium at a desired pressure between the wafer and top surface of the ESC. In order to maintain the wafer at a desired temperature of, for example, 0 to 100° C, the He can be maintained at a pressure of 10 to 30 Torr in the space between the wafer and the chuck.

The process of the invention is especially well suited for etching deep and narrow openings through silicon oxide to an underlying conductive or semiconductive layer. This layer can be a metal such as Al, Ti, Cu, Mo or alloys thereof, a metal nitride such as titanium nitride, doped or undoped polycrystalline or single crystal silicon, a metal silicide such as titanium silicide, tungsten silicide, cobalt silicide, molybdenum silicide, etc. In the case where the oxygen reactant is pure oxygen, the underlying conductive material need not exclude materials which are attached by oxygen such as silicon nitride because the oxygen reactant is supplied to the reactor at a rate relative to the fluorocarbon reactant to avoid excessive attack of silicon nitride.

The following Table 1 sets forth results of etching a silicon nitride layer using a dual frequency plasma etch reactor wherein the reactor conditions were set as follows: 200 mTorr reactor pressure, 500 watts 27 MHZ and 100 watts 2 MHZ power, 20 to 40 °C electrode temperatures, 60 second etch time, with variations in etch gas chemistry as listed in the table. Etch rates of the nitride and oxide layers were calculated from 9-points/wafer Rudolph (Ellipsometry) measurements.

TABLE 1

Run	CH_3F (sccm)	CHF_3 (sccm)	O_2 (sccm)	Ar/N_2 (sccm)	Nitride (A/min)	Oxide (A/min)	Oxide:Nitride Selectivity
1	40	30	10	200/200	624	910	0.69
2	0	60	50	0/200	1668	825	2.02
3	0	60	10	0/0	1058	1488	0.71
4	5	60	50	200/0	2300	991	2.32
5	0	60	10	200/200	1027	923	1.11
6	40	30	10	0/0	dep.	Dep.	NA
7	40	30	50	200/0	1160	283	4.10
8	40	60	10	0/200	dep.	dep.	NA
9	0	30	10	200/0	1421	728	1.95
10	20	45	30	100/100	984	1418	0.69
11	0	30	50	0/0	1839	1049	1.75
12	40	60	50	0/0	902	489	1.84
13	20	45	30	100/100	985	1434	0.69
14	0	30	50	200/200	458	585	0.78
15	40	60	10	200/0	dep.	Dep.	NA
16	0	30	10	0/200	833	444	1.88

17	40	30	50	0/200	1026	1158	0.89
18	40	60	50	200/200	1082	1519	0.71
19	0	60	50	200/200	922	813	1.13
20	0	60	50	450/0	1648	939	1.76
21	40	0	50	200/0	1215	28	43.4
22	40	0	50	200/0	1225	29	42.2
23	20	0	25	200/0	756	18	42.0
24	20	0	15	200/0	851	88	9.67
25	25	0	20	200/0	865	50	15.12

"dep." indicates that the process resulted in deposition

Table 2 sets forth results of etching a silicon wafer having successive layers of 5200 Å photoresist masking layer, 600 Å ARC, 1500 Å oxide, 400 Å nitride, 7000 Å SilK, and 400 Å nitride using a dual frequency plasma etch reactor wherein the reactor conditions were set as follows: 150 mTorr reactor pressure, 500 watts 27 MHZ and 100 watts 2 MHZ power, 20 to 40 °C electrode temperatures, 60 second etch time with variations in etch gas chemistry as follows: 150 mTorr, 200 sccm Ar, 25 sccm O_2, 20 sccm CH_3F in Run 1, 150 mTorr, 200 sccm Ar, 13 sccm O_2, 20 sccm CH_3F in Run 2, 150 mTorr, 200 sccm Ar, 20 sccm O_2, 25 CH_3F in Run 3; 150 mTorr, 200 sccm Ar, 20 O_2, 25 CH_3F, 5 sccm CHF_3, 5 sccm CHF_3 in Run 4, and 200 sccm Ar, 20 O_2, 25 CH_3F in Run 5.

TABLE 2

Run	O_2/CH_3F flow ratio	Nitride (A/min)	Oxide ER (A/min)	PR E/R (A/min)	Silk ER (A/min)	Nitride to Oxide Sel
1	1.25	756	18	3194	2374	42
2	0.65	~1000	~100	1681	1308	~10
3	0.8	1149	34			33.8
4	0.8	1579	155			10.2
5	0.8	851	45			7.6

During processing of a semiconductor wafer it may be desired to carry one or more of the following steps: ARC/Via Mask (Nitride) etch wherein it is desired to maintain the critical dimension (CD)while using a thin photoresist and remove any oxide, a SilK Via Etch wherein it is desired to leave 1000 Å SilK, a Through Mask Etch (nitride) wherein openings are etched into the nitride with selectivity to oxide layers, a second SilK Etch wherein it is desired to maintain CD with a smooth front and with minimal faceting, and a Nitride Finish Etch wherein the etch is selective to oxide, SilK and copper.

The foregoing has described the principles, preferred embodiments and modes of operation of the present invention. However, the invention should not be construed as being limited to the particular embodiments discussed. Thus, the above-described embodiments should be regarded as illustrative rather than restrictive, and it should be appreciated that variations may be made in those

embodiments by workers skilled in the art without departing from the scope of the present invention as defined by the following claims.

WHAT IS CLAIMED IS:

1. A process for etching an organosilicate layer with selectivity to an underlying and/or overlying dielectric layer, comprising the steps of:

introducing a semiconductor substrate into a plasma etching chamber, the semiconductor substrate having an organosilicate layer and an underlying and/or overlying dielectric layer;

supplying an oxygen-free etching gas to the plasma etching chamber and energizing the etching gas into a plasma state, the etching gas comprising at least one nitrogen reactant, at least one fluorocarbon reactant and optional carrier gas, the fluorocarbon reactant and nitrogen reactant being supplied to the chamber at a flow rates such that the fluorocarbon reactant flow rate is less than the nitrogen reactant flow rate;

contacting exposed portions of the organosilicate layer with the plasma so as to etch openings in the organosilicate layer with the plasma while providing a selectivity etching ratio of the etching rate of the organosilicate layer to the etching rate of the dielectric layer of at least about 5.

2. The process of claim 1, wherein the dielectric layer comprises a doped or undoped silicon oxide film, a silicon nitride film, a silicon carbide film or combination thereof. .

3. The process of claim 1, wherein the at least one fluorocarbon reactant is represented by $C_xF_yH_z$ wherein x is at least 1, y is at least 1 and z is equal to or greater than 0.

4. The process of claim 1, wherein the openings are etched to a depth sufficient to provide an aspect ratio of at least 3:1.

5. The process of claim 1, wherein the at least one fluorocarbon reactant comprises C_5F_8, C_4F_8, C_4F_6, CF_2H_2, and mixtures thereof.

6. The process of claim 1, wherein the organosilicate layer overlies an electrically conductive or semiconductive layer comprising a metal-containing layer selected from the group consisting of doped and undoped polycrystalline or single crystal silicon, aluminum or alloy thereof, copper or alloy thereof, titanium or alloy thereof, tungsten or alloy thereof , molybdenum or alloy thereof, titanium nitride, titanium silicide, tungsten silicide, cobalt silicide, and molybdenum silicide.

7. The process of claim 1, wherein the openings are 0.25 micron or smaller sized openings.

8. The process of claim 1, wherein the at least one fluorocarbon reactant consists essentially of a hydrogen-free fluorocarbon represented by C_nF_m wherein n is 4 or more and m is 6 or more and an optional hydrogen-containing fluorocarbon reactant represented by $C_xF_yH_z$ wherein x is 1 or more, y is 1 or more and z is at least 2.

9. The process of clam 1, wherein the etching gas includes a carrier gas selected from the group consisting of Ar, He, Ne, Kr, Xe or mixtures thereof.

10. The process of clam 1, wherein the plasma reactor comprises a dual frequency parallel plate plasma reactor having a showerhead electrode and a bottom electrode on which the substrate is supported, the bottom electrode being supplied RF energy at two different frequencies or the showerhead electrode being supplied RF energy at a first frequency and the bottom electrode being supplied RF energy at a second frequency which is greater than the first frequency.

11. The process of claim 1, wherein the flow rate ratio of the fluorocarbon reactant to the nitrogen reactant is 25% or less.

12. The process of claim 1, wherein the fluorocarbon reactant is supplied to the plasma reactor at a flow rate of 3 to 30 sccm and the nitrogen reactant is supplied to the plasma reactor at a flow rate of 50 to 300 sccm.

13. The process of claim 1, further comprising applying an RF bias to the semiconductor substrate during the etching step.

14. The process of claim 1, further comprising filling the openings with metal after the etching step.

15. The process of claim 1, wherein the etching step is carried out as part of a process of manufacturing a damascene structure.

16. The process of claim 1, further comprising steps of forming a photoresist layer as a masking layer, patterning the photoresist layer to form a plurality of the openings and the etching step forms via or contact openings in the organosilicate layer.

17. The process of claim 1, wherein the openings are formed with an aspect ratio of at least 5:1.

18. The process of claim 1, wherein the etching gas consists essentially of C_5F_8, N_2 and Ar or C_4F_8, CF_2H_2, N_2 and Ar.

19. The process of claim 1, wherein the plasma reactor is at a pressure of 50 to 500 mTorr during the etching step.

20. The process of claim 1, wherein the semiconductor substrate comprises a silicon wafer and the wafer is maintained at a temperature of 20 to 50° C during the etching step.