

NONVOLATILE MEMORY DEVICE WITH A FLOATING GATE COMPRISING SEMICONDUCTOR NANOCRYSTALS

Description

Technical Field

[001] The present invention generally relates to a memory device, and more particularly to a nonvolatile memory device using semiconductor crystals and a method for making the same.

Background Art

[002] Nonvolatile memory is ubiquitous in today's technology-laden world, and the most prevalent type of device used to store information is the flash memory.

[003] In addition to the need for integrated nonvolatile memory in logic systems, there is a large (and rapidly increasing) market for flash memories as stand-alone storage elements. Cellular telephones and digital cameras are several examples of devices which benefit from nonvolatile flash memory cards.

[004] There are various forecasts predicting increased future markets for this type of storage (e.g., see P. Pavan, R. Bez, P. Olivio, and E. Zanoni, *IEEE Proc.* 85 1248 (1997)).

[005] Flash memory is based on the concept of a field effect transistor (FET) whose threshold voltage (V_T) can be reversibly changed between first and second values.

[006] As shown in the side sectional view of Figure 1(a), a conventional flash memory device 100 is shown including a substrate 101, source 102 and drain 103, formed in the substrate 101 with a channel 104 formed therebetween, a program oxide 105 formed over the substrate 101, a floating gate 106 formed over the program oxide 105, a control oxide 107 formed over the floating gate 106, and a control gate 108 formed over the control oxide 107.

[007] A main component of the flash memory device 100 which facilitates this multi-state operation is a conducting floating gate 106 in the gate stack of the transistor (see Fig. 1(a)) which is coupled to its surroundings (the control gate 108, and also the channel 104/source 102/drain 103 regions) via dielectrics (e.g., 107, 105) on top and below.

[008] The device 100 is programmed by injecting charge into the floating gate 106 (through the program oxide 105), and is erased by expelling charge from the floating gate 106. These devices 100 are made nonvolatile by decoupling the floating gate 106 from the source 102/drain 103/channel 104 and control gate 108 with a sufficiently thick control oxide 107.

[009] As with all other semiconductor technologies, flash memory continues to scale to increasingly higher densities. At the same time, improvements in device speed, power

consumption, and endurance (e.g., number of times the memory can be read/erased before failing) also pay obvious benefits.

[010] Finally, some flash memory devices have improved performance through storage of multiple bits per memory cell (e.g., most notably Intel's StrataFlash™ technology currently stores 2 bits/cell with announced future plans to increase the number of bits/cell). This is achieved by programming the floating gate 106 with different amounts of charge in order to achieve multiple possible threshold voltage (VT) shifts in the same device.

[011] The pathway to many of these density and performance benefits involves scaling the memory FET, which is becoming increasingly difficult. For example, shrinking the device width in order to improve packing density and speed results in increased drain turn-on effects from capacitive coupling between the drain 103 and the floating gate 106.

[012] Also, thinning the program oxide 105 thickness in order to achieve lower write/erase voltages (and thus lower power) has the effect of reducing retention times and reliability.

[013] Referring to Figure 1(b), nanocrystal memory devices have been proposed as a way to improve the scaling of flash memory devices, and also as a possible means to achieve robust multi-bit operation (e.g., see H. Hanafi, *IEEE Trans. Elect. Dev.* 43 1553 (1996); S. Tiwari, F. Rana, H. Hanafi, A. Hartstein, E. Crabbe, C. Chan, *Appl. Phys. Lett.* 68 1377 (1996); and S. Tiwari, F. Rana, K. Chan, H. Hanafi, W. Chan, D. Buchanan, *IEDM* 521 (1995)).

[014] Turning to the conventional nanocrystal memory device 150 shown in Figure 1(b), the structure is somewhat similar to that shown in Figure 1(a) except that the floating gate 106 is replaced with nanocrystals 156.

[015] That is, a basic idea in nanocrystal memory devices is that breaking up a continuous, conducting floating gate 106 into small bits of isolated conducting material can aid in overcoming some of the roadblocks to further scaling.

[016] The nanocrystal floating gate 156 has reduced capacitive coupling to the source 151/drain region 152, which leads to a smaller drain turn-on effect. In addition, the nanocrystal floating gate 106 should make the device less susceptible to stress-induced leakage current. That is, if an individual nanocrystal becomes shorted to the channel 154, other nanocrystals remain unaffected. In a standard floating gate device (e.g., such as device 100), any short to the channel 104 is disastrous because charge can no longer be maintained in the floating gate 106.

[017] Nanocrystal floating gate devices (e.g., such as those exemplified by reference numeral 150 in Figure 1(b)) have improved retention characteristics compared to conventional flash devices with the same program oxide thicknesses, because most charge

leakage from the floating gate 156 occurs to the heavily doped source 152/drain regions 153.

- [018] In a flash device, such leakage will deplete charge from the entire floating gate, resulting in a loss of memory (e.g., in the same way as stress-induced leakage currents compromise the device).
- [019] In a nanocrystal device, only those nanocrystals in close proximity to the source 152/drain 153 lose their charge by this leakage mechanism, while those farther away (e.g., near the device center) do not. This argument assumes that there is no electrical conduction between nanocrystals in the floating gate 156 (e.g., a condition which can be controlled via the nanocrystal density).
- [020] The improved retention properties of nanocrystal floating gate devices 150 allows scaling to thinner program oxides 155, which can result in added benefits. Thinner oxides 155 permit programming at lower voltages using direct quantum mechanical tunneling, rather than Fowler-Nordheim field emission processes.
- [021] In addition to the obvious lower-power benefit of lower voltage operation, there is some evidence which suggests that a direct tunneling write/erase mechanism puts less stress on the program oxide 155, thereby resulting in increased device cyclability. Modeling also suggests that devices with thinner oxides 155 can be programmed more quickly (e.g., see M. She, Y. C. King, T. J. King, C. Hu, *IEEE Device Research Conference*, 139 (2001)).
- [022] One of the more intriguing aspects of nanocrystal memories 150 is the possibility to program the floating gate 156 with discrete numbers of electrons, which in turn leads to multiple discrete, well-defined device threshold voltage (VT) shifts. The idea is that the electrostatic energy necessary to add a single charge to a sufficiently small nanocrystal can become significant. This electrostatic charging energy is given by:
- [023] (1) **[coded mathematical formula included]** where e is the electron charge and CS is the nanocrystal capacitance to its surroundings. Tiwari *et al.* have estimated this charging energy for different diameter nanocrystals (in this calculation, the nanocrystals were assumed to be spherical) (e.g., see S. Tiwari, J. A. Wahl, H. Silva, F. Rana, J. J. Welser, *Appl. Phys. A* 71 403 (2000)). The results are shown in Table 1. The charge stored in the floating gate will shift the device VT by an amount:
- [024] (2) **[coded mathematical formula included]** where Q is the amount of charge stored on the floating gate 156 and C_{ctl} is the floating gate capacitance to the control gate 158. Tiwari *et al.* have also computed the DVT for charge stored in different sized nanocrystals. These results are also shown in Table 1 below.

Table 1

Nanocrystal	E_c (eV)	ΔV_T (for a single added
-------------	------------	----------------------------------

Diameter (nm)	charge) (V)	
30	.011	.03
20	.018	.06
10	.036	.23
5	.072	.8
2	.178	>5

- [025] Table 1 above illustrates a calculated charging energy (E_c) and corresponding threshold voltage shift (DVT) for nanocrystals of different sizes (e.g., from Tiwari *et al*., mentioned above).
- [026] Table 1 shows that the addition of a single charge to a nanocrystal can result in a significant threshold voltage shift (DVT~0.5 V for a nanocrystal diameter between 5-10 nm). In this way, it may be possible to use this effect for multi-bit storage, where discrete V_T shifts correspond to adding incrementally larger numbers of charges to the floating gate 156. These types of discrete V_T shifts from adding single charges have been seen experimentally in extremely small devices in which the floating gate 156 contains only a single nanocrystal (e.g., see J. J. Welser, S. Tiwari, S. Rishton, K. Y. Lee, Y. Lee, *IEEE Elect. Dev. Lett.* 18 278 (1997)).
- [027] In more conventional devices where the floating gate 156 contains many nanocrystals (e.g., instead of a single one), effects due to discrete charging are usually averaged out due to nanocrystal size distributions.
- [028] In order to observe this effect (and thus make possible multi-bit storage in the device), it is essential to define all nanocrystals to be of similar size.
- [029] Several groups have demonstrated implementations of nanocrystal-based flash memories. However, none has defined all nanocrystals to be of similar size by using a self-assembly technique.
- [030] Tiwari *et al.* have published numerous papers and also hold a patent (e.g., see U.S. Patent No. 5,714,766, incorporated herein by reference) on a memory device based on CVD-deposited silicon nanocrystals.
- [031] Kim *et al.* have also published results on a similar device (e.g., see I. Kim *et al.*, *IEEE Electron Dev. Lett.* 20 630 (1999)). Welser *et al.* (e.g., see above-mentioned J. J. Welser, S. Tiwari, S. Rishton, K. Y. Lee, Y. Lee, *IEEE Elect. Dev. Lett.* 18 278 (1997)), have demonstrated a memory device based on a single nanocrystal in the floating gate. This type of device is often called a "quantum dot memory". Chou *et al.* also hold a patent on this device structure (e.g., see U.S. Patent No. 6,069,380, incorporated herein by reference).
- [032] Ostraat *et al.* have described operation of a memory device in which the floating

gate contains aerosol-deposited silicon nanocrystals (e.g., see M. L. Ostraat et al., *Appl. Phys. Lett.* 79 433 (2001)).

[033] Finally, King *et al.* have described a device containing germanium nanocrystals (e.g., see Y. C. King, T. J. King, C. Hu, *IEDM*, 155 (1998)).

[034] However, in each of these conventional demonstrations, the nanocrystal sizes were not well-defined, thereby leading to limitations on device performance improvements.

[035] Additionally, as mentioned above, nanocrystal floating gate memories have been difficult to use for multi-bit memory applications, because of the large nanocrystal size distributions.

[036] Further, defining all nanocrystals to be of substantially similar size (and thus making possible multi-bit storage in the device), has not been achieved.

[037] Moreover, there has been no technique which produces a nanocrystal memory device having nanocrystal size distributions which are substantially uniform, using a self-assembly technique.

[038] In sum, the conventional techniques (and subsequently the resulting structure) to make a nanocrystal memory have been notoriously unreliable, and it has been difficult to obtain uniform size of the nanocrystals, and difficult to control the spacing of the distribution around the sample, each of which impact the performance of the device.

Disclosure of Invention

[039] In a first aspect of the present invention, a floating gate for a field effect transistor, includes discrete nanoparticles whose dimensions and distribution are defined by a self-assembling material. For example, in one exemplary aspect, the nanoparticles may have diameters between about 2 and about 30 nanometers, with size distributions no greater than substantially 15 % of a mean diameter of the nanoparticles.

[040] In a second aspect of the present invention, a field effect transistor, includes a source region and a drain region formed in a semiconductor material, a channel region disposed between the source region and the drain region, an insulating layer of electrically insulating material disposed over the channel region, a floating gate layer of electrically conducting material disposed over the insulating layer, a layer of electrically insulating material disposed over the floating gate layer, and a gate electrode overlying the layer of insulating material. The floating gate layer includes discrete nanoparticles whose dimensions and distribution are defined by a self-assembling material.

[041] For example, in one aspect, the nanoparticle density may be greater than $10^{10}/\text{cm}^2$. In addition, in one aspect, the nanoparticles may be arranged in a cubic lattice, or a close-packed, two-dimensional hexagonal lattice. Further, the hexagonal lattice may include an average inter-nanoparticle distance between about 1 and about 2 times an

average nanoparticle diameter, and a standard deviation of inter-nanoparticle distance no greater than substantially 20% of the mean distance. More specifically, the nanoparticles in the floating gate may include first and second distinct sizes, each with diameter standard deviations being less than approximately 15% of a mean diameter of the nanoparticles.

[042] Further, in this aspect of the present invention, self assembly may involve a block copolymer film. For example, the block copolymer may include a diblock copolymer including a molecular weight within a range of about 5,000 kg/mol to about 250,000 kg/mol.

[043] In a third aspect of the present invention, a method of forming a floating gate for a field effect transistor, includes forming discrete nanoparticles whose dimensions and distribution are defined using a self-assembled material to template the nanoparticles.

[044] In a fourth aspect of the present invention, a method for making a uniform nanoparticle array, includes replicating a dimension of a polymer template in a dielectric film, to form a porous dielectric film, conformally depositing a material over the porous dielectric film, and anisotropically and selectively etching the deposited material.

[045] In a fifth aspect of the present invention, a method for making a uniform nanoparticle array, includes performing a diblock copolymer thin film self assembly over a material film, creating a polymer dot array from the diblock copolymer thin film, and using a polymer dot of the polymer dot array as an etch mask for a nanoparticle reactive ion etching (RIE) of the material film.

[046] In a sixth aspect of the present invention, a method for making a uniform nanoparticle array, includes performing a diblock copolymer thin film self assembly over silicon, creating a porous polymer film, directionally depositing a first material over the porous polymer film, and dissolving the polymer to lift off at least one region of the first material deposited over the porous polymer.

[047] In a seventh aspect of the present invention, a method for making a uniform nanoparticle array, includes performing a diblock copolymer thin film self assembly over a first dielectric over an oxidizable material film, creating a porous polymer film, transferring a pattern into the first dielectric, etching the pattern into the material, and thermally oxidizing the material until a narrowest material region between hexagonally-arranged pores close, thereby leaving an array of material nanoparticles.

[048] In an eighth exemplary aspect of the present invention, a method for making a uniform nanoparticle array, includes performing diblock copolymer thin film self assembly over a first dielectric on silicon, creating a porous polymer film, transferring a pattern into the first dielectric, and selectively growing epitaxial silicon off a silicon substrate from within pores to create a silicon nanoparticle array.

[049] Additionally, the invention provides a method of fabricating a nanocrystal memory device.

[050] With the unique and unobvious combination of exemplary features of the invention, a nanocrystal memory device can be formed in which the nanocrystals can be defined using a self-assembly process.

[051] Thus the present invention allows the formation of a nanocrystal memory device in which a self-assembled material is used to template or define the nanocrystals, and allowing good control over the uniformity of the size of the nanocrystal particles, and over their distribution (e.g., where the nanocrystals are located and the spacing between them).

[052] Hence, the method results in a device having a regular array of such nanocrystals throughout the active area of the device.

Brief Description of the Drawings

[053] A preferred embodiment of the present invention will now be described in detail by way of example only with reference to the following drawings in which:

[054] Figure 1(a) illustrates a schematic diagram of a conventional flash memory device 100;

[055] Figure 1(b) illustrates a schematic diagram of a conventional nanocrystal memory device 150;

[056] Figure 2(a) illustrates a top-down scanning electron micrograph (SEM) image of a porous polystyrene (PS) thin film on silicon formed by diblock copolymer self assembly, and in which hexagonally-arranged dark circles are cylindrical holes in the PS film down to the substrate from which the PMMA has been selectively removed;

[057] Figure 2(b) illustrates a histogram of pore diameters showing a narrow distribution of ~10% centered around 20 nm for PS-PMMA molecular weight 67 kg/mol;

[058] Figures 3(a)-3(h) illustrate schematic diagrams depicting silicon nanocrystal array formation based on diblock copolymer self assembly, and more specifically:

[059] Figure 3(a) illustrates a step 310 of assembling PS-PMMA diblock copolymer on a thermally-oxidized silicon substrate; Figure 3(b) illustrates a step 320 of removing the PMMA block, leaving a porous PS template;

[060] Figure 3(c) illustrates a step 330 of using reactive ion etching (RIE) to transfer the PS pattern into the oxide film;

[061] Figure 3(d) illustrates a step 340 of stripping the remaining polymer, leaving a porous oxide film;

[062] Figure 3(e) illustrates a step 350 of conformally depositing a material (e.g., silicon);

[063] Figure 3(f) illustrates a step 360 of anisotropically etching the silicon; and

[064] Figure 3 (g) illustrates a step of 370 stripping oxide to leave the silicon nanocrystal

array on silicon; and

[065] Figure 3(h) illustrates a flowchart of the method 300 shown in Figures 3(a)-3(g); and

[066] Figures 4(a)-4(j) illustrate a schematic process flow 400 showing formation of a nanocrystal memory device, and more specifically;

[067] Figure 4(a) illustrates a step of assembling PS-PMMA diblock copolymer on a thermally-oxidized silicon substrate;

[068] Figure 4(b) illustrates a step of removing the PMMA block, leaving a porous PS template;

[069] Figure 4(c) illustrates a step 430 using reactive ion etching (RIE) to transfer the PS pattern into the oxide film;

[070] Figure 4(d) illustrates a step of stripping the remaining polymer, leaving a porous oxide film;

[071] Figure 4(e) illustrates a step of conformally depositing a material (e.g., silicon);

[072] Figure 4(f) illustrates a step of anisotropically etching the silicon;

[073] Figure 4 (g) illustrates a step of stripping oxide to leave silicon nanocrystal array on silicon;

[074] Figure 4 (h) illustrates a step of stripping oxide to leave silicon nanocrystal array on silicon;

[075] Figure 4 (i) illustrates a step of stripping oxide to leave silicon nanocrystal array on silicon; and

[076] Figure 4(j) illustrates a flowchart of the method 400 shown in Figures 4(a)-4(i).

Mode for the Invention

[077] Referring now to the drawings, and more particularly to Figures 2-4(j), there are shown exemplary method and structures in accordance with preferred embodiments of the present invention.

[078] First, hereinbelow is described an exemplary method for making dense silicon nanocrystal arrays based on self-assembly in accordance with a preferred embodiment of the present invention.

[079] In a preferred embodiment self-assembling materials, which are not exclusively the particular diblock copolymers described below, can be employed. There are a variety of different material which naturally form regular arrays which make it possible to take advantage of the scale in self-assembling materials. Indeed, there are nanoparticles which self-assemble, there are proteins which naturally self-assemble, there are block copolymers which naturally self-assemble, there are self-assembled pores in anodized alumina, there are other self-assembling molecules including self-assembled monolayers (SAMs), etc., all of which the invention may be applied advantageously

thereto. It will be appreciated by those skilled in the art that while diblock copolymer is described here, any such self-assembling material could be employed.

[080] The use of self-assembly is clearly different from the conventional techniques. That is, the conventional techniques may include using a chemical vapor deposition (CVD) technique to scatter silicon over the sample. While this technique may be somewhat acceptable under some conditions, there is little control of the distribution, and there are small and large sizes randomly over the sample.

[081] Another technique (e.g., on the other extreme from CVD) is using lithography in which patterning occurs, and more specifically a point is written at each location where a particle is to be placed. Such a technique is very tedious and slow, is not a very manufacturable solution, and does not achieve the resolution or reliability that can be achieved in a self-assembly process.

[082] Thus, the use of self-assembly overcomes the problems of the conventional techniques and allows controlling the size distribution and positions (e.g., situs) of the particles, as well as a technique which is potentially more manufacturable, simpler, and scalable.

[083] In order to achieve the above-mentioned performance improvements over the conventional flash memory and conventional nanocrystal memory devices, nanocrystals in the device floating gate in accordance with a preferred embodiment of the present invention must be discrete (i.e., electrically isolated from each other), and densely-spaced (e.g., in order to prevent electron conduction by percolation through the silicon channel).

[084] For multi-bit memory operation, nanocrystal sizes should be highly uniform. Nanocrystal sizes on the order of about 3 nm to about 10 nm diameters should provide sufficient Coulomb charging energies for single-electron charging behavior at room temperature (e.g., see above-mentioned Tiwari et al. Article).

[085] Because the transistor device dimensions are typically defined at the limit of lithographic resolution, the nanocrystals residing in the gate stack must be much smaller than this and therefore must be defined using some non-lithographic means.

[086] As mentioned above, previous demonstrations have used CVD-deposited or aerosol-deposited nanocrystals, which have inherent size variations.

[087] In a preferred embodiment of the present invention, the nanocrystals are preferably patterned using a self-assembly process, which sets (e.g., templates or defines) the dimensions, density, and uniformity of the nanocrystals. The characteristic dimensions of self-assembled films depend on fundamental length scales (e.g., such as molecular size), and are therefore inherently more controllable than structures defined using deposition processes, whose size distributions are limited by nucleation and diffusion effects, and sample topography.

[088] There are many self-assembling systems that result in regular arrays of nanometer-scale features.

[089] In a preferred embodiment of the present invention, a system is provided based exemplary on diblock copolymer self-assembly. Obviously, the invention is not limited to the diblock copolymer material as mentioned above and would be clearly evident to one of ordinary skill in the art taking the present application as a whole. Indeed, other materials which could be used may include, as mentioned above, self-assembled nanoparticles, anodized alumina, self-assembling proteins, etc.

[090] Under suitable process conditions (e.g., such as molecular weight, block weight ratio, film thickness, annealing conditions, surface treatment and the like), diblock copolymer molecules can microphase separate on a nanometer-scale length scale, thereby forming a hexagonal array of pores in a thin polymer film.

[091] Many different polymers (e.g., such as:

[092] Polybutadiene-polybutylmethacrylate,

[093] Polybutadiene-polydimethylsiloxane,

[094] polybutadiene-polymethylmethacrylate,

[095] polybutadiene-polyvinylpyridine,

[096] polyisoprene-polymethylmethacrylate,

[097] polyisoprene-polyvinylpyridine,

[098] polybutylacrylate-polymethylmethacrylate,

[099] polybutylacrylate-polyvinylpyridine,

[100] polyhexylacrylate-polyvinylpyridine,

[101] polyisobutylene-polybutylmethacrylate,

[102] polyisobutylene-polydimethoxysiloxane,

[103] polyisobutylene-polymethylmethacrylate,

[104] polyisobutylene-polyvinylpyridine,

[105] polybutylmethacrylate-polybutylacrylate,

[106] polybutylmethacrylate-polyvinylpyridine,

[107] polyethylene-polymethylmethacrylate,

[108] polymethylmethacrylate-polybutylacrylate,

[109] polymethylmethacrylate-polybutylmethacrylate,

[110] polystyrene-polybutadiene,

[111] polystyrene-polybutylacrylate,

[112] polystyrene-polybutylmethacrylate,

[113] polystyrene-polybutylstyrene,

[114] polystyrene-polydimethoxysiloxane,

[115] polystyrene-polyisoprene,

[116] polystyrene-polymethylmethacrylate,

- [117] polystyrene-polyvinylpyridine,
[118] polyethylene-polyvinylpyridine,
[119] polyvinylpyridine-polymethylmethacrylate,
[120] polyethyleneoxide-polyisoprene,
[121] polyethyleneoxide-polybutadiene,
[122] polyethyleneoxide-polystyrene, and
[123] polyethyleneoxide-polymethylmethacrylate
[124] could be used for this process and other phase morphologies are achievable (e.g., besides the hexagonal close-packed cylindrical phase morphology described here). For example, other phase morphologies may include spherical phase, the lamellar phase, etc.
- [125] Hereinbelow and referring first to Figures 2(a) and 2(b), is detailed an exemplary self-assembly process using diblock copolymers exemplary including polystyrene (PS) and poly(methyl methacrylate) (PMMA).
- [126] First, the PS-PMMA diblock copolymers are preferably diluted in a solvent such as toluene or the like, and spin-cast as a thin film preferably having a thickness within a range of about a few nanometers to about a few hundred nanometers onto a sample (e.g., such as a hard mask oxide underneath (e.g., SiO_2 which is thermally grown on silicon) or the like).
- [127] Then, the sample is heated (e.g., to a temperature within a range of 140 °C to about 200 °C, for several hours), thereby to promote the microphase separation (hexagonally close packed (hcp)) array of the exemplary polymers (as shown exemplary in Figure 2(a)), which results in an ordered array formation in the film.
- [128] It is noted that it is the temperature which allows the two types of polymers to separate themselves from one another, and gives them mobility. Thus, the temperature and the time are significant, but may vary depending upon the polymer system, with a particular thickness, concentration, etc.
- [129] For PS-PMMA copolymers having, for example, a molecular weight 67 kg/mol and a mass ratio of 70:30 PS:PMMA, the resulting self assembled film (~40 nm thick) is composed of 20-nm-diameter PMMA cylinders (e.g., the black circles shown in Figure 2(a)) arranged in a hexagonal lattice (40 nm center-to-center spacing) embedded in a matrix of PS (e.g., shown in the white areas in Figure 2(a) around the PMMA). Again, the temperature allows this material to phase-separate into the shown ordered pattern. Prior to being heated, the film is a mixture of the two polymers which are not physically separated yet.
- [130] Again, it is noted that other morphologies can be employed, and thus "ordered array" is not limited to hcp, and may include others such as spherical or lamellar arrays which result in a different packing arrangement and which depend on the morphology

of the materials and the ratio of molecular weights of the two polymers.

- [131] Then, a simple aqueous developing step (e.g., using acetic acid or the like) can selectively remove the PMMA, leaving a porous PS film (e.g., porous template having a thickness of 40 nm center-to-center spacing of adjacent holes), as shown in Figure 2(a).
- [132] The size and density of the holes created in the PS will be varied depending upon the molecular weights of the materials (e.g., polymers) selected. Thus, choosing a material (e.g., PMMA) with a larger molecular weight will create larger holes (e.g., larger spacings). Greater (or lesser) spacing may be desirable depending upon the application. For example, for a flash memory device, it may be desirable to scale the devices to a smaller physical size, and thereby scaling the size of the nanoparticles at the same time would be desirable. Selectively using the molecular weight of the materials allows such a scaling and control to a smaller size.
- [133] It is noted that, instead of the aqueous developing step, another step could be performed such as etching to leave the topography. Thus, preferred embodiments of the present invention are not limited to the aqueous developing step.
- [134] Returning to Figure 2(a), the black circles indicate where the PMMA resides after it is phase-separated, and the white surrounding the PMMA represents the PS matrix.
- [135] Figure 2(b) shows a histogram of pore diameters in the PS-PMMA film. The narrow distribution (e.g., 10%) around the 20-nm mean-diameter shows that these films are highly uniform.
- [136] The characteristic dimensions of features in the self-assembled film can be adjusted by beginning with a different copolymer molecular weight, with typical pore diameters ranging from about 10 to about 100 nm.
- [137] Hence, Figure 2(a) shows a top-down SEM image of a porous PS thin film on silicon formed by diblock copolymer self assembly. The hexagonally-arranged dark circles are cylindrical holes in the PS film down to the substrate from which the PMMA has been selectively removed. Figure 2(b) shows a histogram of pore diameters showing a narrow distribution of ~10% centered around 20 nm for PS-PMMA molecular weight 67 kg/mol.
- [138] The thin porous polymer template formed from diblock copolymer self assembly is compatible with standard semiconductor processes (e.g., it does not introduce contamination and can be used in a manner similar to a polymer resist for reactive ion etch (RIE) transfer, etc.), and can therefore be used as a mask for transfer of the nanometer-scale pattern into an underlying film or substrate (as described below). (This is often desirable since the polymer template is neither thermally stable nor mechanically robust.)
- [139] The above steps will be used in building an exemplary device of interest according

to a preferred embodiment of the present invention, and as described below.

[140] Figures 3(a)-3(g) illustrate schematic diagrams depicting a method 300 (see Figure 3(h) showing a flowchart of the process) of silicon nanocrystal array formation based on diblock copolymer self assembly. That is, Figures 3(a)-3(g) illustrate schematically how to form a dense array of nanocrystals beginning with a self-assembled PS-PMMA film (e.g., which has been exemplary formed as described above and shown in Figure 2(a)).

[141] First, the thin film of PS 303 and PMMA 304 is prepared on a thermally oxidized (e.g., SiO_2 or the like 302) silicon wafer 301, as shown in Fig. 3(a) (step 310 in Figure 3(h)).

[142] Then, the PMMA 304 is removed from the pores (e.g., as shown in Fig. 3(b) and in step 320), and the pattern (e.g., PS 303) is transferred into the oxide film using a reactive ion etch (RIE) process (e.g., a directional etch using CHF_3 and argon or the like as shown in Fig. 3(c) and in step 330).

[143] Then, the remaining polymer (PS) 303 is removed (e.g., as shown in Fig. 3(d) and step 340), to leave a porous oxide film 302 which has the same dimensions as were in the porous polymer film.

[144] In step 350 and as shown in Figure 3(e), a thin film 306 of conformally-deposited material (e.g., silicon, such as polysilicon or amorphous silicon, or potentially other materials from which nanocrystals may be formed such as germanium or silicon germanium or metal; an amorphous silicon layer will be assumed in the exemplary process) is deposited on top of the porous oxide 302. The conformally deposited film 306 preferably should be continuous and preferably should fully conformally cover the surface. Preferably, the thin film 306 has a thickness which is more than about half the pore diameter because the holes must be filled up.

[145] That is, since the thin film 306 should be a truly conformal deposition which covers every surface with the same thickness regardless of the surface being a vertical surface or a horizontal surface, in order to fill up or "pinch off" the holes, the thickness deposited should be at least half of the width on either side of the hole in order to pinch together. Thus, the thickness deposited should be at least half of the diameter of the pore.

[146] Hence, since a directional etch is to be performed subsequently, it is noted that because of the dimension of the patterns, a vertical thickness of the deposited silicon layer (e.g., amorphous silicon layer) is much greater inside the hole than it is on top of the oxide. It is possible to take advantage of such a greater thickness to leave material in these holes which will become the silicon nanocrystals.

[147] Then, in step 360 and as shown in Figure 3(f), the conformally deposited silicon 306 is etched using an anisotropic directional etch RIE process that leaves silicon 306

in the pores. Thus, the directional etch of silicon is performed (e.g., preferably selective against the silicon oxide, but not an etch stop in the conventional sense), stopping on the silicon oxide 302. However, as mentioned above, it is not a natural stop, and it could be possible to continue to etch and remove all of the silicon in the pores. However, this would not be desirable.

[148] Thus, care must be taken to etch just a sufficient amount of silicon material, such that the silicon remains as discrete particles. Thus it is possible to ensure that the amount of material left in the holes preserves the dimensions of the original polymer film (e.g., no shrinkage or growing thereof).

[149] As shown in step 370 and in Figure 3(g), optionally, the oxide 302 is selectively removed using a wet chemical etch or the like such as dilute hydrofluoric acid (HF), thereby resulting in a dense regular array of silicon "dots" (e.g., structures) extending over the sample that reproduce the pore pattern in the original PS-PMMA film.

[150] Thus, with the exemplary process above, it is possible to form an array of silicon particles having the same dimensions as the polymer pores.

[151] It is noted that, as further described below with regard to Figures 4(a)-4(g), the oxide 302 may be left in building a nanocrystal memory device.

[152] Several related and similar techniques could be implemented to create nanocrystal arrays, such as variations on the etch processes or dielectric films used. For example, the dielectric films do not necessarily need to be SiO_2 . Such dielectric films could be oxide, nitride, high-k, or dielectric film stacks. Also, nanocrystals of different material, such as germanium, silicon germanium, and metal, can be created by conformal deposition of materials other than silicon, such as germanium, silicon germanium, and/or metal (e.g., different from that of silicon shown in Fig. 3(e)).

[153] Thus, with this exemplary process nanoparticles (e.g., formed of silicon or the like) have been formed having uniform dimensions by self-assembly.

[154] Hereinbelow, a process flow is described for fabricating the nanocrystal flash memory device, as depicted in Figures 4(a)-4(i) and the flowchart of Figure 4(j), utilizing the nanoparticles having the uniform dimensions as described above.

[155] A key advantage of this device structure is that self-assembly is used to define a dense array of uniform nanometer-scale silicon nanocrystals in the gate stack of the FET.

[156] A key component of the device is a gate stack, and hereinbelow is provided a process flow for producing a stack containing uniformly-sized silicon nanocrystals separated from the silicon channel below by a thin program dielectric.

[157] In step 410, a substrate 401 is provided (e.g., a p-type Si substrate).

[158] Then, a layer of oxide 402 (e.g., exemplary SiO_2) is used, but of course other oxides and nitrides or stack dielectrics or high k dielectrics could be employed is thermally

- grown on the substrate 401 or deposited by CVD or atomic layer deposition (ALD) or other means, as shown in step 420 and Fig. 4(b). This layer thickness defines nanocrystal heights, and may exemplarily be between about 2 to about 20 nm thick. As would be evident to one of ordinary skill in the art, the conductivity of the substrate could be different and it is not required that a p-type substrate is used.
- [159] As shown in step 430 and in Figure 4(c), the diblock copolymer 403 self assembly process is performed on top of this oxide layer 402, and the nanometer-scale pattern is transferred into oxide 402 using the RIE process depicted earlier in Figure 3(c).
- [160] After the RIE, the polymer 403 is stripped, and the wafer cleaned (e.g., by O₂ plasma, and wet chemical cleaner, or the like), thereby leaving a porous dielectric (oxide) film 402A on silicon 401, as shown in step 440 and Fig. 4(d).
- [161] At this stage, the nanometer-scale holes 404 can be optionally shrunk (e.g., to any desired size after the holes are formed) using a nitride deposition and anisotropic etch.
- [162] That is, as described above, one can start initially with different polymer molecular weights to set (e.g., template or define) any of the size, the distribution and spacing of the holes of the polymer.
- [163] However, as another option, a fixed polymer could be used, and after the polymer pattern has been transferred into oxide, the holes could be widened or shrunk once they are in the dielectric material. There are two exemplary methods for performing such a widening or shrinking of the holes.
- [164] First, in Figure 4(d) in which the PS pattern has been transferred into the oxide to make them porous, the holes could be further etched (e.g., overetched), which would widen the holes further laterally, but preserve their center positions, center-to-center spacing, and uniformity. This would make the holes larger. Alternatively, the holes could be shrunk by depositing a conformal, very thin (e.g., having a thickness of ~2-8 nm) nitride dielectric deposition, and then performing an anisotropic silicon nitride RIE etch, which leaves a small nitride ring around the edge of the hole, thereby making the hole narrower than before, but preserving the uniformity of the size.
- [165] Thus, the size of the nanoparticles (to be built) can be suitably adjusted by this step, and allows setting and precisely controlling the dimensions of the nanoparticles.
- [166] Hence, in contrast to the conventional techniques including CVD processes of making a nanocrystal gate device, in which all that can be set is an exemplary particle dimension "which may be within a range of 2-50 nm" and which are scattered randomly all over the wafer with an average distance of "X", it is possible to achieve a very precise controlling of the dimensions of every particle, and can set a very precise specification (e.g., a specification can be made for "a particle having a 20 nm $\pm$ 1-2 nm, and positioned such that each particles is spaced 40 nm from the next").
- [167] Hence, a precise spacing and sizing can be obtained. Indeed, it has been shown to

achieve a substantially uniform particle spacing (e.g., a center-to-center spacing between adjacent particles) with a variance of no more than 20%. More specifically, the variance of the particle spacing may be no more than about 15%. More specifically, the variance of the particle spacing may be no more than about 10%.

[168] Thus, it has been shown to achieve a substantially uniform particle spacing, having a variance of the spacing within a range of about 10% to about 20%. This is in contrast to the CVD method in which the particles are typically clustered randomly on the wafer.

[169] Next, as shown in step 450 and in Figure 4(e), a program oxide 405 is thermally grown (e.g., having an exemplary thickness within a range of about 1.5 to about 4 nm).

[170] This is followed by step 460 in which a conformal silicon 406 (e.g., similar to the amorphous or polysilicon, etc. as above in step 350 of Figure 3(e)) is deposited, as shown in Fig. 4(f).

[171] As shown in step 470 and in Figure 4(g), nanocrystals 407 are defined and isolated from each other with an anisotropic silicon RIE which stops when the oxide layer 402A below is reached.

[172] The thermal oxide 402A between the nanocrystals can be optionally thinned or removed at this stage by selective wet chemical or RIE etching.

[173] Next, in step 480 and as shown in Figure 4(h), a layer of oxide 408 is deposited over (e.g., on top of) the nanocrystals. This layer 408 will serve as the control oxide in the device (e.g., typical thickness values range from about 4 to about 10 nm).

[174] The control oxide is formed preferably by deposited low-temperature oxide such as low pressure CVD (LPCVD) oxide (or plasma-enhanced CVD (PECVD) or rapid thermal CVD (RTCVD) or atomic layer deposition (ALD)). Alternatively, the control oxide may be formed by thermal oxidation (e.g., preferably at a temperature within a range of about 700° to about 1100°) of the silicon nanocrystals. The gate material 409 is deposited next, and is preferably formed of poly-Si or metal having a suitable thickness.

[175] The nanocrystals can optionally be crystallized using a high- temperature anneal. It is noted that typically an amorphous silicon layer is deposited and then etched. Hence, typically the material is amorphous and not necessarily crystalline. However, the conventional device fabrication methods oftentimes use temperatures which are high enough such that the particles become crystallized. Thus if the temperature was kept relatively low (the temperature range depending, of course, on the material being used), then the amorphous nature of the material could be retained.

[176] It is noted again that while the exemplary embodiment above has used silicon to generate the nanocrystals, any material could be used so long as the material can be directionally etched and can be conformally deposited. For example, instead of silicon,

Ge, SiGe, or another material could be employed for the nanocrystals.

[177] Once the gate stack is grown, the device can be completed (source/drain patterning, gate contact) using standard FET fabrication processes.

[178] Such processes may involve removing the nanocrystals from the source/drain region, patterning the source/drain, and performing a self-aligned source/drain implant to define highly-doped regions. These processes are schematically illustrated in step 490 and in Fig. 4(i).

[179] Thus, with the unique combination of exemplary features described hereinbefore a nanocrystal memory device can be formed in which the nanocrystals can be defined using a self-assembly process.

[180] It is important to note that in the preferred embodiments of the present invention at least one of a size, spacing, and density of the nanoparticles may be templated by the self-assembled material (e.g., as illustrated in Figures 4(a)-4(j)). Alternatively, at least one of the size, spacing, and density of the nanoparticles may be defined by the self-assembled material (e.g., where the nanoparticles are separated by the self-assembled material).

[181] Further, the nanocrystal memory device (and method for forming it) allows good control over the uniformity of the size of the nanocrystal particles, and over their distribution (e.g., where the nanocrystals are located and the spacing between them). Thus, the inventive method results in a device having a regular array of such nanocrystals throughout the active area of the device.

[182]

Claims

- [001] A floating gate for a field effect transistor, comprising: a plurality of discrete nanoparticles in which at least one of a size, spacing, and density of said nanoparticles is one of templated and defined by a self-assembled material.
- [002] The floating gate of claim 1, wherein said nanoparticles have diameters between about 2 and about 30 nanometers, with size distributions no greater than substantially 15 % of a mean diameter of the nanoparticles.
- [003] The floating gate of claim 1, wherein a particle spacing is substantially uniform, having a variance of no more than 20 %.
- [004] The floating gate of claim 3, wherein said particle spacing is substantially uniform, having a variance of no more than 15 %.
- [005] The floating gate of claim 4, wherein said particle spacing is substantially uniform, having a variance of no more than 10 %.
- [006] The floating gate of claim 2, wherein a center-to-center spacing between adjacent nanoparticles is controlled to have a variance within a range of 10 % to about 20 %.
- [007] A floating gate for a field effect transistor, comprising: a plurality of discrete nanoparticles, wherein said nanoparticles have diameters between about 2 and about 30 nanometers, with size distributions no greater than substantially 15 % of a mean diameter of the nanoparticles.
- [008] A field effect transistor, comprising: a source region and a drain region formed in a semiconductor material; a channel region disposed between said source region and said drain region; an insulating layer of electrically insulating material disposed over said channel region; a floating gate layer of electrically conducting material disposed over said insulating layer; a layer of electrically insulating material disposed over said floating gate layer; and a gate electrode overlying said layer of insulating material, wherein said floating gate layer includes a plurality of discrete nanoparticles in which at least one of a size, spacing, and density of said nanoparticles is one of templated and defined by a self-assembled material.
- [009] The field effect transistor of Claim 8, wherein said nanoparticles in said floating gate have diameters between about 2 and about 30 nanometers, with size distributions no greater than substantially 15 %.
- [010] The field effect transistor of Claim 8, wherein said self assembly involves a block copolymer film.
- [011] The field effect transistor of Claim 10, wherein said block copolymer comprises a diblock copolymer including polystyrene (PS) and poly(methyl methacrylate)

(PMMA).

- [012] The field effect transistor of Claim 8, wherein said nanoparticles include at least one of silicon, germanium, and silicon-germanium.
- [013] The field effect transistor of Claim 8, wherein said nanoparticle density is greater than $10^{10}/\text{cm}^2$.
- [014] The field effect transistor of Claim 8, wherein said nanoparticles are arranged in a close-packed, two-dimensional hexagonal lattice.
- [015] The field effect transistor of claim 14, wherein said hexagonal lattice includes an average inter-nanoparticle distance between about 1 and about 2 times an average nanoparticle diameter, and a standard deviation of inter-nanoparticle distance no greater than substantially 20% of the mean distance.
- [016] The field effect transistor of Claim 8, wherein said nanoparticles in said floating gate include first and second distinct sizes, each with diameter standard deviations being less than approximately 15% of a mean diameter of said nanoparticles.
- [017] The field effect transistor of Claim 10, wherein said block copolymers comprises a diblock copolymer including any of polystyrene (PS), poly(methyl methacrylate) (PMMA), polybutadiene-polybutylmethacrylate, polybutadiene-polydimethylsiloxane, polybutadiene-polymethylmethacrylate, polybutadiene-polyvinylpyridine, polyisoprene-polymethylmethacrylate, polyisoprene-polyvinylpyridine, polybutylacrylate-polymethylmethacrylate, polybutylacrylate-polyvinylpyridine, polyhexylacrylate-polyvinylpyridine, polyisobutylene-polybutylmethacrylate, polyisobutylene-polydimethoxysiloxane, polyisobutylene-polymethylmethacrylate, polyisobutylene-polyvinylpyridine, polybutylmethacrylate-polybutylacrylate, polybutylmethacrylate-polyvinylpyridine, polyethylene-polymethylmethacrylate, polymethylmethacrylate-polybutylacrylate, polystyrene-polybutadiene, polystyrene-polybutylacrylate, polystyrene-polybutylmethacrylate, polystyrene-polybutylstyrene, polystyrene-polydimethoxysiloxane, polystyrene-polyisoprene, polystyrene-polymethylmethacrylate, polystyrene-polyvinylpyridine, polyethylene-polyvinylpyridine, polyvinylpyridine-polymethylmethacrylate, polyethyleneoxide-polyisoprene, polyethyleneoxide-polybutadiene, polyethyleneoxide-polystyrene, and polyethyleneoxide-polymethylmethacrylate.
- [018] The field effect transistor of Claim 8, wherein said nanoparticles are arranged in one of a hexagonal lattice and a cubic lattice.
- [019] The field effect transistor of Claim 10, wherein said block copolymer comprises a diblock copolymer including a molecular weight within a range of about 5,000

kg/mol to about 250,000 kg/mol.

- [020] The field effect transistor of Claim 10, wherein a molecular weight of said block copolymer film is selected to determine dimensions of said nanoparticles.
- [021] The field effect transistor of Claim 10, wherein a molecular weight of said block copolymer film is selected to determine a diameter of said nanoparticles after said self-assembly and a spacing between adjacent ones of said nanoparticles.
- [022] A method of forming a floating gate for a field effect transistor, comprising: forming a plurality of discrete nanoparticles using a self-assembled material to one of template and define any of a size, spacing, and density of said nanoparticles.
- [023] A method of making a nanoparticle array, comprising: replicating a dimension of a self-assembled film into a dielectric film, to form a porous dielectric film; conformally depositing a material over said porous dielectric film; and anisotropically and selectively etching said deposited material.
- [024] The method of claim 23, wherein said nanoparticle array comprises a uniform nanoparticle array, and wherein said self-assembled film comprises a polymer template.
- [025] The method of claim 23, wherein said replicating is performed without deteriorating a dimension and uniformity inherent in the self-assembled film.
- [026] A method of making a uniform nanoparticle array, comprising: forming a diblock copolymer thin film, via self-assembly, over a first dielectric on silicon; creating a porous polymer film; transferring a pattern into said first dielectric; conformally depositing a nanoparticle material; and anisotropically etching said nanoparticle material.
- [027] The method of claim 26, wherein said creating comprises one of developing pores of said porous polymer film and etching to create pores of said porous polymer film.
- [028] The method of claim 26, wherein said nanoparticles comprise at least one of silicon, germanium, silicon-germanium, and metal.
- [029] A method of making a uniform nanoparticle array, comprising: performing diblock copolymer thin film self assembly over a first dielectric on silicon; creating a porous polymer film; transferring a pattern into said first dielectric; selectively growing epitaxial silicon off a silicon substrate from within pores to create a silicon nanoparticle array.
- [030] The method of claim 23, further comprising: shrinking said nanoparticles by oxidation or etching.
- [031] The method of claim 23, further comprising: one of shrinking pores with a spacer process prior to forming said nanoparticles, and enlarging pores by etching prior

to said forming said nanoparticles.

- [032] A method for fabricating nanocrystal memory device, comprising: the method of fabricating the nanoparticle array of claim 24; forming an oxide layer over nanocrystals of the nanocrystal particle array; and depositing a gate material over said oxide layer.
- [033] The method of claim 32, wherein said oxide layer serves as a control oxide in the device, and includes a thickness within a range from about 4 to about 10 nm.
- [034] The method of claim 32, further comprising: thermally growing a program oxide prior to forming an amorphous silicon layer for use in forming said nanocrystals.
- [035] The floating gate of claim 1, wherein said self-assembled material uses a material which naturally forms a regular array.