

ABSTRACT OF THE DISCLOSURE

An electronic system may include one or more units of processing circuitry configured to implement a main intellectual property (IP), a checker IP, and an error detection circuit. The main IP includes a first data path and a first control signal path. The checker IP includes a second control signal path. The error detection circuit is configured to detect an error of data by performing error correction code (ECC) decoding of output data that is output by the main IP to the error detection circuit through the first data path, and detect an error of a control signal based on a first signal that is output by the main IP to the error detection circuit through the first control signal path, and a second signal that is output by the checker IP to the error detection circuit through the second control signal path.

FIG. 1