CLAIMS

1. An apparatus comprising:

a first processor and a second processor;

a first set of memory and a second set of memory each communicatively coupled to the first processor and to the second processor; and

a memory from at least one of the first set of memory and the second set of memory having instructions stored thereon that when executed by at least one processor direct the at least one processor to:

execute for a first zone a computing application as a first process, wherein the first zone is assigned to the first processor such that the first process is to execute on the first processor and not execute on the second processor;

execute for a second zone a computing application as a second process, wherein the second zone is assigned to the second processor such that the second process is to execute on the second processor and not to execute on the first processor;

move the first process from an execution state to a wait state;

move the first process from the wait state to the execution state, wherein moving the first process from the wait state to the execution state includes determining that the first process is assigned to execute on the first processor and not the second processor, and executing the first process on the first processor based on the determination;

move the second process from the execution state to the wait state; and

move the second process from the wait state to the execution state, wherein moving the second process from the wait state to the execution state includes determining that the second process is assigned to execute on the second processor and not the first processor, and executing the second process on the second processor based on the determination.

2. The apparatus of claim 1, wherein the instructions, when executed by the at least one processor, further direct the at least one processor to:

receive from the first process an indication to create another process for the first zone;

determine that the first zone is assigned to the first processor; and

based at least in part on determining that the first zone is assigned to the first processor, execute the another process for the first zone on the first processor.

3. The apparatus of claim 2, wherein the instructions, when executed by the at least one processor, further direct the at least one processor to:

receive from the second process an indication to create another process for the second user;

determine that the second zone is assigned to the second processor; and

based at least in part on determining that the second zone is assigned to the second processor, execute the another process for the second zone on the second processor.

4. The apparatus of claim 3,

wherein the first processor is configured to store data on the first set of memory and the second set of memory;

wherein the second processor is configured to store data on the first set of memory and the second set of memory;

wherein the first zone is further assigned to the first set of memory such that the first process uses the first set of memory to store data and does not use the second set of memory to store data; and

wherein the second zone is further assigned to the second set of memory such that the second process uses the second set of memory to store data and does not use the first set of memory to store data.

5. The apparatus of claim 4, wherein the instructions, when executed by the at least one processor, further direct the at least one processor to:

receive from the first process an indication to allocate memory;

determine that the first zone is assigned to the first set of memory; and

based at least in part on determining that the first zone is assigned to the first set of memory, allocate memory from the first set of memory.

6. The apparatus of claim 5, wherein the instructions, when executed by the at least one processor, further direct the at least one processor to:

receive from the second process an indication to allocate memory;

determine that the second zone is assigned to the second set of memory; and

based at least in part on determining that the second zone is assigned to the second set of memory, allocate memory from the second set of memory.

7. The apparatus of claim 6, wherein the first processor, the second processor, the first set of memory, and the second set of memory are physically situated within the apparatus, wherein the first processor is physically located closer to the first set of memory than the second set of memory, and wherein the second processor is physically located closer to the second set of memory than the first set of memory.

8. The apparatus of claim 1,

wherein the first processor is configured to store data on the first set of memory and the second set of memory;

wherein the second processor is configured to store data on the first set of memory and the second set of memory;

wherein the first zone is further assigned to the first set of memory such that the first process uses the first set of memory to store data and does not use the second set of memory to store data; and

wherein the second zone is further assigned to the second set of memory such that the second process uses the second set of memory to store data and does not use the first set of memory to store data.

9. The apparatus of claim 8, wherein the instructions, when executed by the at least one processor, further direct the at least one processor to:

receive from the first process an indication to allocate memory;

determine that the first zone is assigned to the first set of memory; and

based at least in part on determining that the first zone is assigned to the first set of memory, allocate memory from the first set of memory.

10. The apparatus of claim 9, wherein the instructions, when executed by the at least one processor, further direct the at least one processor to:

receive from the second process an indication to allocate memory;

determine that the second zone is assigned to the second set of memory; and

based at least in part on determining that the second zone is assigned to the second set of memory, allocate memory from the second set of memory.

11. The apparatus of claim 10, wherein the first processor, the second processor, the first set of memory, and the second set of memory are physically situated within the apparatus, wherein the first processor is physically located closer to the first set of memory than the second set of memory, and wherein the second processor is physically located closer to the second set of memory than the first set of memory.

12. The apparatus of claim 1, wherein the first processor comprises a plurality of cores, and wherein the first zone being assigned to the first processor comprises the first zone being assigned to a subset of the plurality of cores such that the first process executes on one or more of the subset of the plurality of cores and does not execute on any core not part of the subset of cores.

13. The apparatus of claim 1 further comprising a third processor, wherein the first and third processors are spatially separated at a greater distance than the first and second processors; and

wherein the instructions, when executed by the at least one processor, further direct the at least one processor to:

determine that an amount of heat being produced by the first and second processors exceeds a threshold;

determine that at least one application of the first zone and at least one application of the second zone are correlated; and

based at least in part on determining that the amount of heat being produced by the first and second processors exceeds a threshold and that at least one application of the first zone and at least one application of the second zone are correlated, move the first zone to the third processor such that the first zone is assigned to the third processor.