CLAIMS

What is claimed is:

1. A method, comprising:

applying a zero voltage to a plurality of digit lines in a memory array, the memory array comprising a plurality of ferroelectric memory cells comprising a plurality of cell bottom nodes and a plurality of cell plates opposite the plurality of cell bottom nodes, wherein each of the cell bottom nodes is configured to be electrically coupled with a respective digit line of the plurality of digit lines; and

activating a plurality of word lines to electrically couple the plurality of digit lines to the plurality of cell bottom nodes and reset the plurality of cell bottom nodes to the zero voltage.

2. The method of claim **1**, further comprising:

receiving a signal to perform a reset operation, wherein the zero voltage is applied and the plurality of word lines are activated in response to receiving the signal.

3. The method of claim **2**, wherein:

the signal to perform the reset operation comprises a power signal.

4. The method of claim **1**, further comprising:

detecting a voltage increase corresponding to a power-up operation, wherein the zero voltage is applied and the plurality of word lines are activated in response to detecting the voltage increase corresponding to the power-up operation.

5. The method of claim **4**, wherein:

detecting the voltage increase corresponding to the power-up operation comprises detecting, by a voltage level detector, that a power source voltage has met or exceeded a threshold.

6. The method of claim **5**, further comprising:

issuing one or more signals in response to detecting that the power source voltage has passed a threshold, wherein the zero voltage is applied and the plurality of word lines are activated based at least in part on the one or more signals.

7. The method of claim **1**, wherein:

applying the zero voltage comprises activating a plurality of equalize lines.

8. The method of claim **7**, wherein:

a switching component connects a zero voltage source to the plurality of digit lines, and wherein the switching component is activated based at least in part on activating the plurality of equalize lines.

9. The method of claim **7**, wherein:

activating the plurality of equalize lines comprises applying an activation voltage to the plurality of equalize lines.

10. The method of claim **1**, wherein:

activating the plurality of word lines comprises applying an activation voltage to the plurality of word lines by an external power source.

11. The method of claim **1**, wherein:

a selection component connects the plurality of digit lines to the plurality of cell bottom nodes, and the selection component is activated based at least in part on activating the plurality of word lines.

12. The method of claim **1**, further comprising:

writing a physical data "0" to each of the plurality of memory cells.

13. The method of claim **12**, wherein:

writing a physical data "0" to each of the plurality of memory cells comprises raising a cell plate voltage of each of the plurality of cell plates.

14. A device, comprising:

a zero voltage source;

a memory array comprising a plurality of ferroelectric memory cells, each of the ferroelectric memory cells comprising:

a cell plate;

a cell bottom node opposite the cell plate;

a selection component configured to connect the cell bottom node to a digit line upon application of a first voltage to a word line, wherein each of the cell bottom nodes is configured to be electrically coupled with a respective digit line; and

a switching component configured to connect the digit line to the zero voltage source upon application of a second voltage to an equalize line.

15. The device of claim **14**, wherein:

the selection component comprises a transistor comprising a gate node coupled with the word line.

16. The device of claim **14**, wherein:

the switching component comprises a transistor comprising a gate node coupled with the equalize line.

17. The device of claim **14**, further comprising:

a voltage level detector configured to detect that a power source voltage has met or exceeded a threshold.

18. The device of claim **17**, further comprising:

a signal generator configured to generate signals to apply the second voltage to the equalize line and apply the first voltage to the word line when the voltage level detector detects that the power source voltage has met or exceeded the threshold.

19. The device of claim **14**, further comprising:

an external power source; and

a power source selection component connecting the external power source to the word line in each of the plurality of ferroelectric memory cells, wherein the power source selection component is configured to be activated upon application of a third voltage to a reset line.

20. A device, comprising:

a zero voltage source;

a plurality of memory cells, each of the plurality of memory cells comprising a digit line, a cell bottom node, and a cell plate opposite the cell bottom node;

a controller operable to cause the device to:

apply a voltage of the zero voltage source to the digit line in each of the plurality of memory cells, wherein each of the cell bottom nodes is configured to be electrically coupled with a respective digit line of the plurality of digit lines; and

apply a first voltage to each of a plurality of word lines to electrically couple the digit line to the cell bottom node in each of the plurality of memory cells and reset the cell bottom node in each of the plurality of memory cells.

21. The device of claim **20**, wherein the controller is operable to cause the device to:

apply the voltage of the zero voltage source to the digit line in each of the plurality of memory cells and apply the first voltage to the plurality of word lines in response to receiving a signal to perform a reset operation.

22. The device of claim **20**, wherein each of the plurality of memory cells is coupled with an equalize line and the device further comprises:

a switching component connecting the digit line to the equalize line, wherein the switching component is configured to be activated upon application of a second voltage to the equalize line.

23. The device of claim **22**, wherein the controller is operable to cause the device to:

apply the second voltage to the equalize line; and

apply the voltage of the zero voltage source to the digit line in each of the plurality of memory cells based at least in part on applying the second voltage to the equalize line in each of the plurality of memory cells.

24. The device of claim **20**, wherein each of the plurality of memory cells comprises a selection component connecting the cell bottom node to the digit line, and wherein the selection component is configured to be activated upon application of the first voltage to one of the plurality of word lines.

25. The device of claim **20**, wherein the controller is operable to cause the device to:

raise a cell plate voltage of the cell plate at each of the plurality of memory cells after the first voltage is applied to the plurality of word lines.

26. The device of claim **20**, wherein the controller is further operable to cause the device to:

write a physical data "0" to each of the plurality of memory cells after the first voltage is applied to the plurality of word lines.

27. An apparatus, comprising:

a zero voltage source;

a plurality of memory cells, each of the plurality of memory cells comprising a digit line, a cell bottom node, and a cell plate opposite the cell bottom node;

means for applying a voltage of the zero voltage source to the digit line in each of the plurality of memory cells, wherein each of the cell bottom nodes is configured to be electrically coupled with a respective digit line of the plurality of digit lines; and

means for applying a first voltage to each of a plurality of word lines to electrically couple the digit line to the cell bottom node in each of the plurality of memory cells and reset the cell bottom node in each of the plurality of memory cells.

28. The apparatus of claim 27, further comprising:

means for applying the voltage of the zero voltage source to the digit line in each of the plurality of memory cells and means for applying the first voltage to the plurality of word lines in response to receiving a signal to perform a reset operation.

29. The apparatus of claim 27, wherein each of the plurality of memory cells is coupled with an equalize line and the apparatus further comprises:

a switching component connecting the digit line to the equalize line, wherein the switching component is configured to be activated upon application of a second voltage to the equalize line.

30. The apparatus of claim 29, further comprising:

means for applying the second voltage to the equalize line; and

means for applying the voltage of the zero voltage source to the digit line in each of the plurality of memory cells based at least in part on applying the second voltage to the equalize line in each of the plurality of memory cells.

31. The apparatus of claim 27, wherein each of the plurality of memory cells comprises a selection component connecting the cell bottom node to the digit line, and wherein the selection component is configured to be activated upon application of the first voltage to one of the plurality of word lines.

32. The apparatus of claim 27, further comprising:

means for raising a cell plate voltage of the cell plate at each of the plurality of memory cells after the first voltage is applied to the plurality of word lines.

33. The apparatus of claim 27, further comprising:

means for writing a physical data “0” to each of the plurality of memory cells after the first voltage is applied to the plurality of word lines.