

ABSTRACT

A semiconductor memory device includes a bit line extending in a first direction, a channel pattern on the bit line, the channel pattern including first and second vertical portions facing each other and a horizontal portion connecting the first and second vertical portions, first and second word lines provided on the horizontal portion and between the first and second vertical portions and extended in a second direction crossing the bit line, and a gate insulating pattern provided between the first word line and the channel pattern and between the second word line and the channel pattern.

FIG. 4B