(8), which are each covered with a hard polishing pad (1) having ~~low compressibility, and the distance between the upper and the lower surface (2) – which comes into contact with the substrate to be polished – of the polishing pads (1) forms a polishing gap, and this polishing gap extends from the inner edge (B) of the polishing pad (1) as far as the outer edge (A) of the polishing pad (1), wherein the pad surface (2) is processed by a first dressing in such a way that the height of the polishing gap at the inner edge (B) differs from the height of the polishing gap at the outer edge (A)~~a hardness of at least 80° Shore A and a compressibility of less than 2.5%, and the space between the upper and the lower surface (2) - which comes into contact with the wafer to be polished - of the polishing pads (1) forms a polishing gap, wherein the polishing pad (1) has an outer edge (A) and an inner edge (B) adjacent to a center of the polishing pad (1), wherein the polishing gap extends from the inner edge (B) as far as the outer edge (A), wherein the height of the polishing gap decreases linearly from the inner edge (B) to the outer edge (A), and wherein a thickness of at least one of the polishing pad covering the upper polishing plate and the polishing pad covering the lower polishing plate is increases from the inner edge (B) to the outer edge (A).

The method according to the invention used for achieving the object is described in detail below. The embodiments mentioned serve for elucidation, without restricting the scope of the method to these embodiments.

With the method according to the invention for simultaneous double-side polishing of at least one wafer composed of semiconductor material, edge rounding can be significantly reduced or even avoided by means of a combination of hard polishing pads having low compressibility with a specific shape

of the working gap, realized by means of suitable thickness profiles of the polishing pads.

Figure 1 shows the influence of the hardness and the compressibility of a polishing pad on the edge of a wafer composed of semiconductor material.
Figure 1a: In the case of a soft and compressible pad (1), adhesively bonded onto a polishing plate (8), the wafer (5) sinks somewhat into the working surface (2) of the polishing pad (1). As a result, higher forces act on the wafer (5) in the edge region of the wafer than in other regions of the wafer (5), such that the edge is rounded by increased material removal during polishing.

Patent claims:

1. A method for polishing at least one wafer (5) composed of semiconductor material having a front side and the rear side, comprising

at least one first polishing step by means of which the wafer (5) composed of semiconductor material is polished at a process temperature simultaneously on both sides on the front side and on the rear side between an upper and a lower polishing plate (8), which are each covered with a polishing pad (1) having a hardness of at least 80° Shore A and a compressibility of less than 2.5%, and the space between the upper and the lower surface (2) - which comes into contact with the wafer to be polished - of the polishing pads (1) forms a polishing gap,

wherein the polishing pad (1) has an outer edge (A) and an inner edge (B) adjacent to a center of the polishing pad (1),

wherein the polishing gap extends from the inner edge (B) as far as the outer edge (A), wherein the height of the polishing gap decreases linearly from the inner edge (B) to the outer edge (A), and

wherein a thickness of at least one of the polishing pad covering the upper polishing plate and the polishing pad covering the lower polishing plate is increases from the inner edge (B) to the outer edge (A).

2. The method as claimed in claim 1, wherein the difference in the height of the polishing gap between the inner and outer edges is 70 μm to 360 μm relative to one meter ring width, wherein the ring width is defined as the radial distance between the inner edge (B) of the polishing pad (1) and the

outer edge (A) of the polishing pad (1).

3. The method as claimed in claim 1, wherein the hardness of the polishing pad is in the range of 80° Shore A and 100° Shore A.

4. The method as claimed in any of claims 1 to 3, wherein the thickness of the polishing pad is in the range of 0.5 to 1.0 mm.

5. The method as claimed in any of claims 1 to 3, wherein the polishing pad is adhesively bonded onto the polishing plate.

6. The method as claimed in claim 5, wherein the polishing plate is heated to 40 to 50°C for the purpose of adhesively bonding the polishing pad.

7. The method as claimed in any of claims 1 to 3, wherein, during the first dressing, 20 - 100 μm are removed from a working layer (4) of the polishing pad (1) in a thickness direction of the working layer (4).

8. The method as claimed in any of claims 1 to 3, wherein the height of the polishing gap is lower at the outer edge (A) than at the inner edge (B).

9. The method as claimed in any of claims 1 to 3, wherein the double-side polishing is effected at a process temperature of 10°C to 50°C.

Patent claims:

1. A method for polishing at least one wafer (5) composed of semiconductor material having a front side and the rear side, comprising at least one first polishing step by means of which the wafer (5) composed of semiconductor material is polished at a process temperature simultaneously on both sides on the front side and on the rear side between an upper and a lower polishing plate (8), which are each covered with a polishing pad (1) having a hardness of at least 80° Shore A and a compressibility of less than 2.5%, and the distance between the upper and the lower surface (2) - which comes into contact with the wafer to be polished - of the polishing pads (1) forms a polishing gap, and this polishing gap extends from the inner edge (B) of the polishing pad (1) as far as the outer edge (A) of the polishing pad (1), wherein the height of the polishing gap at the inner edge (B) differs linearly from the height of the polishing gap at the outer edge (A).

2. The method as claimed in claim 1, wherein the difference in the height of the polishing gap between the inner and outer edges is 70 µm to 360 µm relative to one meter ring width, wherein the ring width is defined as the radial distance between the inner edge (B) of the polishing pad (1) and the outer edge (A) of the polishing pad (1).

3. The method as claimed in claim 1, wherein the hardness of the polishing pad is in the range of 80° Shore A and 100° Shore A.

4. The method as claimed in any of claims 1 to 3, wherein the thickness of the polishing pad is in the range of 0.5 to 1.0 mm.

5. The method as claimed in any of claims 1 to 4, wherein the polishing pad is adhesively bonded onto the polishing plate.

6. The method as claimed in claim 5, wherein the polishing plate is heated to 40 to 50°C for the purpose of adhesively bonding the polishing pad.

7. The method as claimed in any of claims 1 to 6, wherein, during the first dressing, 20 - 100 μm are removed from the working layer (4) of the polishing pad (1).

8. The method as claimed in any of claims 1 to 7, wherein the height of the polishing gap is lower at the outer edge (A) than at the inner edge (B).

9. The method as claimed in any of claims 1 to 8, wherein the height of the polishing gap decreases linearly from the inner edge (B) to the outer edge (A).

10. The method as claimed in any of claims 1 to 9, wherein the double-side polishing is effected at a process temperature of 10°C to 50°C.