

**TECHNIQUES FOR RAPID AND EFFICIENT INTERCALATION-DOPING OF LARGE-AREA
MULTI-LAYERED GRAPHENE SHEETS**

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CROSS-REFERENCE OF RELATED APPLICATIONS

[0001] This application references United States Patent Application No. 18/674,085, filed on 24-MAY-2024, and titled LOW-TEMPERATURE/BEOL-COMPATIBLE HIGHLY SCALABLE GRAPHENE SYNTHESIS TOOLS INCLUDING RETASKED TOOLS; United States Patent Application No. 18/655,087, filed on 03-MAY-2024, and titled LOW-TEMPERATURE/BEOL-COMPATIBLE HIGHLY SCALABLE GRAPHENE SYNTHESIS TOOL; United States Patent Application No. 18/607,380, filed on 15-MAR-2024, and titled GRAPHENE BEOL INTEGRATION INTERCONNECTION STRUCTURES; United States Patent Application No. 18/527,043, filed on 01-DE 2023, and titled LARGE-AREA WAFER-SCALE CMOS-COMPATIBLE 2D-MATERIAL INTERCALATION DOPING TOOLS, PROCESSES, AND METHODS, INCLUDING DOPING OF SYNTHESIZED GRAPHENE; United States Patent Application No. 17/863,232, filed on 12-JUL-2022, and titled LOW-TEMPERATURE/BEOL-COMPATIBLE HIGHLY SCALABLE GRAPHENE SYNTHESIS TOOL; United States Patent Application No. 17/857,954, filed on 05-JUL-2022, and titled LOW-TEMPERATURE/BEOL-COMPATIBLE HIGHLY SCALABLE GRAPHENE SYNTHESIS TOOL; United States Provisional Patent Application No. 63/441,766, filed on 27-JAN-2023, and titled LARGE-AREA/WAFER-SCALE CMOS-COMPATIBLE 2D-MATERIAL DOPING TOOLS, PROCESSES, AND METHODS, INCLUDING DOPING OF SYNTHESIZED GRAPHENE; United States Provisional Patent Application No. 63/457,362, filed on 05-APR-2023, and titled GRAPHENE BEOL INTEGRATION TECHNIQUES, METHODS, STRUCTURES, AND DEVICES; United States Provisional Patent Application No. 63/620,748, filed on 12-JAN-2024, and titled ADDITIONAL UTILITY OF A GRAPHENE SYNTHESIS TOOL; and United States Provisional Patent Application No. 63/218,498, filed on 06-JUL-2021, and titled WAFER-SCALE CMOS-COMPATIBLE GRAPHENE SYNTHESIS TOOL; as related

applications, the entire contents of the foregoing applications are hereby incorporated herein by reference.

[0002] Furthermore, this application claims priority to and the benefit of United States Patent Application No. 18/744,533, filed on 14-JUN-2024, and titled TECHNIQUES, METHODS, AND STRUCTURES FOR RAPID AND EFFICIENT INTERCALATION-DOPING OF LARGE-AREA MULTI- LAYERED GRAPHENE SHEETS FOR TRANSPARENT AND SEMI-TRANSPARENT CONDUCTOR APPLICATIONS, INCLUDING SOLAR CELLS AND DISPLAYS, which claims priority to United States Provisional Patent Application No. 63/618,862, filed on 08-JAN-2024, and titled TECHNIQUES, METHODS, AND STRUCTURES FOR RAPID AND EFFICIENT INTERCALATION-DOPING OF LARGE-AREA MULTI- LAYERED GRAPHENE SHEETS FOR TRANSPARENT CONDUCTOR APPLICATIONS, INCLUDING SOLAR CELLS AND DISPLAYS; and the entire contents of the foregoing applications are hereby incorporated herein by reference.

BACKGROUND

[0003] In many applications, including mainstream microelectronics (CMOS), often, the conductivity of atomically-thin two-dimensional (2D) layered materials including synthesized multi-layer graphene (MLG), or any multi-layered semiconductor material (such as molybdenum disulphide (MoS_2) or tungsten disulphide (WS_2)), needs to be modulated. Typically, this involves an increase in the carrier concentration of the electrons or the holes. This increase in the carrier concentration can be achieved through a process known as intercalation doping, which involves the insertion (via diffusion) of certain atoms, ions, or molecules into the host material (in the gap between the adjacent layers, as these are “Van der Waals materials” with no out-of-plane bonds) that induces charge transfer between the dopants (intercalants) and the layered material, for example, MLG.

[0004] Depending on the difference in the Fermi-level of the intercalants and the host material, n-type or p-type material with higher electrical conductivity can be engineered. See illustrations in, W. Liu, J. Kang and K. Banerjee, “Characterization of FeCl_3 intercalation doped CVD few-layer graphene,” IEEE Electron Device Letters, Vol. 37, No. 9, pp. 1246 - 1249, 2016.

[0005] Due to the geometry, for example, such as the layered structure of many 2D materials, intercalation doping may be utilized to minimize the bulk resistivity of the few or multiple stack material. Intercalation doping involves insertion of the dopant atoms/molecules through the sidewall faces of these materials via diffusion, which has been shown to make doping

possible for narrow geometries (line-widths) of the 2D materials. Acceleration of such doping processes via application of temperature and/or pressure or via other means can make the doping process production-capable and inexpensive.

[0006] Intercalation doping at relatively low temperatures (<450 °C) is needed in a wide range of applications covering microelectronics, optoelectronics, bioelectronics, quantum computing, antennas (5G/6G/terahertz) and many more to satisfy thermal budget requirements. For example, need for such a low-temperature doping of MLG nanoribbons (MLG NR) arises in several CMOS Back-End-Of-Line (BEOL) applications, particularly on-chip interconnects and inductors. BEOL interconnects must be effectively synthesized and doped under a strict thermal budget of < 450 °C to avoid any damage to the underlying active devices (e.g. transistors, diodes, etc. via increased diffusion of impurities).

[0007] Transparent conducting films or transparent electrodes (TE) are electrically conductive and optically transparent thin film materials. They are used in a variety of electronic devices, such as liquid crystal displays, OLED displays, photovoltaic, touchscreens, and other flexible/wearable electronic components. The global transparent conductive films market size was valued at \$4.9 billion in 2020, and is projected to reach \$12.9 billion by 2030 according to market research.

[0008] Current TE materials predominantly employ ITO (Indium Tin Oxide), which is expensive and suffer from limited flexibility. Intercalation-doped few-layer/multi-layer graphene (FLG/MLG) based electrodes offer excellent transparency along with low sheet resistance that is difficult to achieve with ITO or other TE materials (see Fig. 6 of W. Liu, J. Kang and K. Banerjee, "Characterization of FeCl₃ intercalation doped CVD few-layer graphene," IEEE Electron Device Letters, Vol. 37, No. 9, pp. 1246 - 1249, 2016).

[0009] However, intercalation doping of any relatively large area FLG/MLG sheet is an extremely time consuming process due to the slow diffusion based mechanism of intercalation. Although the intercalation process can be accelerated by applying a diffusion pressure and by increasing the temperature of the intercalation chamber, or via other means of accelerating the diffusion process, it can still take several hours.

[0010] This invention involves methods, processes, and structures that significantly reduce the intercalation diffusion time and also increases the efficiency with which large area FLG/MLG sheets can be doped (n-type or p-type) with any intercalant in the form of atoms, ions, or molecules.

[0011] Current intercalated sheets and structures of FLG/MLG employ pristine structures (squares, rectangles, circles, etc.) that allow intercalation only via the edges of the structures,

while this invention proposes methods, processes, and structures to artificially imprint narrow pathways/openings on the FLG/MLG *sheets* that can allow a multitude of intercalant diffusion conduits, thereby significantly reducing the intercalation time and increasing the intercalation efficiency.

[0012] Applications of the inventive embodiments and concepts presented herein may include; for example, such as TEs which may be employed for use in at least smartphones, tablets, notebooks, PCs, wearable devices displays, solar cells, and flexible electronics and can benefit from the improved intercalation process.

SUMMARY

[0013] In one aspect, a transparent or semi-transparent conducting thin film structure or pattern which facilitates the insertion of dopant atoms, ions, or molecules into layered 2D materials, the film structure including: a layered 2D material, an electrically isolative material, where the electrically isolative material is disposed below the layered 2D material, where the layered 2D material has at least one layer, where the layered 2D material is divided into islands of the 2D material, where separation of the islands of 2D material with respect to each other is greater than 0.5 nm and less than 1 meter, and where the islands of 2D material are intercalation doped with at least one dopant, and where the at least one dopant includes intercalation doping agents.

[0014] In another aspect, a transparent or semi-transparent conducting thin film structure or pattern which facilitates the insertion of dopant atoms, ions, or molecules into layered 2D materials, the film including: a layered 2D material, an electrically isolative material, where the electrically isolative material is disposed below the layered 2D material, where the layered 2D material is multilayered graphene, where the layered 2D material is divided into islands of the 2D material, where separation of the islands of 2D material with respect to each other is greater than 0.5 nm and less than 1 meter, and where the islands of 2D material are intercalation doped with at least one dopant, and where the at least one dopant includes intercalation doping agents.

[0015] And in another aspect, a transparent or semi-transparent conducting thin film structure or pattern which facilitates the insertion of dopant atoms, ions, or molecules into layered 2D materials, the film including: a layered 2D material, an electrically isolative material, where the electrically isolative material is disposed below the layered 2D material, where the layered 2D material is multilayered graphene, where the electrically isolative material is silicon dioxide, where the layered 2D material is divided into islands of the 2D material, where

separation of the islands of 2D material with respect to each other is greater than 0.5 nm and less than 1 meter, where the islands of 2D material are intercalation doped with at least one dopant, and where the at least one dopant includes intercalation doping agents.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] The present application can be best understood by reference to the following description taken in conjunction with the accompanying figures, in which like parts may be referred to by like numerals.

[0017] **Figure 1** is an exemplary top view illustration of intercalation doping of a FLG/MLG sheet with diffusion only through the edges, according to some embodiments.

[0018] **Figure 2** is an exemplary top view illustration of intercalation doping of an engineered FLG/MLG sheet with an etched narrow grid to allow diffusion through the edges as well as the etched regions, according to some embodiments.

[0019] The Figures described above are a representative set and are not exhaustive with respect to embodying the invention or inventions.

DESCRIPTION

[0020] Disclosed are a techniques, method, and structures to allow effective intercalation doping of 2D layered materials including FLG/MLG. The following description is presented to enable a person of ordinary skill in the art to make and use the various embodiments. Descriptions of specific devices, techniques, and applications are provided only as examples. Various modifications to the examples described herein will be readily apparent to those of ordinary skill in the art, and the general principles defined herein may be applied to other examples and applications without departing from the spirit and scope of the various embodiments.

[0021] Reference throughout this specification to "one embodiment," "an embodiment," "one example," or similar language means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the present invention. Thus, appearances of the phrases "in one embodiment," "in an embodiment," and similar language throughout this specification may, but do not necessarily, all refer to the same embodiment.

[0022] Furthermore, the described features, structures, or characteristics of the invention may be combined in any suitable manner in one or more embodiments. In the following description, numerous specific details are provided, such as examples of programming, software modules, user selections, network transactions, database queries, database structures, hardware modules, hardware circuits, hardware chips, etc., to provide a thorough understanding of embodiments of the invention. One skilled in the relevant art can recognize, however, that the invention may be practiced without one or more of the specific details, or with other methods, components, materials, and so forth. In other instances, well-known structures, materials, or operations are not shown or described in detail to avoid obscuring aspects of the invention.

[0023] The schematic flow chart diagrams included herein are generally set forth as logical flow chart diagrams. As such, the depicted order and labeled steps are indicative of one embodiment of the presented method. Other steps and methods may be conceived that are equivalent in function, logic, or effect to one or more steps, or portions thereof, of the illustrated method. Additionally, the format and symbols employed are provided to explain the logical steps of the method and are understood not to limit the scope of the method. Although various arrow types and line types may be employed in the flow chart diagrams, they are understood not to limit the scope of the corresponding method. Indeed, some arrows or other connectors may be used to indicate only the logical flow of the method. For instance, an arrow may indicate a waiting or monitoring period of unspecified duration between enumerated steps of the depicted method. Additionally, the order in which a particular method occurs may or may not strictly adhere to the order of the corresponding steps shown.

DEFINITIONS

[0024] Back-End-Of-Line (BEOL) is the second portion of IC fabrication where interconnects and other passive circuit elements are formed on the wafer (after the active devices have been fabricated) over the individual devices (primarily the transistors) in multiple layers (i.e., the metallization layers) separated by intra-layer and/or inter-layer insulators.

[0025] Complementary metal–oxide–semiconductor (CMOS) is a type of metal–oxide–semiconductor field-effect transistor (MOSFET) fabrication process that uses complementary and often electrically symmetrical pairs of p-type and n-type MOSFETs for implementing logic, memory, and other functions.

[0026] Grain boundary (GB) is the interface between two grains and/or crystallites in a polycrystalline material.

[0027] Graphene is an allotrope of carbon consisting of a single layer of atoms arranged in a two-dimensional honeycomb lattice.

[0028] Graphene nanoribbons (GNRs) are strips of graphene with width less than one-hundred (100) nm.

[0029] Multilayer Graphene nanoribbons (MLGNRs) are strips of MLG with a width less than about one-hundred (100) nm.

[0030] Graphite is a layered crystalline form of the element carbon with its atoms arranged and covalently bonded forming a hexagonal structure within the layers.

[0031] Intercalants are atoms, ions, or molecules utilized to dope a layered material or structure.

[0032] Intercalation doping: Intercalation is a process when a molecule or ion inserts reversibly *between* the layers of a compound (such as potassium ions between graphite layers). N-type intercalation dopants (or n-type intercalants) will transfer electrons to the host material or compound. P-type intercalation dopants (or p-type intercalants) will transfer holes to the host material or compound. Both dopant types will increase the charge carrier density and consequently the electrical conductivity of the material.

[0033] Intercalation doping agents: There are many in the literature. Specific to graphene is recent work by Kaustav Banerjee, *et al.*; for example, J. Jiang, Jae Hwan Chu, and Kaustav Banerjee, "CMOS-Compatible Doped-Multilayer-Graphene Interconnects for Next-Generation VLSI," IEDM 2018, pp. 799-802, 34.5.1-4; J. Jiang, *et al.*, "Intercalation doped multilayer-graphene-nanoribbons for next-generation interconnects," *Nano Letters*, vol. 17, no. 3, pp. 1482-1488, 2017; and J. Kang *et al.*, "On-chip intercalated-graphene inductors for next-generation radio frequency electronics," *Nature Electronics*, vol. 1, no. 1, pp. 46-51, 2018.

[0034] Wafer: is a thin slice of semiconductor (e.g. a crystalline silicon, germanium) used for the fabrication of integrated circuits, etc.

[0035] Silicon dioxide is an oxide of silicon and an insulator with the chemical formula SiO₂.

[0036] Van der Waals materials: materials with strong covalent bonds in the in-plane directions and relatively weak van der Waals bonds in the out-of-plane direction.

DESCRIPTION Continued

[0037] This scheme, process, methods, devices, and structures are not limited to only intercalation doping of FLG/MLG, rather, intercalation doping of many other layered materials and structures can be accomplished by the concepts disclosed.

[0038] As illustrated in **Figure 1**, a conventional intercalation doping process of an FLG/MLG sheet 100 involving intercalant or intercalants 110 diffusion (represented as arrows for clarity and explanation) only through the edges 120 of the FLG/MLG sheet 100 is described. FLG/MLG sheet 100 may include, for example, a few-layer or multi-layer graphene sheet where the distance from edge to edge is so large that effective doping of at least the majority of the sheet volume cannot be obtained in a reasonable amount of time in an intercalation process. Being an edge confined process, intercalation doping can suffer from long processing times as well as not being uniform or efficient. Note that as the thickness (or number of layers) of the MLG increases, there are more pathways along the edges, however, for most TE applications the number of graphene layers is typically < 5 due to transparency requirements.

[0039] As illustrated in **Figure 2**, FLG/MLG sheet 200 may be preprocessed before intercalation doping is processed. An intercalation scheme may include where a grid or grid-like structure including edge openings 210 may be etched on FLG/MLG sheet 200 thereby allowing diffusion of Intercalants 220 through the 'new' edges of FLG/MLG sheet 200 - etched regions edge openings 210 - as well as the conventional edges of FLG/MLG sheet 200. This 'divide and conquer' scheme results in much faster intercalation coverage per unit area of the sheet, which significantly accelerates the intercalation process, thereby reducing the time to fully intercalate (stage-1 intercalation) the entire sheet and also makes the intercalation doping of a large-area sheet more uniform and efficient. Edge openings 210 may include shapes and design layouts such as the grids and grid-like structures edge openings 210 illustrated in Figure 2, and may include non-uniform spacing of edge openings 210. In addition, edge openings 210 may have a 'diagonal' orientation, a chevron pattern, semi and/or complete circle shape(s), and so on, depending on design, engineering, and efficiency considerations. If the desire is to provide a complete doping of the area/volume of the target FLG/MLG sheet 200, then care must be taken to ensure that for the given intercalant 220 species and intercalant diffusion acceleration (temperature and/or pressure, or other means of accelerating intercalant diffusion) utilized, that complete doping (to the desired level) is achieved.

[0040] The size of the individual grid (or grid density) can be varied, and the width of the grid lines (both vertical and horizontal) can also be varied (from a few nanometers to 10s, 100s, or 1000s of nanometers) depending on the target transparency and sheet resistance values. Since the typical 'van der Waals gap' between adjacent graphene layers in the FLG/MLG is < 0.5 nm, even a few nanometer wide etched grid regions can allow intercalation to take place. Moreover, the efficiency of the intercalation doping in the disclosed scheme can outweigh any impact of the grid lines on the effective sheet resistance of the FLG/MLG sheet 200 or resulting full

structure, such as the previous discussed TEs. Such narrowly etched lines will also have minimal impact on the optical properties of the FLG/MLG sheet.

[0041] The FLG/MLG sheet 200 can be directly synthesized or transferred to a desired substrate before fabricating the grid. The etched regions can be defined using oxygen-plasma and passivated after intercalation to prevent any out-diffusion. This scheme can be employed to effectively create novel engineered transparent conductor materials with tunable properties of transparency and sheet resistance.

[0042] See at least patent applications 63/123,587 and PCT/US21/61361 and at least papers J. Jiang, *et al.*, "Intercalation doped multilayer-graphene-nanoribbons for next generation interconnect," *Nano Letters*, 17(3), pp. 1482-1488, 2017.; and J. Jiang, *et al.*, "All-carbon interconnect scheme integrating graphene wires and carbon-nanotube-vias," *IEEE IEDM*, pp. 14.3.1-14.3.4, 2017.; and J. Jiang, *et al.*, "CMOS-Compatible Doped-Multilayer-Graphene Interconnects for Next-Generation VLSI," *IEEE IEDM*, pp. 34.5.1-34.5.4, 2018.; and K. Agashiwala, *et al.*, "Reliability and Performance of CMOS-Compatible Multi-Level Graphene Interconnects Incorporating Vias" *IEEE IEDM*, 2020; and K. Agashiwala, *et al.*, "Demonstration of CMOS-Compatible Multi-Level Graphene Interconnects with Metal Vias" *IEEE Transactions on Electron Devices*, vol. 68, No. 4, April 2021, pp. 2063-2091.; the entirety of all of the forgoing are incorporated by reference.

CONCLUSION

[0043] Although the present embodiments have been described with reference to specific example embodiments, various modifications and changes can be made to these embodiments without departing from the broader spirit and scope of the various embodiments. Accordingly, the specification and drawings are to be regarded in an illustrative rather than a restrictive sense.

CLAIMS

1. A transparent or semi-transparent conducting thin film structure or pattern which facilitates the insertion of dopant atoms, ions, or molecules into layered 2D materials, the film structure comprising:

a layered 2D material,

an electrically isolative material,

wherein said electrically isolative material is disposed below said layered 2D material,

wherein said layered 2D material has at least one layer,

wherein said layered 2D material is divided into islands of said 2D material,

wherein separation of said islands of 2D material with respect to each other is greater than 0.5 nm and less than 1 meter, and

wherein said islands of 2D material are intercalation doped with at least one dopant, and

wherein said at least one dopant comprises intercalation doping agents.

2. The film structure according to claim 1,

wherein said intercalation doped means when any number of atoms, molecules or ions insert reversibly between layers of said layered 2D materials.

3. The film structure according to claim 1,

wherein said layered 2D material has a maximum of 100 layers.

4. The film structure according to claim 1,

wherein said layered 2D material is multilayered graphene.

5. The film structure according to claim 1,

wherein said electrically isolative material is silicon dioxide.

6. The film structure according to claim 1,

wherein said separation between islands is equal to or greater than 10 times the diameter of a molecule of said intercalant dopant.

7. The film structure according to claim 1,
wherein said islands of 2D material have a maximum width or length of 5 micro-meters.
8. A transparent or semi-transparent conducting thin film structure or pattern which facilitates the insertion of dopant atoms, ions, or molecules into layered 2D materials, the film comprising:
a layered 2D material,
an electrically isolative material,
wherein said electrically isolative material is disposed below said layered 2D material,
wherein said layered 2D material is multilayered graphene,
wherein said layered 2D material is divided into islands of said 2D material,
wherein separation of said islands of 2D material with respect to each other is greater than 0.5 nm and less than 1 meter, and
wherein said islands of 2D material are intercalation doped with at least one dopant, and
wherein said at least one dopant comprises intercalation doping agents.
9. The film structure according to claim 8,
wherein said intercalation doped means when any number of atoms, molecules or ions insert reversibly between layers of said layered 2D materials.
10. The film structure according to claim 8,
wherein said layered 2D material has a maximum of 100 layers.
11. The film structure according to claim 8,
wherein said insertion dopant atoms, ions, or molecules into said layered 2D materials is accelerated by pressure, temperature, or electrical bias.
12. The film structure according to claim 8,
wherein said electrically isolative material is silicon dioxide.
13. The film structure according to claim 8,

wherein said separation between islands is equal to or greater than 10 times the diameter of a molecule of said intercalant dopant.

14. The film structure according to claim 8,

wherein said islands of 2D material have a maximum width or length of 5 micro-meters.

15. A transparent or semi-transparent conducting thin film structure or pattern which facilitates the insertion of dopant atoms, ions, or molecules into layered 2D materials, the film comprising:

a layered 2D material,

an electrically isolative material,

wherein said electrically isolative material is disposed below said layered 2D material,

wherein said layered 2D material is multilayered graphene,

wherein said electrically isolative material is silicon dioxide,

wherein said layered 2D material is divided into islands of said 2D material,

wherein separation of said islands of 2D material with respect to each other is greater than 0.5 nm and less than 1 meter,

wherein said islands of 2D material are intercalation doped with at least one dopant, and

wherein said at least one dopant comprises intercalation doping agents.

16. The film structure according to claim 15,

wherein said intercalation doped means when any number of atoms, molecules or ions insert reversibly between layers of said layered 2D materials.

17. The film structure according to claim 15,

wherein said layered 2D material has a maximum of 100 layers.

18. The film structure according to claim 15,

wherein said insertion dopant atoms, ions, or molecules into said layered 2D materials is accelerated by pressure, temperature, or electrical bias.

19. The film structure according to claim 15,

wherein a total edge perimeter of said islands of 2D material is at least 10 times greater than an original perimeter of said 2D layered material with no islands.

20. The film structure according to claim 15,

wherein said islands of 2D material have a maximum width or length of 5 micro-meters.