NROM FLASH MEMORY DEVICES ON ULTRATHIN SILICON

TECHNICAL FIELD OF THE INVENTION

The present invention relates generally to memory devices and in particular the present invention relates to nitride read only memory flash memory devices.

BACKGROUND OF THE INVENTION

The increased speed and capability of computers and other electronic devices requires better performance from the integrated circuits that make up a device. One way to make the integrated circuits faster is to reduce the size of the transistors that make up the device. However, as transistors are made smaller and faster, delays through the connections between the transistors becomes greater in relation to the speed of the transistor.

An alternative technique to speed up integrated circuits is to use alternative semiconductors. For example, silicon-on-insulator (SOI) technology provides a 25 – 35% performance increase over equivalent CMOS technologies. SOI refers to placing a thin layer of silicon on top of an insulator such as silicon oxide or glass. The transistors would then be built on this thin layer of SOI. The SOI layer reduces the capacitance of the transistors so that they operate faster.

Figure 1 illustrates a typical prior art SOI semiconductor. The transistor is formed in the silicon layer 101 that is over the insulator 102. The insulator is formed on top of the substrate 103. Within the silicon layer 101, the drain/source regions 105 and 106 are formed. The gate 107 is formed above the partially depleted channel 109. A floating body 110 is within the depleted region 112 and results from the partial depletion.

SOI technology, however, imposes significant technical challenges. The silicon film used for SOI transistors must be perfect crystalline silicon. The insulator layer, however, is not crystalline. It is very difficult to make perfect crystalline silicon-on-oxide or silicon with other insulators since the insulator layer's crystalline properties are so different from the pure silicon. If perfect crystalline silicon is not obtained, defects will find their way onto the SOI film. This degrades the transistor performance.

Additionally, floating body effects in partially depleted CMOS devices using SOI technology are undesirable in many logic and memory applications. The floating bodies

cause threshold voltages and switching speeds to be variable and complex functions of the switching history of a particular logic gate. In dynamic logic and DRAM memories, the floating bodies cause excess charge leakage and short retention times that can cause data loss. In conventional flash memories and NROM devices, the floating bodies cause reduced erase fields and slower erase times.

For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for a way to eliminate floating body effects in CMOS devices incorporating SOI technology.

SUMMARY

The above-mentioned problems with eliminating floating body effects and other problems are addressed by the present invention and will be understood by reading and studying the following specification.

The present invention encompasses an NROM transistor having an ultra-thin silicon-on-insulator substrate. The silicon has two doped source/drain regions separated by a normally fully depleted body region. The doped regions are a different conductivity than the substrate.

An oxide layer is formed above each of the source/drain regions. A gate insulator is formed over the body region and oxide layer. The gate insulator is capable of storing a plurality of charges. A control gate is formed on the gate insulator.

Further embodiments of the invention include methods and apparatus of varying scope.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows a cross-sectional view of a typical prior art SOI semiconductor.

Figure 2 shows a cross-sectional view of one embodiment for a planar NOR NROM cell using ultra-thin SOI.

Figure 3 shows a cross-sectional view of one embodiment of two vertical NOR NROM cells of the present invention using ultra-thin SOI.

Figure 4 shows a cross-sectional view of another embodiment of two vertical NOR NROM cells of the present invention using ultra-thin SOI.

Figure 5 shows an electrical equivalent circuit of a NOR NROM flash memory array of the present invention.

Figure 6 shows a cross-sectional view of yet another alternate embodiment of a vertical NOR NROM memory array of the present invention using ultra-thin SOI.

Figure 7 shows an electrical equivalent circuit of a NOR NROM flash memory array of the present invention in accordance with the embodiment of Figure 6.

Figure 8 shows a cross-sectional view of one embodiment of a planar NAND NROM cell of the present invention using ultra-thin SOI.

Figure 9 shows a cross-sectional view of one embodiment of two vertical NAND NROM cells of the present invention using ultra-thin SOI.

Figure 10 shows an electrical equivalent circuit of a NAND NROM flash memory array of the present invention in accordance with the embodiment of Figure 9.

Figure 11 shows a block diagram of one embodiment of an electronic system of the present invention.

DETAILED DESCRIPTION

In the following detailed description of the invention, reference is made to the accompanying drawings that form a part hereof and in which is shown, by way of illustration, specific embodiments in which the invention may be practiced. In the drawings, like numerals describe substantially similar components throughout the several views. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope of the present invention. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims and equivalents thereof.

Figure 2 illustrates a cross-sectional view of one embodiment of a planar NROM cell using ultra-thin silicon-on-insulator (SOI) technology. The NROM flash memory cell of Figure 2 is a NOR array cell with virtual ground bit lines.

The NROM flash memory cell is comprised of the silicon layer 201 on the insulator 202. The silicon 201 in an ultra-thin SOI cell is less than 100 nm (1000 Å). This layer 201 is comprised of two source/drain areas 220 and 221 that act as bit lines 220 and 221. In one embodiment, these areas 220 and 221 are n-type material. Alternate embodiments use p-type material if the substrate is an n-type material.

The body region 200 between the bit lines 220 and 221 is normally fully depleted in ultra-thin SOI. The body region 200 is comprised of ionized acceptor impurities 203 and ionized donor impurities 205. Two oxide areas 210 and 211 are deposited on the silicon 201.

A gate insulator 207, in one embodiment, is a composite structure of oxide-nitride-oxide (ONO) formed between the control gate 230 and the silicon layer 201. The control gate 230, in one embodiment, is a polysilicon material and extends in the 'x' direction in the NOR flash cell embodiment. The nitride layer 225 has two charge storage areas 231 and 232.

Alternate embodiments of the present invention use other gate insulators besides the ONO composite structure shown. These structures may include oxide-nitride-aluminum oxide composite layers, oxide- aluminum oxide-oxide composite layers, oxide, silicon oxycarbide-oxide composite layers as well as other composite layers.

In still other alternate embodiments, the gate insulator may include thicker than normal silicon oxides formed by wet oxidation and not annealed, silicon rich oxides with inclusions of nanoparticles of silicon, silicon oxynitride layer that are not composite layers, silicon rich aluminum oxide insulators that are not composite layers, silicon oxycarbide insulators that are not composite layers, silicon oxide insulators with inclusions of nanoparticles of silicon carbide, in addition to other non-stoichiometric single layers of gate insulators of two or more commonly used insulator materials such as Si, N, Al, Ti, Ta, Hf, Zr, and La.

Figure 3 illustrates a cross-sectional view of one embodiment of two vertical NOR NROM cells 350 and 351 of the present invention using ultra-thin SOI. The vertical embodiment provides for higher density memory arrays.

The cells 350 and 351 of Figure 3 each have source/drain areas 330 and 331 that operate as bit lines and are comprised of n+ doped silicon. Alternate embodiments use p-type material if the substrate is comprised of n-type material. Additional source/drain areas 320

and 321 for each transistor are formed at the top of a vertical oxide pillar 310. The left transistor 350 uses source/drain areas 320 and 331 while the right transistor uses source/drain areas 321 and 330. The upper source/drain areas 320 and 321 are separated by a grain boundary but are electrically coupled. The vertical oxide pillar 310 is an insulator between the two transistors 350 and 351.

Vertical epitaxial regrowth is used to provide amorphous layers of ultra-thin silicon 300 and 301 along the sidewalls of the vertical oxide pillar 310. These layers are the ultra-thin silicon (i.e., < 100 nm) body regions 300 and 301 and are normally fully depleted. The direction of thickness of the silicon body region 300 and 301 is illustrated in each region. The left ultra-thin silicon body region is part of the left transistor 350 while the right body region 300 is part of the right transistor 351.

The gate insulator layer 307, in one embodiment, is a composite ONO structure. Alternate embodiments of this layer 307 are disclosed above. The control gate 330 is formed above this insulator layer 307 and is common to both transistors 350 and 351 such that it acts as a word line in a memory array. In one embodiment, the control gate 330 is a polysilicon material.

Figure 4 illustrates a cross-sectional view of another embodiment of two vertical NOR NROM cells of the present invention using ultra-thin SOI. This embodiment has an architecture that is substantially similar to the embodiment of Figure 3 in that the ultra-thin silicon body regions 400 and 401 are formed by epitaxial regrowth along the sidewalls of the oxide pillar 410. The top source/drain areas 420 and 421 are formed at the top of the oxide pillar 410 and the common poly control gate 405 is formed over the gate insulator 420 coupling both transistors 450 and 451 by a word line.

However, in the embodiment of Figure 4, the bottom oxide layer 402 and 404 of the gate insulator 420 is thicker in the trench than in the previous embodiment. Additionally, the two source/drain areas of Figure 3 are replaced by a single n+ source/drain region 430 that is isolated between the portions of the thicker oxide layer. \

Figure 5 illustrates an electrical equivalent circuit of a NOR NROM flash memory array of the present invention. This circuit can represent the planar embodiments of the present invention as well as the vertical embodiment of Figure 3.

The control gate 501 crosses all of the devices 510 – 512 in the array. The n+ source/drain regions 503 and 504 are used as virtual ground data or bit lines. As is well known in the art, the bit lines of the array are coupled to a sense amplifier in order to read data from the cells 510 – 512. The control gate 501 is the word line used to select the cells 510 – 512.

Figure 6 illustrates a cross-sectional view of yet another alternate embodiment of a vertical NOR NROM memory array of the present invention using ultra-thin SOI. This figure illustrates four vertical transistors 650 – 653. For purposes of clarity, only the transistors formed around the first oxide pillar 632 are described. The remaining transistors are substantially identical in structure and operation.

As in previous embodiments, the two ultra-thin silicon body regions 608 and 609 are formed by epitaxial regrowth along the sidewalls of the oxide pillar 632. The gate insulator layers 601 and 602 are formed alongside of the silicon body regions 608 and 609. The n+ polysilicon gate structures 630 and 631 for each transistor 650 and 651 are then formed on the insulator layers 601 and 602.

The nitride layers 603 and 604 provide two charge storage areas 610 and 611 for each transistor 650 - 653. In the trench area, the lower oxide layer 605 has a thicker composition than the rest of the gate insulator layer. The above cells 650 – 653 are formed on a lower n+ region 620 on the substrate that acts as a common source/drain area, depending on the direction that each transistor is biased.

The upper n+ regions 660 and 661 are the second common source/drain area for each transistor 650 and 651. The upper n+ region 660 and 661 of each transistor is coupled to other transistors in the array by a bonding wire 640 or other conductive device.

Figure 7 illustrates an electrical equivalent circuit of a NOR NROM flash memory array of the present invention in accordance with the embodiment of Figure 6. This figure illustrates the respective cells 650 – 653 as described in Figure 6 above.

The control gates 701 – 704 are coupled to other cells in the array and act as word lines. Two of these control gates 701 – 704 are illustrated in Figure 6 as 630 and 631. The top common source/drain areas 660 and 661 are shown as virtual ground or data bit line 709 while the common source/drain area 620 is shown as virtual ground or data bit line 708.

Figure 8 illustrates a cross-sectional view of one embodiment of a planar NAND NROM cell of the present invention using ultra-thin SOI. This embodiment is comprised of the two source/drain regions 803 and 804 with the fully depleted body region 801 in the ultra-thin SOI. The two oxide regions 807 and 808 are formed above the n+ areas and the gate insulator 805 is formed over this architecture. In one embodiment, the gate insulator 805 is a composite ONO layer but can be any other type of material including those described above.

The control gate 806 is formed above the gate insulator 805. In the NAND embodiment, the gate 806 extends in the 'z' direction instead of the 'x' direction as in the NOR embodiment.

Figure 9 illustrates a cross-sectional view of one embodiment of two vertical NAND NROM cells 910 and 911 of the present invention using ultra-thin SOI. Each transistor 910 and 91 1 is comprised of a source/drain region 905 and 906 formed in a p-type substrate material. Second source/drain regions 920 and 921 are formed on top of the oxide pillar 930 and separated by the grain boundary while still electrically coupled. The source/drain regions 905, 906, 920, and 921 function as virtual ground bit lines/data lines.

Epitaxial regrowth is used to grow ultra-thin silicon body regions 901 and 902 on the sidewalls of the oxide pillar 930. As in previous embodiments, these regions 901 and 902 are each less than 100 nm thick.

The gate insulator 950 is formed on top of the transistors 910 and 911. In one embodiment, the gate insulator 950 is an ONO composite layer. Alternate embodiments for the composition of this layer have been illustrated previously.

Control gates 907 and 908 for each transistor 910 and 911 respectively are formed from a polysilicon material on each side of the gate insulator 950. The control gates 907 and 908 are coupled to other transistors to act as word lines.

Figure 10 illustrates an electrical equivalent circuit of a NAND NROM flash memory array of the present invention in accordance with the embodiment of Figure 9. The two transistors 910 and 911 of Figure 9 are shown.

The n+ source/drain connection 1005 of Figure 10 corresponds to the two source/drain regions 920 and 921 of Figure 9. The word lines 1001 and 1002 of Figure 10 correspond to the control gate 907 and 908 respectively of Figure 9. The source/drain regions

905 and 906 formed in the substrate of Figure 9 correspond to the source/drain connections 1009 and 1007 of Figure 10.

The above embodiments are illustrated as n-channel type transistors. However, one of ordinary skill in the art will understand that the conductivity types can be reversed by altering the doping types such that the present invention is equally applicable to include structures NROM structures having ultra-thin silicon, p-channel type transistors.

The masking and etching steps used to form the ultra-thin silicon NROM flash memory cells of the present invention are not discussed in detail. The various steps required to form the above-described architectures are well known by those skilled in the art.

Figure 11 illustrates a functional block diagram of a memory device 1100 that can incorporate the ultra-thin SOI flash memory cells of the present invention. The memory device 1100 is coupled to a processor 1110. The processor 1110 may be a microprocessor or some other type of controlling circuitry. The memory device 1100 and the processor 1110 form part of an electronic system 1120. The memory device 1100 has been simplified to focus on features of the memory that are helpful in understanding the present invention.

The memory device includes an array of flash memory cells 1130. In one embodiment, the memory cells are NROM flash memory cells and the memory array 1130 is arranged in banks of rows and columns. The control gates of each row of memory cells is coupled with a wordline while the drain and source connections of the memory cells are coupled to bitlines. As is well known in the art, the connection of the cells to the bitlines depends on whether the array is a NAND architecture or a NOR architecture.

An address buffer circuit 1140 is provided to latch address signals provided on address input connections A0-Ax 1142. Address signals are received and decoded by a row decoder 1144 and a column decoder 1146 to access the memory array 1130. It will be appreciated by those skilled in the art, with the benefit of the present description, that the number of address input connections depends on the density and architecture of the memory array 1130. That is, the number of addresses increases with both increased memory cell counts and increased bank and block counts.

The memory device 1100 reads data in the memory array 1130 by sensing voltage or current changes in the memory array columns using sense/buffer circuitry 1150. The sense/buffer circuitry, in one embodiment, is coupled to read and latch a row of data from the

memory array 1130. Data input and output buffer circuitry 1160 is included for bi-directional data communication over a plurality of data connections 1162 with the controller 1110). Write circuitry 1155 is provided to write data to the memory array.

Control circuitry 1170 decodes signals provided on control connections 1172 from the processor 1110. These signals are used to control the operations on the memory array 1130, including data read, data write, and erase operations. The control circuitry 1170 may be a state machine, a sequencer, or some other type of controller.

Since the NROM memory cells of the present invention use a CMOS compatible process, the memory device 1100 of Figure 11 may be an embedded device with a CMOS processor.

The flash memory device illustrated in Figure 11 has been simplified to facilitate a basic understanding of the features of the memory. A more detailed understanding of internal circuitry and functions of flash memories are known to those skilled in the art.

CONCLUSION

In summary, the NROM flash memory cells of the present invention utilize ultra-thin SOI to provide a fully depleted body region. This eliminates the undesirable floating body effects experienced by partially depleted CMOS devices.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement that is calculated to achieve the same purpose may be substituted for the specific embodiments shown. Many adaptations of the invention will be apparent to those of ordinary skill in the art. Accordingly, this application is intended to cover any adaptations or variations of the invention. It is manifestly intended that this invention be limited only by the following claims and equivalents thereof.

What is claimed is:

1. An NROM transistor comprising:
an ultra-thin silicon-on-insulator layer having two source/drain regions separated by a normally fully depleted body region;
an oxide layer formed above each of the source/drain regions;
a gate insulator formed over the body region and oxide layer, the gate insulator capable of storing a plurality of charges; and
a control gate formed on the gate insulator.

2. The transistor of claim 1 wherein the gate insulator is an oxide-nitride-oxide composite structure.

3. The transistor of claim 1 wherein the gate insulator layer is a composite layer comprised of one of an oxide-nitride-aluminum oxide composite layer, an oxide-aluminum oxide-oxide composite layer, or an oxide-silicon oxycarbide-oxide composite layer.

4. The transistor of claim 1 wherein the gate insulator layer is a non-composite layer comprised of one of silicon oxides formed by wet oxidation and not annealed, silicon-rich oxides with inclusions of nanoparticles of silicon, silicon oxynitride layers, silicon-rich aluminum oxide insulators, silicon oxycarbide insulators, or silicon oxide insulators with inclusions of nanoparticles of silicon carbide.

5. The transistor of claim 1 wherein the gate insulator is comprised of non-stoichiometric single layers of two or more of silicon, nitrogen, aluminum, titanium, tantalum, hafnium, lanthanum, or zirconium.

6. The transistor of claim 1 wherein the transistor has a planar structure.

7. The transistor of claim 1 wherein the transistor has a NAND architecture.

8. The transistor of claim 1 wherein the transistor has a NOR architecture.

9. An NROM flash memory cell comprising:
a substrate comprising an insulator layer and a silicon-on-insulator layer that has a thickness less than 100 nm, the silicon-on-insulator layer comprising two source/drain regions separated by a normally fully depleted body region;
an oxide layer formed above each of the source/drain regions;
a composite gate insulator formed over the body region and oxide layer, the gate insulator having a nitride layer capable of storing a first charge when the cell is operated in a first direction and a second charge when the cell is operated in a second direction; and
a control gate formed on the composite gate insulator.

10. The cell of claim 9 wherein the control gate is comprised of a polysilicon material.

11. The cell of claim 9 wherein a first source/drain regions operates as a drain region when the cell is operated in the first direction and as a source region when the cell is operated in the second direction.

12. A vertical NROM flash memory array comprising
a substrate having a first plurality of source/drain regions;
an oxide pillar extending outward from the substrate;
a plurality of ultra-thin silicon body regions, each comprising epitaxial regrowth of silicon along opposite sidewalls of the oxide pillar, each body region extending vertically from a different source/drain region;
a second plurality of source/drain regions formed on the oxide pillar, each source/drain region coupled to a different body region;
an insulator layer formed over the first plurality of source/drain regions, the plurality of body regions, and the second plurality of source/drain regions; and
a control gate formed over the insulator layer.

13. The array of claim 12 wherein a first transistor of the memory array is comprised of a first source/drain region from the first plurality of source/drain regions, a first ultra-thin silicon body region, a first source/drain region from the second plurality of

source/drain regions, a portion of the insulator layer over the first silicon body region, and a portion of the control gate over the portion of the insulator layer.

14. The array of claim 12 wherein the insulator layer is comprised of a composite oxide-nitride-oxide structure.

15. The array of claim 14 wherein the lower oxide layer has a greater thickness in a trench on either side of the oxide pillar than a remaining portion formed around the oxide pillar.

16. The array of claim 15 wherein the first plurality of source/drain regions is isolated between each trench.

17. A vertical NROM flash memory array comprising

a substrate having a lower source/drain region;

an oxide pillar extending outward from the substrate above the lower source/drain region;

a plurality of ultra-thin silicon body regions, each comprising epitaxial regrowth of silicon along opposite sidewalls of the oxide pillar, each body region extending vertically from each side of the lower source/drain region;

an upper source/drain region formed on the oxide pillar, each side of the upper source/drain region coupled to a different body region;

an insulator layer formed around either side of the lower source/drain region, the plurality of body regions, and the upper source/drain region, portions of the insulator layer on each side of the lower source/drain region having a greater thickness than the remaining insulator layer such that the lower source/drain region is isolated between the thicker insulator layer portions; and

a control gate formed over the insulator layer.

18. The memory array of claim 17 wherein the thicker insulator layer portions are a lower oxide layer.

19. A vertical NROM flash memory array comprising:

a substrate having a doped region of a different conductivity type than the substrate extending along the substrate, the doped region acting as a first source/drain region;

a plurality of oxide pillars extending from the first source/drain region;

a plurality of ultra-thin silicon body regions each formed along an opposing sidewall of an oxide pillar, each ultra-thin silicon body region being fully depleted;

a polysilicon material formed on top of each oxide pillar and each body region, the polysilicon material acting as a second source/drain region and having the same conductivity type as the first source/drain region;

an oxide layer formed over the substrate, body regions, and second source/drain regions such that the oxide layer has a greater thickness along the substrate than in other areas;

a nitride-oxide layer formed over the oxide layer only on the opposing sides of the oxide pillar; and

a polysilicon control gate formed over the nitride-oxide layer.

20. The memory array of claim 19 and further including a conductive wire coupling the second source/drain regions on each oxide pillar.

21. The memory array of claim 19 wherein the first and second source/drain regions are n+ type conductive material.

22. The memory array of claim 19 wherein the array has a NOR type architecture.

23. An electronic system comprising:

a processor that generates control signals for the system; and

a memory array coupled to the processor and having a plurality of memory cells comprising:

an ultra-thin silicon-on-insulator layer having two source/drain regions separated by a normally fully depleted body region;

an oxide layer formed above each of the source/drain regions;

a gate insulator formed over the body region and oxide layer, the gate insulator capable of storing a plurality of charges; and

a control gate formed on the gate insulator.

24. A method for forming an array of NROM flash memory cells, the method comprising:
forming a plurality of doped regions in an ultra-thin silicon-on-insulator, the silicon-on-insulator having a fully depleted body region;
forming an oxide layer above each of the plurality of doped regions;
forming a gate insulator layer over the doped regions and the fully depleted body region; and
forming a polysilicon control gate over the gate insulator layer.

25. The method of claim 24 wherein forming the gate insulator comprises forming an oxide-nitride-oxide layer.

26. The method of claim 24 wherein the polysilicon control gate is formed such that the array is a NOR flash memory array.

27. The method of claim 24 wherein the polysilicon control gate is formed such that the array is a NAND flash memory array.

28. A method for forming a memory array comprising a plurality of vertical NROM memory cells, the method comprising:
forming a first plurality of doped regions in a substrate such that a gap exists between each doped region, the doped regions having a different conductivity type than the substrate;
forming an oxide pillar over the gap between the doped regions;
forming an ultra-thin silicon body region by epitaxial regrowth extending from each doped region along opposing sidewalls of the oxide pillar;
forming a second plurality of doped regions in a polysilicon material over the oxide pillar and body regions such that the doped regions over the pillar are electrically coupled and have the same conductivity type as the first plurality of doped regions;
forming a gate insulator layer over the first plurality of doped regions, the body regions, and the second plurality of doped regions; and

forming a polysilicon control gate area over the gate insulator adjacent to each of the body regions.

29. The method of claim 28 wherein the forming of the polysilicon control gate area includes forming the control gate as a continuous layer over the gate insulator.

30. A method for forming a memory array comprising a plurality of vertical NROM memory cells, the method comprising:

forming a first plurality of doped regions in a substrate, the doped regions having a different conductivity type than the substrate;

forming an oxide pillar over each doped region such that each end of each doped region extends beyond an adjacent sidewall of the oxide pillar;

forming an ultra-thin silicon body region by epitaxial regrowth extending from the ends of the doped regions and along opposing sidewalls of the oxide pillar;

forming a second plurality of doped regions in a polysilicon material over the oxide pillar and body regions such that the doped regions over the pillar are electrically coupled and have the same conductivity type as the first plurality of doped regions;

forming a gate insulator layer over the first plurality of doped regions, the body regions, and the second plurality of doped regions, the gate insulator layer having a lower layer, adjacent to each end of a doped region of the first plurality of doped regions, that has a thickness greater than remaining portions of the lower layer; and

forming a polysilicon control gate area over the gate insulator adjacent to each of the body regions.

31. The method of claim 30 wherein the gate insulator layer is a composite oxide-nitride-oxide layer and the lower layer is the oxide layer.

32. The method of claim 30 wherein the lower layer is an oxide layer.