

DESCRIPTION**TITLE: Method for transferring a membrane****FIELD OF THE INVENTION**

The present invention relates to the field of microelectronics and microsystems. In particular, it relates to a method for producing a structure comprising a membrane having a piezoelectric nature capable of deforming above at least one cavity.

TECHNOLOGICAL BACKGROUND OF THE INVENTION

MEMS (microelectromechanical systems) devices find wide use in the production of a variety of sensors. The operating principle of many of these MEMS devices is that of vibrating a flexible membrane above a cavity. Mention may be made, for example, of PMUT (piezoelectric micromachined ultrasonic transducer) microsystems. In operation, the vibration of the membrane generated by a physical parameter, for example the propagation of an acoustic wave, is converted into an electrical signal (or vice versa, depending on whether the device is in receiver or emitter mode).

To produce a structure with a membrane suspended over cavities, a number of approaches may be taken. A first approach consists in disassembling an SOI (silicon-on-insulator) substrate previously bonded to a substrate provided with cavities. Another approach comprises steps of deposition and of releasing of the membrane through chemical attack.

Forming a suspended membrane by way of sacrificial deposition has a number of drawbacks: the empty space in the cavity might be limited, the risk of bonding the membrane to

the bottom of the cavity during release, the risk of partial release, the difficulty in managing the mechanical stresses on the membrane, etc. Additionally, forming a suspended membrane by bonding an SOI substrate before removing it by grinding/chemical attack allows better control of the atmosphere in the cavity (sealed at the moment of bonding). However, this operation is relatively expensive because it requires the consumption of an SOI substrate.

Another, more elegant alternative consists in employing the transfer of a layer directly over the cavities using the Smart-Cut™ technique in order to form the suspended membrane.

With this alternative, it is difficult to transfer a membrane over cavities with large dimensions. However, there is a real need for cavities with large dimensions, especially for PMUT devices in which the cavities generally measure several hundred microns so that their operating frequency is not too high and is between 0.1 and 10 MHz.

French patent FR2715502 describes how to transfer a membrane suspended over cavities using Smart-Cut. According to this teaching, when the substrate comprising the cavities is made of silicon, the dimension (L_{max}) of the cavities should be less than 10 times the thickness (e_0) of the transferred membrane. What is understood by "dimension" of the cavity is the lateral dimension in the main plane of the front face of the substrate, for example a width, a length, a diameter, etc.

Additionally, the maximum thickness (e_0) of the membrane to be transferred using a Smart-Cut™-type method is limited by the donor substrate implantation energy, and therefore cannot be more than a few microns. Specifically, the high-energy ion implanters (>250 keV) which could allow deeper

implantation have low fluxes and the ion implantation step would require a significant amount of time. Consequently, to implant the target doses (several 10^{16}cm^{-2}), the method would be difficult to carry out (slow) and expensive. In addition, such equipment is not standard. As a result, the maximum lateral dimension of a cavity in this type of structure obtained using Smart-Cut cannot be more than a few tens of microns.

OBJECT OF THE INVENTION

The present invention aims to overcome all or some of the aforementioned drawbacks. It relates to a method for using Smart-Cut to transfer a membrane of piezoelectric nature to a substrate comprising at least one cavity of large size.

To that end, the invention relates to a method for producing a device comprising a membrane of piezoelectric nature above at least one cavity, the method comprising the following steps:

- a) providing a carrier substrate having a first face extending over a plane (x, y) and provided with a cavity opening out onto the first face, the cavity having a lateral dimension in the plane (x, y) that is larger than 30 μm ,
- b) providing a donor substrate provided with a buried weakened plane formed by implanting light species through a front face of the donor substrate, the weakened plane delimiting a surface layer,
- c) depositing, on the front face of the donor substrate, a stiffening layer made of piezoelectric material having a thickness greater than 500 nm,
- d) joining the carrier and donor substrates at a bonding interface arranged between the first face of the carrier substrate and the stiffening layer,

- e) splitting, after step d), the donor substrate at the buried weakened plane so as to transfer a membrane comprising the surface layer and the stiffening layer to the carrier substrate, the membrane being located above the cavity.

According to other advantageous and non-limiting features of this production method, which may be implemented alone or in any technically feasible combination:

- o the donor substrate is made of silicon or of silicon carbide,
- o the carrier substrate is made of silicon,
- o the donor substrate is made of silicon and the stiffening layer is deposited at a temperature lower than 450°C,
- o the donor substrate is made of silicon carbide and the stiffening layer is deposited at a temperature lower than 850°C,
- o the implanted light species are hydrogen ions and/or helium ions,
- o a first electrically conductive layer is interposed between the stiffening layer and the carrier substrate, the first layer being directly in contact with the stiffening layer and configured to form a lower electrode of the device,
- o a bonding layer is interposed between the stiffening layer and the carrier substrate, said bonding layer being directly in contact with the carrier substrate, the bonding layer preferably being made of silicon oxide,
- o a second electrically conductive layer is formed on the stiffening layer, the second layer being configured to form an upper electrode of the device,
- o the method comprises at least one mechanical grinding operation and/or at least one chemical-mechanical

- polishing operation and/or at least one chemical etching operation on the surface layer after splitting step e),
- o joining step d) comprises bonding by molecular adhesion between, on the one hand, the donor substrate provided with the stiffening layer and, on the other hand, the first face of the carrier substrate,
 - o a step of deposition on the free surface of the surface layer is performed after step e) so as to increase the thickness of the surface layer.

According to another aspect of the invention, the invention also relates to a donor substrate configured to transfer a membrane of piezoelectric nature to a carrier substrate provided with at least one cavity having a lateral dimension larger than 30 μm , the donor substrate comprising:

- a weakened plane arranged in the donor substrate (2) and delimiting a surface layer, and
- a stiffening layer made of piezoelectric material having a thickness (e) greater than 500 nm arranged on the surface layer (22).

BRIEF DESCRIPTION OF THE FIGURES

Other features and advantages of the invention will become apparent from the following detailed description of the invention, which is given with reference to the appended figures, in which:

[Fig. 1]

[Fig. 2]

[Fig. 3]

[Fig. 4]

[Fig. 5] Figures 1 to 5 show steps in a method for transferring a membrane arranged above buried cavities, in accordance with the invention;

[Fig. 6A]

[Fig. 6B]

[Fig. 6C]

[Fig. 6D] Figures 6A to 6D show variants and other steps in a transfer method according to the invention.

DETAILED DESCRIPTION OF THE INVENTION

In the description, the same references in the figures may be used for elements of the same type. The figures are schematic representations which, for the sake of legibility, are not to scale. In particular, the thicknesses of the layers along the z-axis are not to scale with respect to the lateral dimensions along the x- and y-axes; and the relative thicknesses of the layers with respect to one another have not necessarily been respected in the figures.

The invention relates to a method for transferring a membrane 14 of piezoelectric nature to a carrier substrate 1 comprising cavities 11 (Figures 1 to 5), said transfer method aiming to produce a structure 10 comprising buried cavities 11 of large size.

The method according to the invention comprises a step of providing the carrier substrate 1 (see Figure 1); the latter has a first face 12 intended to be joined to a donor substrate 2 and a second face 12', called the back face, opposite the first face 12. By way of non-limiting example, the carrier substrate 1 may comprise silicon, glass, sapphire,

etc. The thickness of the carrier substrate 1 may be of the order of a few hundred μm , typically 775 μm for substrates having a diameter of approximately 300 mm.

The carrier substrate 1 comprises a plurality of cavities 11 opening out onto the first face 12 thereof. Each cavity 11 has a bottom and peripheral walls. Preferably, the carrier substrate 1 is a silicon substrate.

The geometry of each cavity 11, which is dependent on the target device, in particular the target MEMS device, is defined by:

- the shape of the cavity 11 in the plane of the first face 12 of the carrier substrate 1 (called the main plane (x,y)): it will possibly be circular, square, rectangular or polygonal;
- the lateral dimensions L of the cavity 11, in the main plane (x,y): they will possibly vary from a few tens of microns to a few millimetres;
- the depth of the cavity 11, along the z-axis normal to the main plane (x,y): it will possibly vary from a few hundred nanometres to a few tens of microns, or even a few hundred microns.

According to the invention, the transfer method comprises transferring a membrane 14 of piezoelectric nature to the carrier substrate 1 comprising the buried cavities 11 of large size. What is meant by "large size" is that the lateral dimension L in the plane (x,y) of the cavities 11 is larger than 30 μm .

The planar distribution of the cavities 11, i.e. their distribution in the main plane (x,y) is also dependent on the target device and will define the inter-cavity spacing 11: it

will possibly vary from a few microns to a few hundred microns, or even a few millimetres. The inter-cavity spacing will possibly be uniform and identical over the entire surface of the carrier substrate 1 or vary between regions on the surface of said carrier substrate 1.

It will be noted that the carrier substrate 1 will possibly contain cavities 11 having different shapes, lateral dimensions, depths and/or planar distributions, in particular if provision is made to co-integrate devices of various types into the structure 10 comprising buried cavities.

Various layers will possibly be deposited on the bottom and/or on the walls of the cavities 11 (for example, silicon nitride, silicon oxide, etc.) depending on the type of device intended to be produced with the structure 10 comprising buried cavities 11.

The method according to the invention also comprises a step of providing a donor substrate 2 having a front face 21, which is intended to be joined to the carrier substrate 1, and a back face 21' (see Figure 2).

By way of example, and in a non-limiting manner, the donor substrate 2 will possibly comprise at least one semiconductor material, for example silicon, silicon carbide, gallium nitride, etc., or a piezoelectric material, for example lithium tantalate, lithium niobate, aluminium nitride, zinc oxide, PZT, etc. Preferably, the donor substrate 2 is a silicon substrate or a silicon carbide (SiC) substrate.

The steps of providing the donor substrate 2 also comprises a step of implanting light species into said donor substrate 2 through the front face 21 so as to form a weakened

plane 20 that lies between a first portion of the donor substrate 1, intended to form a surface layer 22, and a second portion 23 intended to make up the rest of the donor substrate 2. Preferably, the implanted light species are hydrogen ions and/or helium ions.

The thickness of the first portion, and therefore of the future surface layer 22, is dependent on the implantation energy of the light species (hydrogen and/or helium for example). Advantageously, the implantation energy is chosen so that the first portion of the donor substrate 2 has a thickness of about 0.2 microns to 2 microns.

Additionally, the method according to the invention further comprises a step of depositing a stiffening layer 13 made of material having a piezoelectric nature on the front face 21 of the donor substrate 2 (see Figure 3). The deposition step is implemented after the step of ion implantation of light species into the donor substrate 2. The thickness e of the layer 13 is greater than 500 nm. Even more preferably, the thickness e of the layer 13 is greater than 1 μm or even than 4 μm .

The stiffening layer 13 may comprise a material chosen from lithium niobate (LiNbO_3), lithium tantalate (LiTaO_3), potassium-sodium niobate ($\text{K}_x\text{Na}_{1-x}\text{NbO}_3$ or KNN), barium titanate (BaTiO_3), quartz, lead zirconate titanate or PZT ($\text{Pb}(\text{Zr},\text{Ti})\text{O}_3$), a compound of lead-magnesium niobate and of lead titanate (PMN-PT) in variable proportions (for example 70/30 or 90/10) depending on the sought-after properties, zinc oxide (ZnO), aluminium nitride (AlN) or aluminium-scandium nitride (AlScN), etc.

Preferably, the stiffening layer 13 is made of AlN or of PZT. Specifically, these two materials are considered to be the most commonly used piezoelectric materials in the MEMS field. Additionally, the elasticity coefficient of AlN is of the order of 300 GPa, and it is substantially higher than that of PZT. Thus, even more preferably, AlN will be chosen as the piezoelectric material of the stiffening layer 13.

By way of exemplary implementation, when the stiffening layer 13 is made of AlN and the donor substrate 2 is made of silicon provided with cavities having lateral dimensions of approximately 50 μm , the thickness of the stiffening layer is preferably greater than or equal to 1.5 μm . According to another, similar exemplary implementation, in which the stiffening layer 13 is made of PZT, then the thickness of the stiffening layer 13 is preferably chosen so as to be greater than 7.5 μm .

Additionally, a person skilled in the art will be able to choose the thickness of the stiffening layer 13 according to the lateral dimensions L of the cavities 11 and the mechanical properties (for example Young's modulus) of the stiffening layer 13 so as to succeed in transferring the membrane 14.

A person skilled in the art will also be able to adapt the temperature for the deposition of the stiffening layer 13 according to the nature of the donor substrate 2 so as to prevent blistering.

In other words, the stiffening layer 13 is advantageously deposited at a temperature that is adapted and configured so as to prevent blistering which may be caused by

the weakened plane 20 under the effect of a heat treatment with a high thermal budget.

Specifically, the effect of implanting light ions is to create defects (vacancies or interstitial defects) at the weakened plane 20. These defects are commonly called platelets and they have a size of the order of about ten nanometres. The effect of the temperature brings about a change in the population of these defects through Ostwald ripening, thereby leading to the occurrence of microcracks or microcavities. When oversaturated, the light ions implanted into the donor substrate 2 precipitate in gaseous form into these microcavities under the effect of the temperature. When a high thermal budget is applied, the cavities then grow vertically and laterally in the form of bubbles and coalesce, causing blistering on the front face 21.

According to one variant embodiment, when the donor substrate 2 is made of silicon (or comprises a layer made of silicon into which the light ions have been implanted), the deposition temperature is preferably lower than 450°C, and even more preferably lower than 400°C.

According to another variant embodiment, when the donor substrate 2 is made of silicon carbide (or comprises a layer made of silicon carbide into which the light ions have been implanted), the deposition temperature is preferably lower than 850°C.

The layer 13 may be deposited using any technique known to those skilled in the art which is compatible with conventional methods in the microelectronics field. Preferably, the stiffening layer 13 is deposited using cathode

sputtering or using the sol-gel technique, a chemical deposition technique.

By way of example, deposition by cathode sputtering advantageously makes it possible to obtain crystallized piezoelectric layers for low deposition temperatures of the order of 300 or 400°C for certain materials, such as aluminium nitride (AlN).

Advantageously, a piezoelectric stiffening layer 13 made of AlN is deposited using cathode sputtering according to the invention.

Additionally, PZT is deposited using cathode sputtering at relatively higher temperatures than for the deposition of AlN, in order to be crystallized. The temperatures for the deposition of PZT may reach 700°C.

According to one embodiment of the invention, a stiffening layer 13 made of PZT may be deposited using the sol-gel method. This is a chemical deposition technique: the precursors to be deposited are added in solid form to a solvent. The obtained solution is then spread over the front face 21 of the donor substrate 2. The spreading may be achieved by spin coating. The substrate is then dried to evaporate the solvent before undergoing a step of calcination to break up carbon chains. The sequence of spreading, drying and calcination steps may be repeated multiple times in order to increase the thickness of the obtained layer. Additionally, the obtained layer is generally amorphous in nature and requires a final crystallization/densification heat treatment step.

According to another embodiment, a stiffening layer 13 made of PZT may be produced using low-temperature MOCVD (metalorganic chemical vapour deposition). Specifically, it is known that this technique makes it possible to deposit PZT in a crystalline state at temperatures that may be lower than 400°C or even less.

According to one embodiment of the invention, the method optionally comprises a heat treatment for healing the deposited stiffening layer 13. Said healing heat treatment may advantageously serve to partially or completely recrystallize the stiffening layer 13. This treatment may also be used to degas and/or rid the deposited piezoelectric layer of impurities which might have been introduced into the layer during, before or after deposition thereof. According to one alternative, the heat treatment may comprise a thermal anneal to improve the crystal quality of the deposited layer 13.

As illustrated in Figure 4, the method according to the invention further comprises a step of joining the carrier 1 and donor 2 substrates. The carrier 1 and donor 2 substrates are joined at a bonding interface 30 arranged between the first face 12 of the carrier substrate 1 and the stiffening layer 13 arranged on the front face 21 of the donor substrate 2.

Advantageously, this step comprises direct bonding, by molecular adhesion, between: on the one hand, the first face 12 of the donor substrate 1 and, on the other hand, the stiffening layer 13 of the carrier substrate 1. The principle of molecular adhesion, which is well known in the prior art, will not be described in further detail here. It will be noted that the surfaces to be joined must have a very good surface

finish (cleanness, low roughness, etc.) for a joint of good quality to be obtained.

Advantageously, in order to guarantee a joint of good quality, the joining step comprises cleaning the surfaces to be joined of the donor substrate 2 (here according to this embodiment the surface of the stiffening layer 13) and of the carrier substrate 1, before said surfaces are brought into contact. By way of example, a conventional sequence used in microelectronics, especially for silicon-based substrates, comprises an ozone clean, an SC1 clean (SC1 being the acronym of Standard Clean 1) and an SC2 clean (SC2 being the acronym of Standard Clean 2) with intermediate rinses. The surfaces to be joined will also possibly be activated, for example using a plasma, before being brought into contact, in order to promote a high bonding energy between said surfaces.

The method according to the invention further provides for a step of splitting the donor substrate 2 at the buried weakened plane 20 so as to transfer a membrane 14 comprising the surface layer 22 and the stiffening layer 13 to the carrier substrate 1. The splitting occurs at the buried weakened plane 20, between the surface layer 22 and the rest 23 of the donor substrate 2 (see Figures 2, 4 and 5).

Additionally, the splitting step is, of course, carried out after the step of joining the carrier substrate 1 and the donor substrate 2 provided with the stiffening layer 13. It is a conventional splitting step as per the Smart Cut method.

As illustrated in Figure 5, upon completion of the splitting step, a membrane 14 transferred to the carrier substrate 1 is obtained. It will be recalled that the Smart

Cut method advantageously allows thin layers having an excellent thickness uniformity to be obtained. This criterion may be very advantageous for certain MEMS devices requiring flexible membranes exhibiting controlled thicknesses.

This splitting is preferably performed during a heat treatment at a temperature of between a few hundred degrees and 950°C. Preferably, the splitting is implemented during a heat treatment carried out at a temperature lower than 700°C when the weakened plane is arranged in a silicon layer of the donor substrate 2. According to another embodiment, the splitting is implemented during a heat treatment carried out at a temperature lower than 950°C when the weakened plane is arranged in a silicon carbide layer of the donor substrate 2.

According to one embodiment, the splitting step could alternatively be mechanically assisted or performed after the heat treatment, by means of a mechanical stress.

According to the embodiment in which the stiffening layer 13 is made of PZT deposited using sol-gel, the splitting heat treatment performed at a temperature of between 500 and 750°C will advantageously allow the splitting of the donor substrate and the recrystallization of the deposited PZT. In other words, the splitting heat treatment also comprises the heat treatment for healing the PZT layer.

After the membrane 14 has been transferred to the carrier substrate 1, the splitting step may comprise a finishing treatment aiming to improve the crystal quality (removal of defects from the layer), the surface quality (removal of residual roughness from the free surface of the layer 22) and/or to modify the thickness of the surface layer 22. This treatment will possibly include one or more heat

treatments, chemical-mechanical polishes, chemical etches, epitaxial growth and/or deposition of additional layers.

Specifically, in certain cases where the thickness of the surface layer 22 transferred using the Smart Cut method is insufficient, it is possible to increase this thickness by depositing an additional layer on the free surface of the surface layer 22, for example by epitaxial growth or other known deposition methods, during a finishing treatment that is mentioned above (see Figure 6D). The additional layer is preferably of the same nature as the surface layer 22.

Upon completion of the method according to the invention, what is obtained is a structure 10 provided with buried cavities 11 of large size, and a membrane 14 of piezoelectric nature (comprising the surface layer 22 and the stiffening layer 13) above the one or more cavities 11.

The method according to the invention is easy to implement and advantageously allows the effective transfer of a membrane to a carrier substrate provided with cavities of large size, cavities having a lateral dimension larger than 30 μm . The membrane is transferred in its entirety and benefits from the advantages of the Smart Cut method. Specifically, the applicant has observed that a stiffening layer having a thickness greater than 500 nm makes it possible to increase the stiffening effect on the donor substrate, even though its nature is piezoelectric and different from the donor substrate. This advantageously makes it possible to avoid the problems of blistering and/or of partial transfer of a membrane which may occur when the Smart Cut method involves a carrier substrate covered with cavities of large size. What is meant by "partial transfer" is that a part of the membrane is

not transferred to the carrier substrate after the splitting step.

In addition, the stiffening layer according to the invention is of piezoelectric nature. Thus, the method according to the invention provides a solution that is elegant, easy to implement and effective in producing a membrane of piezoelectric nature on a substrate with cavities of large size, while benefiting from the advantages of the Smart Cut method. In other words, the transferred membrane exhibits excellent uniformity of thickness, which may be highly advantageous for certain MEMS devices which require flexible membranes above cavities, with controlled thicknesses. In particular, the obtained structure may be used to produce PMUT devices in which the cavities generally measure several hundred microns. By virtue of the benefits of the Smart Cut method, of the piezoelectric nature of the transferred membrane, and of the large size of the cavities in the carrier substrate, the method according to the invention makes it possible to obtain a structure configured for the production, in particular, of PMUT devices having a precise and uniform operating frequency.

According to one embodiment illustrated in Figure 6A, the carrier substrate 1 and/or the donor substrate 2 may comprise a bonding layer 32 at the first face 12 and/or above the stiffening layer 13, respectively, in order to promote bond quality and the bonding energy of their interface. The bonding layer 32 is preferably arranged on the stiffening layer 13 such that the bonding interface 30 is between the first face 12 of the carrier substrate 1 and said bonding layer 32 (see Figures 6A and 6C). Advantageously, the bonding layer 32 is made of silicon oxide. Specifically, silicon oxide

is an easily deposited material and allows a roughness compatible with direct bonding to be obtained.

Preferably, the bonding layer 32 is made of silicon oxide and it is formed using TEOS (tetraethyl orthosilicate) PECVD. After deposition thereof, the oxide layer may be planarized and then cleaned in order to prepare it for the direct bonding step, as described above.

In addition to the layer 32 configured to improve bonding, additional layers may be provided, in particular at the stiffening layer 13. The arrangement, nature and function of these layers will be described in detail below.

According to one embodiment illustrated in Figure 6B, a first electrically conductive layer 31 is interposed between the stiffening layer 13 and the carrier substrate 1. The first layer 31 is directly in contact with the stiffening layer 13 and it is configured so as to form a lower electrode 31 of the device 10 produced upon completion of the method according to the invention.

The first layer 31 may be deposited after the step of depositing the stiffening layer 13. This layer 31 may be made of platinum (Pt), of gold (Au), of copper (Cu), of molybdenum or of aluminium (Al). Additionally, the first layer 31 may be produced using any technique known to those skilled in the art which is compatible with conventional methods in the microelectronics field. The lower electrode 31 may advantageously take the form of an interdigitated comb.

By way of example, the first layer 31 may be deposited using PVD (physical vapour deposition). The deposition is preferably performed at low temperature (lower than 450°C).

For the deposition of the layer 31, tie and/or diffusion barrier layers may also be provided. A tie layer serves to improve the quality of deposition of the layer 31 on the donor substrate 2, in particular if the layer 31 is of metallic nature. Additionally, a diffusion barrier layer advantageously makes it possible to prevent the diffusion of metals in the final structure during possible later technological steps.

According to one embodiment, when the layer 31 is compatible with direct bonding (sufficient level of roughness), it may be bonded directly to the carrier substrate 1 (e.g. Au/Au direct bonding). In this case, thermocompression bonding may also be envisaged.

According to one embodiment of the invention in which the bonding layer 32 is used as described above, the latter may be deposited on the first layer 31.

According to another embodiment illustrated in Figure 6B, a second electrically conductive layer 33 is formed on the surface layer 22. The second layer 32 is directly in contact with the surface layer 22 and it is configured so as to form an upper electrode 32 of the device 10 produced upon completion of the method according to the invention.

The second layer 33 may be deposited after the splitting step (see Figure 6B) or before the deposition of the stiffening layer 13 (see Figure 6C). This layer 33 may be made of platinum (Pt), of gold (Au), of copper (Cu), of molybdenum or of aluminium (Al).

Preferably and as illustrated in Figure 6C, the layer 33 is deposited before the deposition of the stiffening layer 13 such that it is interposed, after the splitting step,

between the surface layer 22 and the stiffening layer 13. According to this embodiment, the electrodes 31 and 33 are advantageously buried and are therefore passivated such that they are less exposed to unwanted oxidation or deterioration.

Additionally, the second layer 33 may be produced in the same way as the layer 31, in other words using any technique known to those skilled in the art which is compatible with conventional methods in the microelectronics field. Furthermore, the layers 31 and 33 may have a thickness ranging from a few nanometres to a few tens of nanometres.

The invention also relates to a donor substrate 2 configured to transfer a membrane 14 of piezoelectric nature to a carrier substrate 1 comprising cavities 11 of large size (Figures 1 to 5).

As illustrated in Figure 3, the donor substrate 2 comprises a bulk substrate comprising at least one semiconductor material, for example silicon, silicon carbide, gallium nitride, etc., or a piezoelectric material, for example lithium tantalate, lithium niobate, aluminium nitride, zinc oxide, PZT, etc. Preferably, the donor substrate 2 is a silicon substrate or a silicon carbide (SiC) substrate.

The donor substrate according to the invention is provided with a weakened plane 20 that lies between a first portion of the donor substrate 1, intended to form a surface layer 22, and a second portion 23 intended to make up the rest of the donor substrate 2. The weakened plane is formed by implanting light species into said donor substrate 2. Preferably, the implanted light species are hydrogen ions and/or helium ions.

Furthermore, the donor substrate 2 is provided with a stiffening layer 13 of piezoelectric nature, arranged on the front face 21 of the donor substrate 2. The thickness e of the layer 13 is greater than 500 nm. Even more preferably, the thickness e of the layer 13 is greater than 1 μm or even than 4 μm .

The stiffening layer 13 may comprise a material chosen from lithium niobate (LiNbO_3), lithium tantalate (LiTaO_3), potassium-sodium niobate ($\text{K}_x\text{Na}_{1-x}\text{NbO}_3$ or KNN), barium titanate (BaTiO_3), quartz, lead zirconate titanate or PZT ($\text{Pb}(\text{Zr},\text{Ti})\text{O}_3$), a compound of lead-magnesium niobate and of lead titanate (PMN-PT) in variable proportions (for example 70/30 or 90/10) depending on the sought-after properties, zinc oxide (ZnO), aluminium nitride (AlN) or aluminium-scandium nitride (AlScN), etc.

Preferably, the stiffening layer 13 is made of AlN or of PZT.

The layer 13 may be deposited using any technique known to those skilled in the art which is compatible with conventional methods in the microelectronics field. Preferably, the stiffening layer 13 is deposited using cathode sputtering or using the sol-gel technique, which is a chemical deposition technique.

The donor substrate according to the invention is advantageously configured to transfer a membrane 14 formed by the stiffening layer 13 and the surface layer 22 to a carrier substrate 1 provided with cavities 11 of large size (see Figure 5). The donor substrate 2 according to the invention advantageously allows the transfer of a membrane providing both a stiffening nature to facilitate successful effective

transfer of the membrane, and a piezoelectric nature to produce devices requiring such a material, in particular PMUT devices.

CLAIMS

1. Method for producing a device (10) comprising a membrane (14) of piezoelectric nature above at least one cavity (11), the method comprising:
 - a) providing a carrier substrate (1) having a first face (12) extending over a plane (x, y) and provided with a cavity (11) opening out onto the first face (12), the cavity (11) having a lateral dimension in the plane (x, y) that is larger than 30 μm ,
 - b) providing a donor substrate (2) provided with a buried weakened plane (20) formed by implanting light species through a front face (21) of the donor substrate (2), the weakened plane (20) delimiting a surface layer (22),
 - c) depositing, on the front face (21) of the donor substrate (2), a stiffening layer (13) made of piezoelectric material having a thickness (e) greater than 500 nm,
 - d) joining the carrier (1) and donor (2) substrates at a bonding interface (30) arranged between the first face (12) of the carrier substrate (1) and the stiffening layer (13),
 - e) splitting, after step d), the donor substrate (2) at the buried weakened plane (20) so as to transfer a membrane (14) comprising the surface layer (22) and the stiffening layer (13) to the carrier substrate (1), the membrane (14) being located above the cavity (11).
2. Method according to the preceding claim, in which the donor substrate (2) is made of silicon or of silicon carbide.
3. Method according to Claim 1, in which the carrier substrate (1) is made of silicon.

4. Method according to Claim 1, in which the donor substrate (2) is made of silicon and the stiffening layer (13) is deposited at a temperature lower than 450°C.
5. Method according to Claim 1, in which the donor substrate is made of silicon carbide and the stiffening layer (13) is deposited at a temperature lower than 850°C.
6. Method according to one of the preceding claims, in which the implanted light species are hydrogen ions and/or helium ions.
7. Method according to one of the preceding claims, in which a first electrically conductive layer (31) is interposed between the stiffening layer (13) and the carrier substrate (1), the first layer (31) being directly in contact with the stiffening layer (13) and configured to form a lower electrode (31) of the device (10).
8. Method according to one of the preceding claims, in which a bonding layer (32) is interposed between the stiffening layer (13) and the carrier substrate (1), said bonding layer (32) being directly in contact with the carrier substrate (1).
9. Method according to the preceding claim, in which the bonding layer (32) is made of silicon oxide.
10. Method according to one of the preceding claims, in which a second electrically conductive layer (33) is formed on the stiffening layer (13), the second layer (33) being configured to form an upper electrode (33) of the device (10).

11. Method according to one of the preceding claims, comprising at least one mechanical grinding operation and/or at least one chemical-mechanical polishing operation and/or at least one chemical etching operation on the surface layer (22) after splitting step e).
12. Method according to one of the preceding claims, in which joining step d) comprises bonding by molecular adhesion between, on the one hand, the donor substrate (2) provided with the stiffening layer (3) and, on the other hand, the first face (12) of the carrier substrate (1).
13. Method according to one of the preceding claims, in which a step of deposition on the free surface of the surface layer (22) is performed after step e) so as to increase the thickness of the surface layer (22).
14. Donor substrate (2) configured to transfer a membrane (14) of piezoelectric nature to a carrier substrate provided with at least one cavity having a lateral dimension larger than 30 μm , the donor substrate (2) comprising:
 - a weakened plane (20) arranged in the donor substrate (2) and delimiting a surface layer (22), and
 - a stiffening layer (13) made of piezoelectric material having a thickness (e) greater than 500 nm arranged on the surface layer (22).