ABSTRACT

INTEGRATED CIRCUIT SYSTEM EMPLOYING STRESS MEMORIZATION TRANSFER

An integrated circuit system that includes: providing a gate and a spacer formed over a substrate; performing an implant that amorphizes the gate and a source/drain region defined by the spacer; removing the spacer; depositing a stress memorization layer over the integrated circuit system; and transferring a stress from the stress memorization layer to the gate and the source/drain region.

FIG 2