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PATENT SPECIFICATION

DRAWINGS ATTACHED

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COMPLETE SPECIFICATION

Logic Circuits

We, RADIO CORPORATION OF AMERICA, a Corporation organized under the laws of the State of Delaware, United States of America, of 30, Rockefeller Plaza, City and State of New York, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to logic circuits and, in particular, to new and improved logic circuits which employ transistors of opposite conductivity type.

Heat generated in electrical circuits usually is undesirable because of its aging effect on circuit components, its effect in changing the operating parameters and electrical characteristics of some components, and the resulting need and expense of providing cooling means in some cases. Moreover, the heat generated represents a power loss. The problem of heat generation is especially significant in integrated structures because of the small physical size of the circuitry and the close spacing of adjacent circuits.

Accordingly it is an object of this invention to provide a logic circuit that dissipates little or no power as heat in the steady state condition and very little power during a switching transient.

Circuits embodying the invention employ semiconductor devices each having a pair of electrodes defining a conduction path, and a control electrode which in use serves to control the conductivity of the conduction path. The semiconductor devices preferably are MOS silicon or TFT field-effect transistors in which case the pair of electrodes defining the conduction path are source and drain electrodes, and the control electrode is a gate electrode. Devices of one conductivity type

have their conduction paths connected so as to provide a first circuit branch between a first point and a first output terminal, and a second circuit branch between the first point and a second output terminal. Devices of opposite conductivity type provide a third circuit branch between a second point and the first output terminal, and a fourth circuit branch between the second point and the second output terminal. An operating potential is applied across the first and second points. Two input terminals are provided for receiving information signals, and a third input terminal receives clock, or control signals. Connections between the input terminals and the control electrodes of the semiconductor devices are such that there is no low impedance path between the first and second points for any operating condition of the circuit.

In the accompanying drawings:

FIGURE 1 is a schematic diagram of a gated bistable circuit embodying the invention;

FIGURE 2 is a truth table for the bistable circuit of FIGURE 1;

FIGURE 3 is a schematic diagram of an other gated bistable circuit embodying the invention;

FIGURE 4 is a truth table for the bistable circuit of FIGURE 3;

FIGURE 5 is a block diagram which shows the manner in which the bistable circuits of FIGURES 1 and 3 can be connected to perform a shift type circuit;

FIGURE 6 is a schematic diagram of a "blocking" gate;

FIGURE 7 is a truth table for the blocking gate; and

FIGURE 8 is a block diagram of a shift circuit arrangement employing gated bistable circuits and blocking gates.

An insulated-gate field-effect transistor has

[Price 4s. 6d.]

characteristics that make the device particularly suitable for use in integrated circuitry. Such a transistor may be defined as a majority carrier field effect device that includes a semiconductor layer or wafer, with source and drain regions spaced from each other and contiguous to the semiconductor layer. The semiconductor layer provides a conduction path between the source and drain regions. A gate (control) electrode is separated by an insulating film from a portion of the semiconductor that lies between source and drain, and controls the conductivity (inverse of the resistivity) of the conduction path.

Since the gate electrode is insulated from the semiconductor, it does not draw any current, or at least it draws no appreciable current. For this reason the drain electrode of one transistor can be connected directly to the gate of another transistor, and there is little or no current flow through, or power dissipated in, the connection.

Two known types of insulated-gate field-effect transistors are the thin-film transistor (TFT) and the metal-oxide semiconductor (MOS). Some of the physical and operating characteristics of the TFT are described in the article "The TFT—A new Thin-Film Transistor", by P. K. Weimer, appearing at pages 1462—1469 of the June, 1962 issue of the Proceedings of the IRE. The MOS transistor is described in an article entitled, "The Silicon Insulated-Gate Field-Effect Transistor", by S. R. Hofstein and F. P. Heiman, in the September, 1963 issue of the Proceedings of the IEEE at pages 1190—1202.

Insulated-gate field-effect transistors may be of either the enhancement type or the depletion type. The enhancement type unit is of particular interest in the present application. In an enhancement type unit, the conductivity of the conduction path is low and only a small leakage current flows between source and drain when the gate and source have the same voltage. The transistor is biased "on" when the gate voltage differs from the source voltage in a specified polarity direction. The conductivity of the conduction path in an "on" transistor is a function of the voltage difference between source and gate.

A transistor may be either a P-type unit or an N-type unit, depending upon the conductivity type material of the semiconductor. A P-type unit is one in which the majority carriers are holes; in an N-type unit, the majority carriers are electrons. According to this definition, a P-type enhancement unit is one that has a relatively high conductivity conduction path when the gate voltage is negative relative to the source voltage; the N-type enhancement unit has a relatively high conductivity conduction path when its gate voltage is positive relative to its source voltage.

Because of the desirable characteristics of insulated-gate field-effect transistors, the circuit arrangements to be described are illustrated as employing such transistors. A P-type unit may be identified in the drawing by an arrowhead on the source lead pointing toward the unit. An N-type unit has an arrowhead on the source lead pointing away from the unit.

A clocked, gated or trigger type bistable circuit embodiment of the invention is illustrated schematically in FIGURE 1. The bistable portion of the circuit comprises a pair of N-type enhancement transistors 20a, 20b and a pair of P-type enhancement transistors 30a, 30b. N-type transistors 20a and 20b have their source electrodes 22a and 22b connected to a point of first operating potential, illustrated as circuit ground, and have their drain electrodes 24a and 24b connected respectively to a pair of output terminals 28 and 38. First output terminal 28 is labeled "(0) out" and second output terminal 38 is labeled "(1) out".

The P-type transistors 30a and 30b have their drain electrodes 34a and 34b connected to the first and second output terminals 28 and 38, respectively, and to the drain electrodes 24a and 24b, respectively, of the N-type transistors 20a and 20b. The gate, or control, electrodes 26a and 36a of transistors 20a and 30a, respectively, are connected together and to the second output terminal 38. Gate electrodes 26b and 36b of transistors 20b and 30b, respectively, are connected together and to the first output terminal 28.

Third and fourth N-type enhancement transistors 20c and 20d have their conduction paths serially connected between circuit ground and the first output terminal 28. In particular, fourth transistor 20d has its drain electrode 24d connected to the output terminal 28 and has its source electrode 22d connected to the drain electrode 24c of third N-type transistor 20c. Third transistor 20c has its source electrode grounded. Fifth and sixth N-type enhancement transistors 20e and 20f have their conduction paths serially connected, in a similar manner, between circuit ground and the second output terminal 38.

Third and fourth P-type enhancement transistors 30c and 30d have their drain electrodes 34c and 34d connected together and to the source electrode 32a of transistor 30a. The source electrodes 32c and 32d of transistors 30c and 30d are connected together and to a junction point 40. In a similar manner, fifth and sixth P-type enhancement transistors 30e and 30f have their conduction paths connected in a parallel between the source electrode 32b of transistor 30b and the junction point 40 as shown.

Operating potential is applied between point 40 and the other common voltage point

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(circuit ground) by connecting a bias source of V volts, such as a battery 42, between point 40 and ground. Battery 42 is shown as having its positive terminal connected to the point 40 and having its negative terminal grounded, whereby the voltage at point 40 is $+V$ volts relative to circuit ground.

Transistors 20c and 30c have their gate electrodes 26c and 36c connected to a RESET input terminal 44, and transistors 20e and 30f have their gate electrodes 26e and 36f connected to a SET input terminal 46. Transistors 20d, 20f, 30d and 30e have their gate electrodes 26d, 26f, 36d and 36e connected to a trigger, or clock, input terminal 48.

It will be noted that all of the various connections between the various transistors and between the transistors and the input and output terminals are direct connections in the sense that they are made by negligible impedance means. This is a distinct advantage when the circuit is fabricated in integrated form. Such direct connections are made possible by the fact that little or no current flows in the high impedance gate circuit of an insulated gate field-effect transistor, and because there is never a low impedance path through the transistors between circuit ground and the $+V$ volt source, as will be apparent as the description proceeds.

FIGURE 2 is a partial truth table for the bistable circuit of FIGURE 1. As listed in the table, the voltage at second output terminal 38, the (1) output terminal, is $+V$ volts when an input of $+V$ volts is applied at the RESET (R) input terminal 44 and a trigger pulse 50 of $+V$ volts is applied concurrently at the trigger (T) input terminal 48. The SET input voltage is zero at that time, assuming that the SET and RESET inputs are complementary, and the voltage at first output terminal 28 also is zero. The bistable circuit may be considered to be in the RESET state and storing a binary "0" when these conditions exist. The bistable circuit becomes SET and stores a binary "1" when the voltage at the SET (S) input terminal 46 is $+V$ volts when the trigger pulse 50 is applied. The voltages at the (1) and (0) output terminals 38 and 28 then are zero and $+V$ volts, respectively.

Consider now the operation of the bistable circuit. Assume that the voltage at the trigger input terminal 48 is at ground potential, as is the case except when new information is to be gated into the bistable circuit. N-type transistors 20d and 20f are biased "off" by the voltage at the trigger input terminal 48, and P-type transistors 30d and 30e are biased "on". The conduction path of an "off" transistor has a very high impedance, of the order of megohms, for example, and the transistor can be considered an "open" circuit for practical purposes. The only current that

flows through an "off" transistor is leakage current, and this current has a very small value, of the order of a few microamperes. Accordingly, there is very little or no current flow in the transistors 20c, 20d, 20e and 20f, and very little power dissipated therein when the trigger voltage at terminal 48 is at ground potential.

Let it be assumed that the bistable circuit is in the RESET state. This means that the voltage at the (1) output terminal 38 is $+V$ volts. N-type transistor 20a is biased "on" by this voltage and the voltage at the (0) output terminal 28 is zero. P-type transistor 30a is biased "off" and presents an "open" circuit between output terminal 28 and the drain electrode 34d of transistor 30d. Thus, only leakage current flows through transistors 20a, 30a and 30d between circuit ground and the positive terminal of the battery 42, and very little power is dissipated.

With ground potential at output terminal 28, transistor 20b is biased "off" and transistor 30b is biased "on". Transistors 30b and 30e present a low impedance path between the (1) output terminal 38 and the positive terminal of the battery 42, whereby the voltage at output terminal 38 is $+V$ volts. However, only leakage current flows through the "on" transistors 30b and 30e because the "off" transistor 20b presents an "open" circuit to ground. Also, as mentioned previously, an insulated-gate field-effect transistor has a very high input impedance due to the insulated gate. For this reason, little or no current is supplied from the output terminal 38 (or 28) to any transistors which are driven from these points.

The bistable circuit may be switched from the RESET to the SET state by applying input voltages of $+V$ volts and zero volts at the SET and RESET input terminals 46, 44, respectively, and applying a trigger or clock pulse 50 at trigger input terminal 48. An input of $+V$ volts at the SET input terminal 46 biases transistor 20e "on" and biases transistor 30f "off". No switching occurs until a trigger pulse 50 is applied because transistors 20d and 20f are biased "off".

When a trigger pulse 50 is applied at terminal 48, transistor 20f is biased "on" and transistor 30e is biased "off". Transistors 20e and 20f present a low impedance path between circuit ground and the (1) output terminal 38, and drive the output voltage at the terminal to ground potential. Transistor 30b is "on" when the trigger pulse is first applied. Were it not for the transistors 30e and 30f, there would be a low impedance circuit path through transistor 20e, 20f and 30b between circuit ground and the positive terminal of battery 42, and a heavy current would flow through these transistors. Parallel transistors 30e and 30f prevent this condition since they are both biased "off" when

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the transistor 20f is biased "on". Therefore, there is no low impedance path between circuit ground and the positive terminal of battery 42.

5 With fast acting transistors, and especially those having turn-on thresholds, a transistor can be turned off as fast as, or faster than, an "off" transistor can be turned "on". Under these conditions, there is no low impedance path through transistors 20e, 20f, 30b and 30e or 30f even during the switching transient. Input capacitances of the transistors are charged or discharged during the switching transient, with a resulting small power dissipation in the transistors. However, the only other current that flows is leakage current.

When the voltage at the (1) output terminal 38 falls to ground potential, transistor 20a is biased "off" and transistor 30a is biased "on". Transistor 30c is "on" at this time because the voltage at the RESET input terminal 44 is at ground potential. Thus, there is a low impedance path through transistors 30a and 30c between the (0) output terminal 28 and point 40, whereby the voltage at terminal 28 rises to +V volts. This voltage is fed back to the gate electrode 26b of transistor 20b and turns this latter transistor "on" at the same time transistor 30(b) is turned off. The voltage at the (1) output terminal 38 then remains at ground potential at the termination of the trigger pulse 50.

The bistable circuit remains in the SET state until the voltages at the SET and RESET input terminals 46 and 44 are changed to zero and +V volts, respectively, and a trigger pulse 50 is applied. As mentioned previously, no switching can occur in the absence of a trigger input pulse 50 since transistors 20d and 20f are "off" and the voltage at an output terminal 28 or 38 cannot be driven from +V volts to ground potential. It follows also that no switching of the flip-flop can occur if the voltages at both the RESET and SET input terminals 44 and 46 are at ground potential, even in the presence of an applied trigger pulse 50, because both of the transistors 20c and 20e then are biased "off". Advantage is taken of this feature in an embodiment of the invention to be described hereinafter.

By way of summary of the above discussion, there is never a low impedance path through any combination of transistors between circuit ground and the positive terminal of battery 42 in a steady state circuit condition. Also, with fast transistors, especially those having a turn-on threshold, there is no low impedance path between circuit ground and the positive terminal of the battery 42 even during a switching transient. The only current that flows through the transistors in the steady state is leakage current, and the power dissipated is, therefore, very low. Dur-

ing a switching transient, some additional current may flow through various ones of the transistors due to charge and discharge of the interelectrode capacitances.

FIGURE 3 is a schematic diagram of another gated bistable circuit embodiment of the invention. In FIGURE 3, the transistors 20c and 20d are connected in parallel, and the source electrode 22a of transistor 20a is connected to the drain electrodes 24c, 24d of the transistors 20c, 20d, respectively. Transistors 20e and 20f also have their conduction paths connected in parallel and have their drain electrodes connected to the source electrode 22b of transistor 20b. The source electrodes 32a, 32b of transistors 30a and 30b are connected directly to a source of +V volts as indicated. Transistors 30c and 30d have their conduction paths connected in series between the +V volt source and the (0) output terminal 28. In a like manner, transistor 30e and 30f have their conduction paths connected in series between the +V volt source and the (1) output terminal 38. The other connections are the same as those in the FIGURE 1 circuit.

FIGURE 4 is a truth table for the bistable circuit of FIGURE 3. By a comparison of this table with the table of FIGURE 2, it may be seen that from a functional or logic standpoint the only difference between the circuits of FIGURES 1 and 3 is that the FIGURE 3 circuit requires a trigger input of zero volts to enter new information into the bistable circuit, whereas the FIGURE 1 bistable circuit requires a trigger voltage of +4 volts. Otherwise the operation of the bistable circuits of FIGURES 1 and 3 is similar in concept. Advantage can be taken of the different triggering potentials of the two types of bistable circuits to provide a relatively simple shift circuit.

Considering that a bistable circuit of the type shown in FIGURE 1 is designated a type "A" bistable circuit, and a bistable circuit of the type shown in FIGURE 3 is designated a type "B" flip-flop, a two stage per bit shifting circuit requiring only one clock or trigger source may be provided in the manner illustrated in FIGURE 5. Odd numbered stages 53a, 53b of the shifting circuit, which may be a shift register, ring counter, or the like, comprise bistable circuits of type A, and the even numbered stages 54a, 54b are of type B. Each of the stages has its (0) and (1) output terminals connected at the SET (S) and RESET (R) input terminals, respectively, of the next succeeding stage. The trigger (T) input terminal of all of the stages are connected to a common bus bar 56 and the bus bar, in turn, is connected to receive the clock or trigger pulses 50 from any suitable source (not shown).

Information is gated into a type A bistable circuit i.e. A₁ when the clock or trigger pulse

is at +V volts, as mentioned previously. Therefore, when the clock voltage rises from zero to +V volts, each remaining type A bistable circuit other than A₁, i.e. A₂, assumes the state of the type B bistable circuit which immediately precedes it. When the clock voltage falls from +V volts to zero volts, new information is entered into the type B bistable circuit, and each B bistable circuit assumes the state of the type A bistable circuit which immediately precedes it. There is no "race" condition in the shifting circuit, since the type A bistable circuits cannot change state when the clock voltage is zero volts and the type B bistable circuits cannot change state when the clock voltage is +V volts. Moreover, only a single clock pulse source is needed for shifting information, and no reactive elements are required. The circuit, therefore, is not repetition rate sensitive.

In some cases, it is desirable to provide a shifting type circuit that has only one stage per bit of storage. As is known, some means must be provided between stages to provide interim storage and to prevent a race condition. A gating circuit which may be used in such a shifting circuit is illustrated in FIGURE 6. The gating circuit of FIGURE 6 also has other uses.

The gate (gating circuit) comprises first and second P-type transistors 70a and 70b having their conduction paths connected in series between a point 78 and an output terminal 88, labelled "output B". First transistor 70a has its source electrode 72a connected directly to a point 78, and has its drain electrode 74a connected to the source electrode 72b of second transistor 70b. The drain electrode 74b is connected to the output terminal 88. A bias source of V volts, such as the battery 90, has its positive terminal connected at the point 78 and has its negative terminal connected to a point indicated as circuit ground. Third and fourth P-type transistors 70c and 70d are connected in a similar manner between the point 78 and a second output terminal 92, ~~labelled~~ "output A".

A first N-type unit 80a has its drain electrode 84a connected to the output terminal 88 and has its source electrode 82a connected to ground. A second N-type unit 80b is similarly connected between the second output terminal 92 and circuit ground.

The gate electrode 76b of transistor 70b and the gate electrode 86a of transistor 80a are connected directly together and to a RESET (R) input terminal 94. Gate electrode 76d of transistor 70d and gate electrode 86b of transistor 80b are connected together and to a SET (S) input terminal 96. The gate electrodes 76a and 76c of the remaining transistors 70a and 70c are connected together and to a trigger (T), or clock, input terminal

98. Clock pulses 50 are applied between the trigger (T) terminal 98 and ground.

As will be seen subsequently, the outputs A and B, in the absence of a clock pulse 50, are determined by the voltages applied at the R and S input terminals 94 and 96. These outputs do not change when the clock pulse is applied, provided that the R and S inputs do not change. If they do change, the A and B outputs during the clock period are determined by both the new R and S inputs and by the operating state of the circuit prior to the application of the clock pulse. As an aid to a better understanding of the circuit's characteristics, the "truth" table of FIGURE 7 lists the various voltage values as a function of time. The different time periods given in the table correspond to the like-designated time periods shown for the clock input voltage to the right of the table. In particular, the clock pulse 50 is present during the period t_n to t_p . The time t_{n-} is prior to the beginning of the clock pulse, and t_{n+} is a time after t_n and before t_p .

Consider now the state of the circuit at t_{n-} when the R and S inputs are +V volts and zero, respectively. The R input biases transistor 70b "off" and biases transistor 80a "on", and the output B is zero volts (rows 1 and 2, FIGURE 7). The S input biases transistor 80b "off" and biases transistor 70d "on". Transistor 70c also is "on" at this time because of the ground potential at the trigger input terminal 98. Transistors 70c and 70d provide a low impedance path between the point 78 and the output terminal 92, whereby output A is +V volts (rows 1 and 2).

The clock pulse is applied at time t_n and biases transistors 70a and 70c "off". The output B does not change because transistor 80a is "on". In the right hand branch of the circuit only the transistor 70d is "on" when transistor 70c turns "off". The charge stored in transistor 70d and in the interelectrode capacitance between output terminal 92 and circuit ground maintains output A at +V volts because the transistors 70c and 80b are high impedance leakage paths. Some of this charge would leak off if the clock pulses were of long enough duration. However, it has been found that there is no perceptible change in the output A voltage under these conditions for a clock pulse of several microseconds duration. Thus, if the R and S inputs do not change while the clock pulse is being applied, the A and B outputs do not change at time t_{n+} (row 1).

Consider now the effect of reversing the R and S inputs at t_{n+} . The S ~~input~~ ^{input} now is +V volts, transistor 80b is biased "on", and the output A voltage falls to ground potential (row 2). The R input goes from +V volts to ground potential and biases "off" transistor 80a and biases "on" transistor 70b.

Transistor 70a is "off" because of the clock voltage. Transistor 70a presents a high impedance "open" circuit path between the terminal 88 and the positive terminal of the battery 90. Transistor 80a presents an "open" circuit between output terminal 88 and ground. Accordingly, there is very little current flow through these paths to charge or discharge the charge stored in previously "on" transistor 80a and the interelectrode capacitance between output terminal 88 and ground, whereby output B remains at ground potential (row 2). It is seen that the effect of changing the R and S input voltages is to change the output A from +V volts to ground potential.

By similar analysis it can be shown that output A is at ground potential and output B is at +V volts at t_{n-} when the R and S input voltages are zero and +V volts, respectively (rows 3 and 4), and that the A and B outputs do not change at t_{n+} if the R and S inputs do not change (row 3). It can also be shown that the output B voltage falls from +V volts to ground potential if the R and S inputs change from zero and +V to +V and zero, respectively, at t_{n+} (row 4).

A comparison of the A and B outputs at t_{n-} with the A and B outputs at t_{n+} indicates that an output voltage A or B can fall from +V volts to zero (rows 2 and 4) while the clock pulse is applied, but that an output voltage cannot rise from zero to +V volts. Advantage may be taken of this characteristic of the gate to provide a one stage per bit shift circuit.

It will be recalled from the description of the FIGURE 1 bistable circuit that the bistable circuit is only subject to being switched when a clock pulse is applied. It will also be recalled from that description that once the bistable circuit switches, both the RESET and SET inputs can change to ground potential, even during the clock period, without affecting the status of the bistable circuit. These characteristics of the bistable circuit are compatible with those of the gate circuit of FIGURE 6, and the two circuits can be connected as shown in FIGURE 8 to form a shift register, ring counter, and the like.

In the block diagram of FIGURE 8, three bistable circuits 110, 112 and 114 are illustrated. A first gate 116 has its R and S input terminals connected to the (1) and (0) output terminals, respectively, of first bistable circuit 110, and has its A and B output terminals connected to the R and S input terminals of the second bistable circuit 112. A second gate 118 is similarly connected between the output terminals of the second bistable circuit 112 and the input terminals of the third bistable circuit 114. All of the bistable circuits and gates have their trigger (T) terminals connected to a common bus bar 122 to which clock pulses 50 (or shift pulses) are applied.

Each of the bistable circuits 110 . . . 114

stores a binary bit "1" or "0" in the steady state, that is, when no clock pulse 50 is present. In the steady state, the outputs of gates 116 and 118 are determined by the outputs of bistable circuit 110, 112, respectively. Accordingly, when a clock pulse 50 is applied the second bistable circuit 112 assumes the pre-clock state of the first bistable circuit 110, and third bistable circuit 114 assumes the pre-clock state of second bistable circuit 112.

The outputs of a bistable circuit, the second bistable circuit 112 for example, change if the state of the bistable circuit changes. Moreover, the change in outputs may occur before the clock pulse terminates. In the latter event, the outputs of the next succeeding gate 118 will both be zero volts (rows 2 and 4, FIGURE 7) after the change. Before the outputs reach this value, however, the following bistable circuit 114 will have switched, if switching is called for by the pre-clock inputs thereto, or will at least be in the process of switching. As mentioned previously in describing the bistable circuit, both inputs to a bistable circuit can become zero volts, after switching commences, without affecting the bistable circuit.

It is not possible for both inputs i.e. S and R to a bistable circuit to be +V volts when the clock pulse is present. Due to the gate characteristics, therefore, a bistable circuit is rendered insensitive to change in the state of the preceding bistable circuit during the presence of a suitable clock pulse. Also, a bistable circuit cannot be switched after the clock pulse terminates. It is thus seen that there can be no "race" condition in the shift circuit arrangement.

WHAT WE CLAIM IS:—

1. A logic circuit comprising in combination first and second output terminals, first and second semiconductor amplifying devices of one conductivity type and a third semiconductor amplifying device of the opposite conductivity type, each of the devices having first and second electrodes defining a conduction path, and a control electrode for controlling the conductivity of the path, means connecting the second electrode of the first device to the first electrode of the second device, means connecting the second electrode of the second device and the second electrode of the third device to each other and to the first output terminal, fourth and fifth semiconductor amplifying devices of the first conductivity type and a sixth semiconductor amplifying device of the opposite conductivity type, means connecting the second electrode of the fourth device to the first electrode of the fifth device, means connecting the second electrodes of the fifth and sixth devices to each other and to the second output terminal, means for applying input sig-



Transistor 70a is "off" because of the clock voltage. Transistor 70a presents a high impedance "open" circuit path between the terminal 88 and the positive terminal of the battery 90. Transistor 80a presents an "open" circuit between output terminal 88 and ground. Accordingly, there is very little current flow through these paths to charge or discharge the charge stored in previously "on" transistor 80a and the interelectrode capacitance between output terminal 88 and ground, whereby output B remains at ground potential (row 2). It is seen that the effect of changing the R and S input voltages is to change the output A from +V volts to ground potential.

By similar analysis it can be shown that output A is at ground potential and output B is at +V volts at t_{n-} when the R and S input voltages are zero and +V volts, respectively (rows 3 and 4), and that the A and B outputs do not change at t_{n+} if the R and S inputs do not change (row 3). It can also be shown that the output B voltage falls from +V volts to ground potential if the R and S inputs change from zero and +V to +V and zero, respectively, at t_{n+} (row 4).

A comparison of the A and B outputs at t_{n-} with the A and B outputs at t_{n+} indicates that an output voltage A or B can fall from +V volts to zero (rows 2 and 4) while the clock pulse is applied, but that an output voltage cannot rise from zero to +V volts. Advantage may be taken of this characteristic of the gate to provide a one stage per bit shift circuit.

It will be recalled from the description of the FIGURE 1 bistable circuit that the bistable circuit is only subject to being switched when a clock pulse is applied. It will also be recalled from that description that once the bistable circuit switches, both the RESET and SET inputs can change to ground potential, even during the clock period, without affecting the status of the bistable circuit. These characteristics of the bistable circuit are compatible with those of the gate circuit of FIGURE 6, and the two circuits can be connected as shown in FIGURE 8 to form a shift register, ring counter, and the like.

In the block diagram of FIGURE 8, three bistable circuits 110, 112 and 114 are illustrated. A first gate 116 has its R and S input terminals connected to the (1) and (0) output terminals, respectively, of first bistable circuit 110, and has its A and B output terminals connected to the R and S input terminals of the second bistable circuit 112. A second gate 118 is similarly connected between the output terminals of the second bistable circuit 112 and the input terminals of the third bistable circuit 114. All of the bistable circuits and gates have their trigger (T) terminals connected to a common bus bar 122 to which clock pulses 50 (or shift pulses) are applied.

Each of the bistable circuits 110 . . . 114

stores a binary bit "1" or "0" in the steady state, that is, when no clock pulse 50 is present. In the steady state, the outputs of gates 116 and 118 are determined by the outputs of bistable circuit 110, 112, respectively. Accordingly, when a clock pulse 50 is applied the second bistable circuit 112 assumes the pre-clock state of the first bistable-circuit 110, and third bistable circuit 114 assumes the pre-clock state of second bistable circuit 112.

The outputs of a bistable circuit, the second bistable circuit 112 for example, change if the state of the bistable circuit changes. Moreover, the change in outputs may occur before the clock pulse terminates. In the latter event, the outputs of the next succeeding gate 118 will both be zero volts (rows 2 and 4, FIGURE 7) after the change. Before the outputs reach this value, however, the following bistable circuit 114 will have switched, if switching is called for by the pre-clock inputs thereto, or will at least be in the process of switching. As mentioned previously in describing the bistable circuit, both inputs to a bistable circuit can become zero volts, after switching commences, without affecting the bistable circuit.

It is not possible for both inputs i.e. S and R to a bistable circuit to be +V volts when the clock pulse is present. Due to the gate characteristics, therefore, a bistable circuit is rendered insensitive to ~~change~~ in the state of the preceding bistable circuit during the presence of a suitable clock pulse. Also, a bistable circuit cannot be switched after the clock pulse terminates. It is thus seen that there can be no "race" condition in the shift circuit arrangement.

WHAT WE CLAIM IS:—

1. A logic circuit comprising in combination first and second output terminals, first and second semiconductor amplifying devices of one conductivity type and a third semiconductor amplifying device of the opposite conductivity type, each of the devices having first and second electrodes defining a conduction path, and a control electrode for controlling the conductivity of the path, means connecting the second electrode of the first device to the first electrode of the second device, means connecting the second electrode of the second device and the second electrode of the third device to each other and to the first output terminal, fourth and fifth semiconductor amplifying devices of the first conductivity type and a sixth semiconductor amplifying device of the opposite conductivity type, means connecting the second electrode of the fourth device to the first electrode of the fifth device, means connecting the second electrodes of the fifth and sixth devices to each other and to the second output terminal, means for applying input sig-

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5 nals from a first source at the control electrode of the third device and at the control electrode of one of the first and second devices, means for applying input signals from
10 a second source at the control electrode of the sixth device and at the control electrode of one of the fourth and fifth devices, means for applying input signals from a third source at the control electrode of the other one of
15 the first and second devices and at the other one of the fourth and fifth devices and means for applying operating potential between the first electrodes of the first and third devices, and between the first electrodes of the fourth and sixth devices.

2. A circuit as claimed in claim 1, wherein each of the semiconductor amplifying devices is an insulated gate field-effect transistor.

20 3. A circuit as claimed in claim 1 or 2, further comprising seventh and eighth semiconductor amplifying devices of the one conductivity type, ninth, tenth, eleventh and twelfth semiconductor amplifying devices of the opposite conductivity type and first and
25 second points, wherein the conduction paths of the third and eleventh devices are connected in parallel with each other and in series with the conduction path of the ninth device, in that order, between the first point and
30 the first output terminal, the conduction paths of the sixth and twelfth devices are connected in parallel with each other and in series with the conduction path of the tenth device, in that order, between the first point and the
35 second output terminal, the conduction paths of the seventh and eighth devices are connected between the second point and the first and second output terminals, respectively, the conduction paths of the first and second devices are connected in series between the
40 second point and the first output terminal, the conduction paths of the fourth and fifth devices are connected in series between the second point and the second output terminal, the seventh and ninth devices are connected
45 to each other and to the second output terminal, the control electrodes of the eighth and tenth devices are connected to each other and to the first output terminal, a first input terminal common to the control electrodes of
50 the first and third devices, a second input terminal common to the control electrodes of the fourth and sixth devices and a third input terminal common to the control electrodes of the second, fifth, eleventh and twelfth
55 devices.

4. A circuit as claimed in claim 3, wherein all of the recited connections between the devices are by way of negligible impedance means.
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5. A circuit as claimed in claim 3 or 4, wherein when the circuit is a bistable storage stage, reset and set input signals are applied at the first and second input terminals, res-

pectively, and control signals are applied at the third input terminal. 65

6. A circuit as claimed in claim 1 or 2, further comprising first and second junction points, wherein the first electrode of the first device and the first electrode of the fourth
70 device are connected to the first junction point, the first electrode of the third device and the first electrode of the sixth device are connected to the second junction point, the first source of input signals is connected to
75 the control electrodes of the second and third devices, the second source of input signals is connected to the control electrodes of the fifth and sixth devices, the third source of input signals is connected to the control electrodes of the first and fourth devices and wherein the means for applying operating potential is connected to the first and second junction points.

7. A two stage shift register circuit including two bistable storage stages as claimed in claim 5, wherein the first output terminal of a first of the two bistable storage stages is connected to the second input terminal of a second of the two bistable storage stages and the second output terminal of the first bistable stage is connected to the first input terminal of the second bistable stage and wherein the third input terminals of said two stages are connected together. 85
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8. A single stage shift register comprising a plurality of bistable storage stages and a plurality of gate means interconnecting the storage stages in a cascaded chain; each of the storage stages including: first and second output terminals: first, second, third, fourth, fifth, and sixth transistors of one conductivity type, and seventh, eighth, ninth, tenth, eleventh and twelfth transistors of the opposite conductivity type, each transistor having first and second electrodes defining a conduction path, and a control electrode: first and second points of different operating potential; means connecting the conduction paths of the third and fourth transistors in parallel with each other and in series with the conduction path of the first transistor, in that order, between the first point and the first output terminal; means connecting the conduction paths of the fifth and sixth transistors in parallel with each other and in series with the conduction path of the second transistor, in that order, between the first point and the second output terminal; means connecting the conduction paths of the seventh and eighth transistors between the second point and the first and second output terminals, respectively; means connecting the control electrodes of the first and seventh transistors to each other and to the second output terminal; means connecting the control electrodes of the second and eighth transistors to each other and to the first output terminal; means connecting the conduction paths of the ninth and tenth transistors in
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series between the second point and the first output terminal; and means connecting the conduction paths of the eleventh and twelfth transistors in series between the second point and the second output terminal; each gate means including two points of different operating potential; first and second transistors of one conductivity type and a third transistor of the opposite conductivity type having their conduction paths connected in a series chain, in the order named, between said two points, with a point on the chain between the second and third transistors being connected to the control electrodes of the sixth and eleventh transistors in the next succeeding storage stage; fourth and fifth transistors of said one conductivity type and a sixth transistor of the opposite conductivity type having their conduction paths connected in a series chain, in the order named, between the said two points, with a point on the chain between the fifth and sixth transistors being connected to the control electrodes of the third and ninth transistors in the next succeeding storage stage; means connecting the first output terminal of a storage stage to the control electrode of said sixth transistor and to the control electrode of one of the fourth and fifth transistors in the next succeeding gate means; means con-

necting the second output terminal of a storage stage to the control electrode of the third transistor and to the control electrode of the one of the first and second transistors in the next succeeding gate means; means connecting the control electrode of the other one of the first and second transistors in each gate means, the control electrode of the other one of the fourth and fifth transistors of each gate means, and the control electrodes of the fourth, fifth, tenth and twelfth transistors in each storage stage to a common terminal; and means for applying control signals selectively at said common terminal.

9. The combination as claimed in claim 8, wherein all of the transistors are insulated-gate field-effect transistors, and wherein all of the recited connections are direct current connections of negligible impedance.

10. A logic circuit as claimed in claim 1 substantially as hereinbefore described with reference to and as illustrated in Figures 1 and 2, 3 and 4 or 6 and 7 of the accompanying drawings.

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