SEMICONDUCTOR DEVICE AND A METHOD THEREFOR

Field of the Invention

This invention relates, in general, to semiconductor devices and a method for forming thereof, and, more particularly, to semiconductor devices with dual gates and a method for forming thereof.

Background of the Invention

Polysilicon has traditionally been used as the gate electrode for MOS transistors. The polysilicon electrode is typically doped either P+ or N+ to match the doping of the source and drain regions in CMOS technology. As device dimensions shrink, however, problems exist with using polysilicon as a gate electrode. For example, as the dimensions of the P+ doped polysilicon gate electrode decrease, boron can penetrate from the polysilicon gate electrodes through the gate dielectric and decrease the reliability of the device. In addition, as dimensions shrink for both P+ and N+ doped polysilicon, doping concentrations increase. High temperature processes are performed in order to drive the dopants into the gate electrode. Due to scaling, the source and drain are shallower. Disadvantageously, the high temperature process can cause the source and drain to become deeper. If the high temperature is not performed, however, the dopants are more likely to reside away from the gate dielectric. Hence, there will be an area of the gate electrode that is not doped. This polydepletion effect will act as an

additional capacitance in series with the gate dielectric capacitance. In other words, it will undesirably increase the effective oxide thickness of the transistor. The polydepletion effect was not a significant effect in older technology, because the thickness of the polydepletion area was small compared to the gate dielectric effective thickness.

One solution is to use a material which has a work function approximately equal to the work function of either P doped or N doped silicon. P doped silicon has a work function of approximately 4.1 eV whereas N doped silicon has a work function of approximately 5.2 eV. The difficulty is to choose a material which is suitable to both these values. Another option is to use two different materials where one would be approximately equal to the work function of N doped silicon and the other approximately equal to the work function of P doped silicon. It is difficult to find two different materials with different work functions that have the chemical and thermo-stability necessary to be incorporated into a CMOS process flow. Therefore a need exists to find gate materials that are suitable for scaled devices.

Brief Description of the Drawings

The present invention is illustrated by way of example and not limitation in the accompanying figures, in which like references indicate similar elements, and in which:

FIG. 1 includes an illustration of a cross-sectional view of a portion of a semiconductor device substrate after forming gate dielectric and metal gate electrode layers.

FIG. 2 includes an illustration of a cross-sectional view of a portion of a semiconductor device substrate after patterning the metal gate layer.

FIG. 3 includes an illustration of a cross-sectional view of the substrate of FIG. 2 after forming a polysilicon layer.

FIG. 4 includes an illustration of a cross-sectional view of the substrate of FIG. 3 after patterning the polysilicon metal gate and gate dielectric layers.

FIG. 5 includes an illustration of a cross-sectional view of the substrate of FIG. 4 after forming a substantially completed device.

Skilled artisans appreciate that elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale. For example, the dimensions of some of the elements in the figures may be exaggerated relative to other elements to help improve the understanding of the embodiments of the present invention.

Detailed Description of the Drawings

The conduction band for silicon lies at 4.1eV below the vacuum level. The valence band lies approximately 1.1eV below the conduction band for silicon or at 5.2 eV below the vacuum level. The approximate 1.1eV difference between the valence and conduction bands of silicon is referred to as the band-gap. The mid-gap is approximately half of the band-gap and is approximately halfway between the conduction and valance bands of the material. A desirable work function for gate electrodes of N channel transistors is one which falls between the conduction band and mid-gap of the semiconductor substrate. A more desirable work function for N channel transistors is additionally at least 0.2 eV from the mid-gap. In other words, the more desirable work function for N channel transistor is between approximately 4.1 and 4.5 eV below vacuum level. A desirable work function for gate electrodes of P channel transistors is one which falls between the valence band and the mid-gap of the semiconductor substrate. A more desirable work function for P channel transistors is additionally at least 0.2 eV from the mid-gap or between approximately 4.9 and 5.2 eV below vacuum level.

FIG. 1 illustrates trench 20 within semiconductor substrate 10 to isolate the subsequently formed transistors. In a preferred embodiment, trench 20 is a shallow trench isolation region. Traditional etch and deposition processes for forming trench 20, as known to one skilled in the art are used. Semiconductor substrate 10 can be monocrystalline silicon, silicon germanium, gallium arsenic, silicon on insulator (SOI), or the like. In a first embodiment, semiconductor substrate 10 is P doped silicon. Silicon can be doped P type by doping the silicon with boron. In

this embodiment, well 30 is an N doped well. Well 30 can be doped N type by implanting arsenic, phosphorous or the like. Gate dielectric 40 is formed over semiconductor substrate 10. In one embodiment gate dielectric 40 is SiO_2. In this embodiment, the gate dielectric 40 is thermally grown to a thickness of approximately 15 to 50 Angstroms. One of ordinary skill in the art realizes as devices shrink the SiO_2 thickness may decrease below 15 Angstroms. In an alternate embodiment, gate dielectric 40 can be an oxide, especially a metal oxide, such as HfO_2, ZrO_2, Al_2O_3, La_2O_3, combinations thereof, or the like. If gate dielectric 40 is a metal oxide, it will typically be in the thickness of approximately 5-100 Angstroms, or more preferably less than 25 Angstroms. If gate dielectric 40 is a metal oxide, atomic layer deposition (ALD), chemical vapor deposition (CVD), physical vapor deposition (PVD), combinations thereof, or the like can be used for deposition.

Afterwards, metal gate layer 50 is deposited using ALD, CVD, PVD, combinations thereof, or the like. Metal gate layer 50 can be tantalum silicon nitride (TaSiN), platinum, ruthenium oxide, molybdenum nitride, tungsten silicon nitride, tantalum nitride, molybdenum silicon nitride, titanium silicon nitride, and tungsten nitride. Tantalum silicon nitride has been shown to be a suitable material for NMOS devices, and platinum and tungsten nitride for PMOS devices. In the preferred embodiment where metal gate layer 50 is TaSiN, the silicon or nitrogen concentration can be adjusted to change the work function of this material. For example increasing the concentration of silicon will decrease the work function of this material to approximately 4.4 eV.

Increasing the concentration of nitrogen is directly proportional to the work function. Thus increasing the nitrogen concentration can result in a work function of approximately 4.8 eV.

Turning to FIG. 2, semiconductor substrate 10 is patterned and metal gate layer 50 is etched. Metal gate layer 50 remains over the portion of semiconductor substrate that contains well 30. Metal gate layer 50 may also remain over a significant portion of trench 20. Etching chemistry similar to those used for etching polysilicon can be used for forming metal gate layer 50. Halogen-based chemistries such as carbon tetrafluoride (CF_4), hexafluoroethane (C_2F_6), hydrogen bromide (HBr), sulfur hexafluoride (SF_6), hydrogen chloride (HCl), molecular chlorine (Cl_2), or the like can be used during plasma etching, reactive ion etching, electron cyclotron resonance etching or microwave etching. After metal gate layer 50 has been patterned the photoresist layer is removed using conventional methods, such as exposing the photoresist to an oxygen-containing environment. Metal gate layer 50 is approximately greater than or equal to 50 Angstroms. Typically, the etch is performed using endpoint detection. A timed etched can also be performed.

Turning to FIG. 3, second gate electrode 60 is formed. In the first embodiment, second gate electrode 60 is a doped silicon layer. Silicon gate 60 includes deposited amorphous silicon or polysilicon and is doped either in situ or during a separate doping step. In this particular embodiment the thickness of second gate electrode 60 is approximately 1000 – 2000 Angstroms thick. Optionally, an antireflective coating (ARC) can be formed over doped silicon layer 60.

A photoresist layer is deposited over doped silicon layer 60. The same etched chemistries and processes used to previously etch metal gate layer 50 can be used to etch second gate electrode 60 and metal gate layer 50. If gate dielectric 40 is SiO2, a wet etch of dilute HF can be used. Typically the concentration of water to HF is 100:1. If gate dielectric 40 is a metal oxide, HF or phosphoric acid is used. The resulting structure is shown in FIG. 4 with metal gate layer and second gate electrode 60 forming a metal/gate or gate stack. If second gate electrode 60 is silicon then the stack is a metal/silicon gate stack. In one embodiment the metal/silicon gate stack is a tantalum silicon nitride gate portion over a silicon gate portion.

Processing continues to form the rest of the semiconductor device as illustrated in FIG. 5. Source and drain 80 are formed during ion implantation. In this first embodiment, source and drain 80 will be N doped, whereas source and drain 81 will be P doped. Spacers 70 are formed surrounding the gate electrodes and gate dielectric. Typically the spacers are formed of nitride. CMOS processing, known to one of ordinary skill in the art, is continued from this point.

Although the first embodiment invention has been described with respect to specific doping types, skilled artisans appreciate that doping types may be reversed. For example, semiconductor substrate 10 can be N doped and well 30 can be P doped. In this case, the silicon electrode will be over the P doped well and the metal/silicon stack electrode will be over the N doped region.

In the second embodiment, a stack consisting of a semiconductor material and a metal will be formed over the P type substrate or a P

well, and a semiconductor gate will be formed over an N well. This can be performed by making semiconductor substrate 10 N doped and well 30 P doped. Or if the semiconductor substrate 10 is P type, the metal/silicon stack will be formed over semiconductor substrate 10 and the gate electrode alone will be formed over well 30. In this embodiment the semiconductor electrode is P doped silicon germanium. All etch and formation processing that has been discussed in regards to the first embodiment can be used in the second embodiment.

It is advantageous to use a metal electrode for either an N channel or P channel transistors and a silicon electrode for the other. This allows the reuse of silicon processes and tools that are already established in the semiconductor field. In addition, it eliminates the necessity to find two different materials with good chemical and thermo-stability with desirable work functions for N channel and P channel transistors. Furthermore, one material with the two different work functions is not needed.

In the foregoing specification, the invention has been described with reference to specific embodiments. However, one of ordinary skill in the art appreciates that various modifications and changes can be made without departing from the scope of the present invention as set forth in the claims below. Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of present invention.

Benefits, other advantages, and solutions to problems have been described above with regard to specific embodiments. However, the

benefits, advantages, solutions to problems, and any element(s) that may cause any benefit, advantage, or solution to occur or become more pronounced are not to be construed as a critical, required, or essential feature or element of any or all the claims. As used herein, the terms "comprises," "comprising," or any other variation thereof, are intended to cover a non-exclusive inclusion, such that a process, method, article, or apparatus that comprises a list of elements does not include only those elements but may include other elements not expressly listed or inherent to such process, method, article, or apparatus.

What is claimed is:

1. A method of forming a semiconductor device, comprising:

providing a semiconductor substrate having a first doped region and a second doped region;

providing a dielectric over the first doped region and a second doped region;

providing a metal layer over the dielectric, wherein the metal layer comprises tantalum, silicon and nitrogen;

patterning the metal layer to leave a metal portion over at least a portion of the first doped region;

forming a silicon layer over the metal portion and the second doped region; and

patterning the silicon layer and the metal portion to leave a silicon gate over the second doped region and a metal/silicon gate stack over the first doped region.

2. The method of claim 1, wherein the silicon layer is in situ doped with one or more of arsenic and phosphorus.

3. The method of claim 1, wherein the silicon layer is in situ doped with germanium.

4. The method of claim 3, wherein the silicon layer is boron doped.

5. The method of claim 1, wherein the semiconductor substrate has a valence band and a conduction band with a mid-gap that is half way therebetween, and the metal layer has a work function that is between the valence band and the mid-gap.

6. The method of claim 1, wherein the semiconductor substrate has a valence band and a conduction band with a mid-gap that is half way therebetween, and the metal layer has work function that is between the valence band and the conduction band and is at least 0.2 eV from the mid-gap.

7. The method of claim 1, wherein the semiconductor substrate has a valence band and a conduction band with a mid-gap that is half way therebetween, and the metal layer has a work function that is between the conduction band and the mid-gap.

8. A semiconductor device, comprising:

a semiconductor substrate comprising a first doped region and a second doped region;

a first gate dielectric over the first doped region;

a metal/silicon gate stack over the first gate dielectric, wherein the metal/silicon gate stack comprises a metal portion over the first gate dielectric and a polysilicon portion over the metal portion;

a second gate dielectric over the second doped region; and

a silicon gate over the second gate dielectric.

9. A method of making a semiconductor device, comprising:

providing a semiconductor substrate having a first doped region and a second doped region;

providing a dielectric layer over the first doped region and a second doped region;

providing a tantalum silicon nitride layer over the dielectric layer;

patterning the tantalum silicon nitride layer to leave a tantalum silicon nitride portion over at least a portion of the first doped region;

forming an in situ doped silicon layer over the tantalum silicon nitride portion and the second doped region; and

patterning the in situ doped silicon layer and the tantalum silicon nitride portion to leave a silicon gate over the second doped region and a gate stack over the first doped region wherein the gate stack comprises a tantalum silicon nitride gate portion over a silicon gate portion.

10. A method for forming a transistor comprising:

forming an insulating layer;

forming a portion of the transistor control electrode overlying the insulating layer by atomic layer deposition, wherein the transistor control electrode comprises a first element and a second element and comprising:

depositing the first element;

depositing the second element after the first element; and

one of changing the concentration of the first element while depositing the first element and changing the second element while depositing the second element; and

choosing one of the first element and the second element to change the concentration based upon a conductivity of a channel of the transistor.