POLY PROFILE ENGINEERING TO MODULATE SPACER INDUCED STRESS FOR DEVICE ENHANCEMENT

ABSTRACT OF THE DISCLOSURE

The present invention provides a method of inducing stress in a semiconductor device substrate by applying an ion implantation to a gate region before a source/drain annealing process. The source/drain region may then be annealed along with the gate which will cause the gate to expand in certain areas due to said ion implantation. As a result, stress caused by said expansion of the gate is transferred to the channel region in the semiconductor substrate.

Figure 1a