ABSTRACT OF THE DISCLOSURE

LOW DIELECTRIC CONSTANT DIELECTRIC LAYER FABRICATION METHOD EMPLOYING HARD MASK LAYER DELAMINATION

A method for forming, within a low dielectric constant dielectric layer formed upon a substrate employed within a microelectronics fabrication, a conductor pattern employing a hard mask cap layer. There is first provided a substrate having conductor regions formed therein upon which is formed a low dielectric constant dielectric layer. There is then formed over the substrate a silicon containing hard mask cap layer. There is then formed over the hard mask cap layer a patterned photoresist etch mask layer. There is then subtractively etched employing the patterned photoresist etch mask layer and a first subtractive etching environment the pattern into the hard mask layer. There is then subtractively etched employing the patterned hard mask layer and a second etching environment the pattern into the low dielectric constant dielectric layer, simultaneously stripping the photoresist etch mask layer. There is then removed by delamination the hard mask cap layer employing a chemical treatment, leaving a trench pattern in the low dielectric constant dielectric layer.

The trench pattern may be filled with a microelectronics material to form a patterned layer around which is a maximized amount of low dielectric constant dielectric material. The order of filling with microelectronics material and delamination of the hard mask layer may be reversed if desired to minimize the amount of patterned microelectronics material remaining above the substrate surface, in which case the method is a lift off method for patterning a microelectronics layer. After filling and patterning, the substrate surface may be planarized for further processing and optional additional microelectronics layers formed thereover.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)