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A METHOD TO FABRICATE A SINGLE GATE WITH DUAL WORK-FUNCTIONS

BACKGROUND OF THE INVENTION

(1) FIELD OF THE INVENTION

The present invention relates to the fabrication of integrated circuit devices, and more particularly, to a method of fabricating a single gate having dual work-functions in the fabrication of integrated circuits.

(2) DESCRIPTION OF THE PRIOR ART

As technology progresses, enabling higher levels of integration within system integrated circuit chips, it will be essential to be able to fabricate semiconductor device gates that accommodate different work-functions within a single gate across a short device channel. Many mature methods can be used to fabricate such gates, either metal or silicon. However, these processes might be cumbersome or expensive.

U.S. Patent 5,770,490 to Frenette et al discloses a dual work-function device wherein different gates have different work-functions depending on doping. U.S. Patent 6,187,657 to Xiang et al shows a gate composed of dual

gate materials. U.S. Patent 5,620,906 to Yamaguchi et al teaches ion doping to form source/drain regions. U.S. Patents 5,530,265 to Takemura and 6,235,574 to Tobben et al show doping processes.

SUMMARY OF THE INVENTION

Accordingly, a primary object of the invention is to provide a process for forming a single gate having dual work-functions in the fabrication of integrated circuits.

A further object of the invention is to provide a process for forming a single gate having a dual work-function by means of plasma enhanced ion doping in the fabrication of integrated circuits.

Another object of the invention is to provide a process for forming a single gate having a dual work-function by means of selective plasma enhanced ion doping.

In accordance with the objects of the invention, a method for forming a single gate having a dual work-function is achieved. A gate electrode is formed overlying a gate dielectric layer on a substrate. Sidewalls of the gate electrode are selectively doped whereby the doped

sidewalls have a first work-function and whereby a central portion of the gate electrode not doped has a second work-function to complete formation of a single gate having multiple work-functions in the fabrication of integrated circuits.

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings forming a material part of this description, there is shown:

Figs. 1 through 4 are cross-sectional representations of a preferred embodiment of the present invention.

Figs. 3A through 3C are cross-sectional representations of three alternatives in a preferred embodiment of the present invention.

Fig. 5 is a cross-sectional representation of a combination of alternatives in a preferred embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention proposes a simple and relatively inexpensive method to fabricate a single gate having a dual work-function across the device channel. The sidewalls of the gate are selectively doped via plasma doping with appropriate masking. The extent and profile of the doped sidewall is determined by the ion density, pressure, and annealing duration. During doping, the substrate is not biased so as to eradicate plasma induced damage. Because of the selective doping, the gate portion at the sidewalls will possess different properties from the central bulk gate. This will mean that the sidewall portions will have a different work-function across the device channel than will the central bulk gate.

Referring now more particularly to Fig. 1, there is shown a semiconductor substrate 10. This is preferably monocrystalline silicon. A gate dielectric oxide layer 14 is grown or deposited over the substrate to a thickness of between about 10 and 100 Angstroms. The gate dielectric layer may be a high dielectric constant (k) material such as silicon nitride, HfO_2, ZrO_2, Ta_2O_5, and so on, or silicon dioxide or a stack of high-k materials and silicon dioxide, depending on the gate material and other

design considerations. Now, a gate material layer 16 is deposited over the gate dielectric layer to a thickness of between about 1000 and 3000 Angstroms. The gate material may comprise polysilicon, amorphous silicon, or metal, for example.

A mask 20 is formed over the gate material layer 16. The gate material layer is patterned to form a gate electrode 18, as shown in Fig. 2, using a dry etch, for example.

Now, the gate is doped by plasma enhanced ion doping (PEID). In one alternative, shown in Fig. 3A, the mask 20 remains on the gate. The mask shields the top portion of the gate 18 from the plasma doping. PEID is an isotropic doping process that will dope the gate without implantation induced damage. The gate dielectric acts as a shield for the substrate during doping. The sidewalls 24 of the gate 18 are doped with dopants in the plasma. The ion density, duration, and pressure of the doping process will determine the extent and the profile of the doped sidewall gate. For example, pressure may be maintained at between about 1 and 740 Torr and the doping duration may be between about 5 and 200 seconds. The doping profile after PEID is uniform.

After doping, an annealing is performed to drive-in the dopants. The duration of the annealing step also plays a part in determining the depth of dopant diffusion into the gate. For example, the annealing preferably is performed under a N_2 ambient at between about 800 and 1000 °C for 15 to 30 minutes.

Fig. 3B illustrates the alternative in which the mask 20 is removed before the plasma doping step. In this case, a top portion as well as the sidewall portions of the gate 18 are doped 24.

During the doping step, the substrate is not biased. This will reduce the occurrence of plasma induced damage. If the gate material is polysilicon or amorphous silicon, for example, the dopant ions may be germanium ions, nitrogen ions, oxygen ions, metallic ions, and so on. If the gate material is a metal such as titanium nitride, tungsten, ruthenium and so on, silicon ions or germanium ions may be used as dopants.

The work-function of the central bulk gate 18 and the work-function of the doped gate 24 will be different. The difference in work-function will depend upon the dopant concentration and annealing duration.

It should be noted that if germanium, for example, is doped on the top portion of the gate (as in Fig. 3B), there may be a concern during subsequent silicidation.

In a further alternative, the mask 20 may be removed before doping and a second mask 25 may be formed over the gate to shield all except one side portion of the gate as shown in Fig. 3C. In this case, the plasma enhanced ion doping is restricted to just one side of the gate. This implies that the channel beneath the doped sidewall gate experiences a different work-function than the other portions of the gate.

Fig. 4 illustrates the channel portion 30 under the doped sidewall 24 of the gate. This small part of the channel that experiences a different work-function may be used for other specific purposes such as hot carrier injection (HCI), for example. The portion of the channel underlying the doped region can be engineered for HCI to be between about 20 and 100 nm, for example, depending upon the width of the doped portion of the gate 24. Electrons 40 and hot carrier injection 42 are illustrated in Fig. 4, for example.

Combinations of the alternatives shown in Figs. 3A through 3C may be used to achieve multiple work functions in the single gate. For example, alternative A may be used to form doped portion 24 of the gate 18. Then alternative C may be used as shown in Fig. 5 to dope the another portion 25 of the gate. In this example, the gate has three work-functions - one under the undoped gate 18, a second work-function under the doped portion 24, and a third work-function under the doped portion 26.

This completes formation of a single gate having multiple work-functions.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

What is claimed is:

1. A method of forming a single gate having multiple work-functions in the fabrication of integrated circuits comprising:

forming a gate electrode overlying a gate dielectric layer on a substrate; and

selectively doping sidewalls of said gate electrode whereby said doped sidewalls have a first work-function and whereby a central portion of said gate electrode not doped has a second work-function to complete formation of a single gate having multiple work-functions in the fabrication of integrated circuits.

2. The method according to Claim 1 wherein said gate material layer is selected from the group consisting of: polysilicon, amorphous silicon, and metal.

3. The method according to Claim 1 wherein said gate dielectric is selected from the group consisting of: silicon dioxide, high dielectric constant (k) dielectric materials, and a combination of silicon dioxide and high k dielectric materials.

4. The method according to Claim 1 wherein said step of selectively doping said sidewalls comprises plasma enhanced ion doping.

5. The method according to Claim 1 wherein said step of selectively doping said sidewalls comprises masking a top portion of said gate electrode whereby said dopants dope said sidewalls of said gate electrode and do not dope said top portion and said central portion of said gate electrode.

6. The method according to Claim 1 wherein in said step of selectively doping said sidewalls, said dopants dope said sidewalls of said gate electrode and a top portion of said gate electrode and do not dope said central portion of said gate electrode.

7. The method according to Claim 1 wherein said step of selectively doping said sidewalls comprises masking a top portion and one sidewall of said gate electrode whereby said dopants dope one of said sidewalls of said gate electrode not masked and do not dope said top portion, said central portion, and said masked sidewall of said gate electrode.

8. The method according to Claim 1 wherein said gate material comprises silicon and wherein said step of selectively doping said sidewalls comprises doping with ions chosen from the group consisting of: germanium

ions, nitrogen ions, oxygen ions, and metallic ions.

9. The method according to Claim 1 wherein said gate material comprises metal and wherein said step of selectively doping said sidewalls comprises doping with ions chosen from the group consisting of: silicon ions and germanium ions.

10. The method according to Claim 1 wherein during said doping step, said substrate is not biased.

11. The method according to Claim 1 further comprising annealing said substrate after said doping step to drive-in said dopants.

12. The method according to Claim 1 wherein each of said sidewalls of said gate is doped differently and wherein one of said sidewalls has said first work-function and wherein another of said sidewalls has a third work-function.

13. A method of forming a single gate having multiple work-functions in the fabrication of integrated circuits comprising:

forming a gate electrode overlying a gate

dielectric layer on a substrate; and

selectively doping sidewalls of said gate electrode using plasma enhanced ion doping whereby said doped sidewalls have a first work-function and whereby a central portion of said gate electrode not doped has a second work-function to complete formation of a single gate having multiple work-functions in the fabrication of integrated circuits.

14. The method according to Claim 13 wherein said gate material layer is selected from the group consisting of: polysilicon, amorphous silicon, and metal.

15. The method according to Claim 13 wherein said gate dielectric is selected from the group consisting of: silicon dioxide, high dielectric constant (k) dielectric materials, and a combination of silicon dioxide and high k dielectric materials.

16. The method according to Claim 13 wherein said step of selectively doping said sidewalls comprises masking a top portion of said gate electrode whereby said dopants dope said sidewalls of said gate electrode and do not dope said top portion and said central portion of said gate electrode.

17. The method according to Claim 13 wherein in said step of selectively doping said sidewalls, said dopants dope said sidewalls of said gate electrode and a top portion of said gate electrode and do not dope said central portion of said gate electrode.

18. The method according to Claim 13 wherein said step of selectively doping said sidewalls comprises masking a top portion and one sidewall of said gate electrode whereby said dopants dope one of said sidewalls of said gate electrode not masked and do not dope said top portion, said central portion, and said masked sidewall of said gate electrode.

19. The method according to Claim 13 wherein said gate material comprises silicon and wherein said step of selectively doping said sidewalls comprises doping with ions chosen from the group consisting of: germanium ions, nitrogen ions, oxygen ions, and metallic ions.

20. The method according to Claim 13 wherein said gate material comprises metal and wherein said step of selectively doping said sidewalls comprises doping with ions chosen from the group consisting of: silicon ions and germanium ions.

21. The method according to Claim 13 wherein during said doping step, said substrate is not biased.

22. The method according to Claim 13 further comprising annealing said substrate after said doping step to drive-in said dopants.

23. The method according to Claim 13 wherein each of said sidewalls of said gate is doped differently and wherein one of said sidewalls has said first work-function and wherein another of said sidewalls has a third work-function.

24. A method of forming a single gate having multiple work-functions in the fabrication of integrated circuits comprising:

forming a gate electrode overlying a gate dielectric layer on a substrate;

selectively doping sidewalls of said gate electrode using plasma enhanced ion doping wherein said substrate is not biased whereby said doped sidewalls have a first work-function and whereby a central portion of said gate electrode not doped has a second work-function; and

annealing said substrate to drive-in said dopants to complete formation of a single gate having multiple

work-functions in the fabrication of integrated circuits.

25. The method according to Claim 24 wherein said gate material layer is selected from the group consisting of: polysilicon, amorphous silicon, and metal.

26. The method according to Claim 24 wherein said step of selectively doping said sidewalls comprises masking a top portion of said gate electrode whereby said dopants dope said sidewalls of said gate electrode and do not dope said top portion and said central portion of said gate electrode.

27. The method according to Claim 24 wherein in said step of selectively doping said sidewalls, said dopants dope said sidewalls of said gate electrode and a top portion of said gate electrode and do not dope said central portion of said gate electrode.

28. The method according to Claim 24 wherein said step of selectively doping said sidewalls comprises masking a top portion and one sidewall of said gate electrode whereby said dopants dope one of said sidewalls of said gate electrode not masked and do not dope said top

portion, said central portion, and said masked sidewall of said gate electrode.

29. The method according to Claim 24 wherein said gate material comprises silicon and wherein said step of selectively doping said sidewalls comprises doping with ions chosen from the group consisting of: germanium ions, nitrogen ions, oxygen ions, and metallic ions.

30. The method according to Claim 24 wherein said gate material comprises metal and wherein said step of selectively doping said sidewalls comprises doping with ions chosen from the group consisting of: silicon ions and germanium ions.

31. The method according to Claim 24 wherein each of said sidewalls of said gate is doped differently and wherein one of said sidewalls has said first work-function and wherein another of said sidewalls has a third work-function.