ENHANCED STRUCTURE AND METHOD FOR BURIED LOCAL INTERCONNECTS

Technical Field

The present invention relates to semiconductor front end of line (FEOL) processing and more specifically to a buried local interconnect formed at the transistor level.

Background Art

In microelectronics industry, there is a continued need for dense, high speed and yet miniaturized microcircuits, particularly for memory cells and support circuits. Different solutions have been implemented to achieve maximum density, speed and desired size requirements.

In semiconductor processing, formerly specialized techniques such as Silicon-on-Insulator (SOI) are being used more widely, to help meet the demand for high-speed integrated circuits. In SOI technology, a relatively thin layer of semiconductor material, usually silicon (Si), generally overlays a layer of insulating material referred to as buried oxide (BOX). This relatively thin layer of semiconductor material is generally the area wherein active devices are formed in SOI devices.

Integrated circuits are manufactured with a large number of electronic semiconductor devices, such as resistors, transistors, diodes, and capacitors, which are fabricated in a combined process together on a semiconductor substrate. A substrate refers to one or more semiconductor layers or structures which includes active or operable portions of semiconductor devices. An important aspect of manufacturing integrated circuits is to electrically interconnect the active devices therein through interconnect structures.

The interconnect structure generally comprises a region of conducting material that is formed between the semiconductor devices that are being placed in electrical contact. The interconnect serves as a conduit for delivering electrical current between semiconductor devices. Specific types of interconnect structures are known to those skilled in the art and can include M0, M1 wiring

level local interconnects, buried contacts, vias, studs, surface straps and buried straps to name a few. Diodes can sometimes also function as interconnects between semiconductor devices. A diode can be formed in a semiconductor substrate by joining active regions of different carrier types.

One type of frequently used interconnect structure is the buried contact. The buried contact may be a region of polysilicon that makes direct contact between the interconnect structure and the active region, eliminating the need for a metal link. In forming the buried contact, a window is opened in a thin gate oxide over the active region that the interconnect structure is to electrically connect. Thereafter, the polysilicon is deposited in direct contact with the active region in the opening, but is isolated from the underlying silicon of the active region by gate oxide and by field oxide in other parts of the semiconductor substrate. An ohmic contact is formed at the interface between the polysilicon and the active region by diffusion into the active region of a dopant preset in the polysilicon. The dopant diffusion into the active region, in effect, merges the polysilicon with the active region. A layer of insulating film is then deposited to cover the buried contact. The buried contact is so termed because a metal layer can cross over the active region forming the buried contact without making an electrical connection to the buried contact.

In certain instances, to allow for the increasing density of the circuits involved, multiple layers of metal interconnects are stacked on top of each other. Typically, each consecutive metal layer has a reduced density of elements. Such hierarchy in the density is due to mask overlay error which accumulates with each additional interconnect layer. For example, if a contact is needed between the active area (AA) and the second metal layer (M2), one has to create a via between the AA and a first metal layer (M1) and then create a second via to interconnect M1 to M2. The overall overlay tolerance for the AA to M2 contact is the sum of the tolerances for the AA-to-M1 and the M1-to-M2 contacts. Therefore, the ability to increase circuit density by adding layers of interconnects is limited.

In many instances, providing for adequate manufacturing tolerances while meeting the size, speed and density requirements can be a challenging task. A

new structure is needed to allow for increased circuit density, while keeping manufacturing tolerances at workable levels.

Disclosure of the Invention

According to an aspect of the invention, a structure and method is provided for forming a buried interconnect of an integrated circuit in a single crystal semiconductor layer of a substrate. The buried interconnect is formed of a deposited conductor and has one or more vertical sidewalls which contact a single crystal region of an electronic device formed in the single crystal semiconductor layer.

According to another aspect of the invention, a method for forming a buried interconnect is provided which comprises: forming a trench isolation region in a substrate; forming a trench in a single crystal region of the substrate which abuts the isolation region, wherein the trench has a bottom isolated from the single crystal region, and a sidewall abutting the trench isolation region; then depositing a conductor in the trench, the conductor contacting the single crystal region on at least one sidewall of the trench; and forming a contact to the deposited conductor from above.

Brief Description of The Drawings

Figures 1, 9 and 10 illustrate buried interconnect structures according to alternative embodiments of the invention.

Figures 2 through 8 illustrate stages in fabrication of a buried interconnect structure according to embodiments of the invention.

Best Mode for Carrying Out the Invention

Figure 1 illustrates a buried interconnect structure according to a silicon-on-insulator (SOI) embodiment of the invention. As shown in Figure 1, a buried interconnect 10 is formed in a single crystal semiconductor layer (SOI layer 12)

of an SOI substrate having a buried oxide layer (BOX 14) overlying a supporting substrate 16. Buried interconnect 10 has a generally vertically oriented (hereinafter referred to as "vertical") sidewall 18 which contacts a single crystal region 12 of an electronic device 20, which may be, for example, a transistor, diode, capacitor, or resistor, which is formed in the SOI layer 12.

When the electronic device 20 is an insulated gate field effect transistor (IGFET), the vertical sidewall 18 of the buried interconnect 10 may directly contact the body or a diffusion region (e.g. source/drain diffusion region) of the electronic device 20, formed in SOI layer 12. When the electronic device 20 is a diode or a depletion capacitor, the vertical sidewall 18 of the buried interconnect 10 may contact a diffusion region of such device.

The buried interconnect 10 is fashioned to extend in a direction generally parallel to the substrate 16 (extending in a direction into and out of the page in Figure 1). In this manner, buried interconnect 10 passes next to other single crystal regions 12 of the substrate where it may contact one or more single crystal regions 12 of other electronic devices through vertical sidewall 18 or other sidewall where it is not isolated. An isolation region 28 (for example, a trench isolation), extending at least part of the length of buried interconnect 10 in a direction into and out of the page, isolates buried interconnect 10 along sidewall 30 from other electronic devices except where contact is desired. Where contact to other electronic devices is desired, contact may be made along portions of sidewall 30 where isolation region 28 is not present.

The buried interconnect 10 is formed of a deposited conductor such as polysilicon, a metal silicide (e.g. WSi_x, $CoSi_x$, $TiSi_x$, deposited polysilicon followed by a subsequent metal deposition and self-aligned silicidation, or even a deposited metal, which may preferably be tungsten (W) or other refractory metal or titanium (Ti), niobium (Nb), zirconium (Zr), tantalum (Ta), molybdenum (Mo), or layers thereof The buried interconnect may be lined with a liner 32 comprising a nitride of the deposited conductor metal or nitride of similar metal, e.g tungsten nitride, or titanium nitride or tantalum silicon nitride (TaSiN) Alternatively, especially when the deposited conductor is polysilicon, a very thin

layer (e.g. 7 Å or less) of silicon nitride may be used, as described more fully below.

The buried interconnect 10 is preferably conductively coupled to a conductive line 22 formed above the substrate, the conductive line 22 being a polysilicon conductor, for example, which may form the gate conductor or "polyconductor" of an MOS device 24 (that is an "MOS", i.e. insulated gate, field effect transistor, or MOS capacitor), the gate conductor overlying a gate dielectric 26 formed over the SOI layer 12. Polyconductor 22 is shown in Figure 1 linking an MOS device, e.g. MOSFET 24 as a gate conductor to the source/drain region 20 of another electronic device, e.g. another MOSFET. MOSFETs may be linked in such manner where cross-coupled CMOSFET pairs are used, as in a multitude of latches, flip-flops, drivers, or even static random access memory (SRAM).

Alternatively, polyconductor 22 can be patterned to extend only over the STI 28 and oxide 46, merely as an interface to buried interconnect 10. As another alternative, the polyconductor 22 may extend over a gate dielectric of a MOSFET device 20, the body of which the buried interconnect 10 conductively contacts through sidewall 18. In such case, the body of the MOSFET 20 would be tied to the same voltage as the gate conductor 22. Such gate and body interconnection allows the MOSFET 20 to be operated as a variable threshold voltage device in which the threshold voltage decreases as the gate conductor voltage increases.

Figure 1A is a top-down view illustrating an exemplary semiconductor device layer layout having buried interconnects formed according to the present invention. In such layout, areas 110 and 210 represent buried interconnects and areas 120 and 220 represent active areas of the substrate. In the example shown, n-channel IGFETs (NFETs) are preferably formed in active area 120, and p-channel (PFETs) are preferably formed in active area 220. Polyconductors 122, 222 and 322 are shown crossing over portions of active areas 120 and 220, as gate conductors of the NFETs and PFETs therein. A first buried interconnect 110 has one or more sidewalls 118, 119 making contact to a source/drain region of an NFET in a single crystal region (active area 120). Buried interconnect 110

also has sidewalls 218, 219 making contact to a source/drain region of another device, a PFET, in a single crystal region (active area 220). Thus, it will be understood that a single buried interconnect has one or more sidewalls which contact one or more single crystal regions of a plurality of electronic devices (e.g. NFETs and PFETs). A buried contact 148 is formed between the polyconductor 222 and the buried interconnect 110 to establish a conductive interconnection to the polyconductor 222.

Similarly, a second buried interconnect 210 has one or more sidewalls 318, 319 making contact to a source/drain region of an electronic device, an NFET, in a single crystal region (active area 120). Buried interconnect 210 also has sidewalls 418, 419 making contact to a source/drain region of another device, a PFET, in a single crystal region (active area 220). A buried contact 248 is formed between the polyconductor 122 and the buried interconnect 210 to establish a conductive interconnection to polyconductor 122.

Figures 2 through 7 illustrate stages in fabrication of a buried interconnect 10 as shown in Figure 1 in an SOI process embodiment. As shown in Figure 2, a shallow trench isolation region (STI 28) is formed in an SOI layer 12 of the substrate having a buried oxide layer (BOX 14) overlying a supporting substrate 16. The STI 28 extends to the BOX layer 14 in order to isolate electronic devices formed in SOI layer 12 on respective sides thereof. A pad nitride 34 covers SOI layer 12 in locations other than STI 28.

Next, as shown in Figure 3, a photoresist is deposited and patterned to form a mask 36, and an opening 35 is etched which abuts STI 28 on at least one side, and SOI layer 12 on at least one other side, preferably using a directional, reactive ion etch (RIE). This etch may be timed, or is preferably stopped when the supporting substrate 16 is reached. The mask 36 is then removed. The exposed sidewall 13 of SOI layer 12 may be passivated at this time, to remove surface damage to the single crystal SOI layer, as by a timed sidewall oxidation and subsequent oxide removal.

Then, as shown in Figure 4, an oxide is deposited, preferably by high density plasma deposition, to form an isolating layer 38 at the bottom of the trench and oxide 40 on the surface. Oxide adhering to sidewall 13 of opening 35

is removed at this time (e.g. by an isotropic etch), including any oxide resulting from the optional passivation process described above. Then, as illustrated in Figure 5, a conductor 44 is deposited to fill the opening 35, preferably after first lining the opening by depositing a liner 32. A variety of materials may be deposited as conductor 44, among which are polysilicon, metals including tungsten (W), niobium (Nb), zirconium (Zr), tantalum (Ta), molybdenum (Mo) and silicides and nitrides of such metals, or layers thereof. When the conductor 44 is formed by depositing a refractory metal such as tungsten, the liner 32 is preferably formed by depositing a material which promotes adhesion, such as tungsten nitride or titanium nitride.

When the polysilicon is deposited to form conductor 44, it is preferably highly doped as deposited, but, alternatively, may be doped in situ following deposition. When the conductor 44 is formed of polysilicon, a liner 32 may not be required for adhesion. However, it may still be preferable, for other reasons, to line the opening 35 with a barrier of either a conductive material, or even a very thin layer of silicon nitride. A very thin layer of silicon nitride, for example, 7 Å or less, is known to be conductive because of quantum tunneling through the very thin layer. Such barrier layer would act to retard the diffusion of dopants from the polysilicon into the adjacent SOI region 12, and/or inhibit the recrystallization of the polysilicon at the interface between conductor 44 and SOI region 12. Recrystallization should be avoided because it can potentially cause crystal defects in the SOI region 12, ultimately worsening the performance of electronic devices formed therein.

After the conductor 44 is deposited, the substrate is planarized to the level of pad nitride 34 through a process such as chemical mechanical polishing (CMP) selective to nitride, to clear the deposited conductor and deposited oxide from the top surface of the substrate, resulting in a structure as shown in Figure 5. The conductor 44 and liner 32 are then recessed, preferably by a directional etch such as reactive ion etching selective to oxide and nitride, resulting in the structure as shown in Figure 6.

Then, as illustrated in Figure 7, a top oxide layer 46 is formed above conductor 44. This is performed preferably by depositing oxide by a high density

plasma process, and then planarizing the oxide 46 to the level of the pad nitride 34 (as by CMP selective to nitride), and then clearing the remaining pad nitride 34 from the SOI region 12.

Next, referring again to the completed structure shown in Figure 1, further processing is done to form a buried contact 48 from a polyconductor 22. Polyconductor 22 may be, but need not be a gate conductor of one or more electronic devices located in SOI regions 12. This process is preferably performed after performing any necessary ion implants to device 24, and optionally to device 20, and forming a gate dielectric 26, either by oxidation or deposition. A photoresist is then deposited and patterned to define a window for etching a contact opening in the deposited top oxide 46. Thereafter, the photoresist is stripped, and highly doped polysilicon is deposited and patterned to form the polyconductor 22 and buried contact 48 which is shown.

Figures 8 and 9 illustrate stages in an alternative process for completing a buried interconnect 10. Figure 9 illustrates a completed structure resulting from an alternative process in which a buried contact 50 is made to the buried interconnect 10 from a second conductor 52 in contact with polyconductor 22. The structure shown in Figure 9 also varies from that of Figure 1 in that buried interconnect 10 has a sidewall 18 contacting the body of an electronic device 20A formed in SOI layer 12, since the SOI layer 12 where contacted underlies a gate dielectric 26 and polyconductor 22 is used there as a gate conductor. Note that contact to the body of an electronic device 20A by buried interconnect 10 is merely one possible embodiment, and is by no means required in this alternative process which focuses on use of a second conductor 52 in contact with the polyconductor 22. Second conductor 52 may be formed of any suitable material such as highly doped polysilicon, a metal silicide or a metal itself.

In such alternative process, processing proceeds the same way as that described above with reference to Figures 2 through 7 and through formation of the gate dielectric. Then, a polyconductor layer 22 is deposited, as shown in Figure 8. This differs from that described above relative to Figure 1 in that the polyconductor layer 22 is deposited over the gate dielectric 26 before etching the opening through oxide layer 46 to form the buried contact 48. Such process

sequence may be desirable to avoid possible interaction between the gate dielectric 26 and a photoresist used to pattern the contact opening.

Referring to Figure 9 once more, a photoresist is then applied and patterned to define a location in the polyconductor layer 22 which is etched to form the contact opening. A second conductor layer 52 is then deposited over polyconductor layer 22, including into the contact opening, to form the buried contact 50. A photoresist may then be applied and patterned, and the second conductor layer 52 and polyconductor layer 22 etched together in one combined etch, as by a directional reactive ion etch, to define the second conductor 52 and polyconductor 22.

Figure 10 illustrates a completed buried interconnect structure 10 formed according to another embodiment of the invention, in this case being formed in a bulk semiconductor substrate, as opposed to an SOI substrate. Processing proceeds in the same manner as that described above with reference to the embodiments of Figures 1-7 or Figures 2-9, except, as will now be described. With reference to Figure 4, since there is no buried oxide layer in the bulk substrate embodiment, oxide 38 may need to be deposited to a higher level of opening 35, such that the buried interconnect 10 contacts a device layer 20B, such as a source/drain diffusion, of an electronic device, rather than the bulk substrate 17, in order to avoid undesirable leakage currents from source/drain diffusion region 20B to bulk substrate 17.

While the invention has been described with reference to certain preferred embodiments thereof, those skilled in the art will understand the many modifications and enhancements which can be made without departing from the true scope and spirit of the invention, which is limited only by the claims appended below.

Industrial Applicability

The invention has applicability to integrated electronic circuits and their fabrication.

Claims

What is claimed is:

1. An integrated circuit including a buried interconnect formed in a single crystal semiconductor layer of a substrate, said buried interconnect formed of a deposited conductor and having one or more vertical sidewalls which contact a single crystal region of an electronic device formed in said single crystal semiconductor layer.

2. The integrated circuit of claim 1 wherein a plurality of electronic devices are contacted at single crystal regions thereof by said buried interconnect through said one or more vertical sidewalls.

3. The integrated circuit of claim 1 wherein said buried interconnect has at least one sidewall which contacts an isolation region on a side other than said vertical sidewall which contacts said single crystal region.

4. The integrated circuit of claim 1 wherein said single crystal region contacted by said buried interconnect comprises at least one diffusion region of at least one said electronic device.

5. The integrated circuit of claim 4 wherein a source/drain region of said electronic device is formed in said diffusion region.

6. The integrated circuit of claim 1 wherein said single crystal region contacted by said buried interconnect comprises a body of at least one said electronic device.

7. The integrated circuit of claim 1 wherein at least one conductive line formed above said substrate is conductively coupled to said buried interconnect.

8 The integrated circuit according to claim 7 wherein said at least one conductive line is conductively coupled to said buried interconnect.

9. The integrated circuit according to claim 8 wherein said conductive line contacts a top surface of said buried interconnect.

10. The integrated circuit according to claim 1 wherein said buried interconnect has a sidewall abutting a trench isolation .

11. The integrated circuit according to claim 1 wherein said deposited conductor includes doped polysilicon.

12. The integrated circuit according to claim 1 wherein said deposited conductor includes a metal.

13. The integrated circuit according to claim 1 wherein said deposited conductor includes a metal silicide.

14. The integrated circuit according to any of claims 11, 12, or 13, further comprising a liner formed in said trench before said deposited conductor.

15. The integrated circuit according to claim 1 wherein said single crystal region is isolated from said substrate by a buried oxide layer.

16. A method of forming a buried interconnect of an integrated circuit according to any of claims 1 through 15, comprising:

forming a trench isolation region in a substrate;

forming a trench in a single crystal region of said substrate abutting said isolation region, said trench having a bottom isolated from said single crystal region and a sidewall abutting said trench isolation region;

depositing a conductor in said trench, said conductor contacting said single crystal region on at least one sidewall of said trench; and

forming a contact to said deposited conductor from above.

17. The method of claim 16 wherein said contact to said deposited conductor is made through an opening etched into an isolation layer deposited onto said deposited conductor.

18. The method of claim 16 further comprising depositing a first conductive line over said substrate, wherein said contact to said deposited conductor conductively couples said conductive line to said deposited conductor.

19. The method of claim 18 further comprising depositing a second conductive line in contact with said first conductive line, wherein said contact to said deposited conductor conductively couples said first conductive line and said second conductive line to said deposited conductor.

20. The method of claim 16 wherein said bottom of said trench is isolated by a deposited oxide.

21. The method of claim 16 further comprising depositing a liner in said trench prior to depositing said conductor.