

ABSTRACT OF THE DISCLOSURETRACEBACK-PERFORMANCE APPARATUS IN VITERBI DECODER

The traceback-performing apparatus includes; 3 storage portions for receiving and storing new and minimum path metric values, where the first portion's first input is the last output value and vice-versa, the second portion's first input is also the first output, the third portion which reverses the first input to the last output and vice-versa, so as to find the decoded bits, and a first and second trace portions for receiving the corresponding outputs from the storing portions, with the first portion also receiving the minimum path metric value and the second portion receiving the first state. Both portions then generate a second state, which is the next state to be traced. Therefore, reducing cost in embodying the Viterbi decoder in a VLSI by reducing chip area and simplifying the embodiment, since an address-generating memory is simple and a global interconnection does not exist.

Fig. 7

(147 words)



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