

SEMICONDUCTOR MEMORY HAVING AN OVERLAID BUS STRUCTURE
ABSTRACT OF THE DISCLOSURE

A plurality of sense amplifiers are provided between a plurality of memory cell arrays having a plurality of memory cells. These sense amplifiers are
5 connected to bit lines of the respective memory cell arrays by array selection switches. Each of the sense amplifiers is connected to data lines by column switches. An array control portion is provided at each of the memory cell arrays. This array control portion
10 selectively controls the array selection switches and column switches to transmit the data in an arbitrary memory cell in a memory cell array to the data lines through the sense amplifier.

FIG. 1