RADIO-FREQUENCY SWITCH HAVING REDISTRIBUTION LAYER INDUCTANCE

CROSS-REFERENCE TO RELATED APPLICATION(S)

[0001] This application claims priority to U.S. Provisional Application No. 63/216,394 filed June 29, 2021, entitled RADIO-FREQUENCY SWITCH HAVING REDISTRIBUTION LAYER INDUCTANCE, the disclosure of which is hereby expressly incorporated by reference herein in its respective entirety.

BACKGROUND

Field

[0002] The present disclosure relates to devices and methods related to radio-frequency switches.

Description of the Related Art

[0003] In radio-frequency (RF) applications, switches are utilized to provide various functionalities such as routing of signals. Many of such switches are implemented as switching transistors.

SUMMARY

[0004] In accordance with one aspect, the present disclosure relates to a semiconductor chip that includes a semiconductor substrate having a switching circuit with a first node, and a plurality of layers configured to support the semiconductor substrate and to provide electrical connections for the switching circuit between a second node connectable to a location external to the semiconductor chip and the first node. The plurality of layers includes a redistribution layer. The semiconductor chip further includes a signal path implemented as a part of the redistribution layer, wherein the signal path includes a copper trace. The signal path has a first end electrically connected to the first node and a second end electrically connected to the second node, and is configured to provide a selected inductance.

[0005] In some examples, the signal path can be configured so that the selected inductance compensates for some or all of parasitic capacitance associated with the switching circuit. In some examples, the semiconductor chip can be

implemented as a flip chip device. In some examples, the semiconductor substrate can include a silicon-on-insulator substrate. The switching circuit can include a plurality of switching transistors, such that at least some of the parasitic capacitance results from one or more switching transistors in an OFF state.

[0006] In some examples, the selected inductance compensating for the parasitic capacitance can result in a reduced insertion loss associated with the switching circuit.

[0007] In some examples, the redistribution layer can be positioned away from the semiconductor substrate among the plurality of layers. For example, the redistribution layer can be a layer furthest away from the semiconductor substrate among the plurality of layers.

[0008] In some examples, the signal path can include a copper trace. The copper trace can have thickness and width values and extend in partial or full winding(s) to provide the selected inductance and a desired Q value. For example, the selected inductance can be in a range of 0.1 nH to 10 nH, and the desired Q value can be greater than 20. As a more specific example, the selected inductance can be in a range of 0.8 nH to 1.2 nH, and the desire Q value can be at least 25 at a frequency in a range of 2 GHz to 3 GHz.

[0009] In some examples, the copper trace can extend in approximately one winding.

[0010] In some examples, the second node can be configured to receive an amplified signal from a power amplifier. In some examples, the first node can be configured as a pole connectable to one or more of a plurality of throws of the switching circuit.

[0011] In another aspect, the present disclosure relates to a method for manufacturing a semiconductor chip device. The method includes forming a plurality of layers including a redistribution layer. The forming of the redistribution layer includes implementing a signal path as part of the redistribution layer such that the signal path provides a selected inductance with a first end electrically connected to a first node and a second end electrically connected to a second node, wherein the signal path includes a copper trace. The method further includes coupling a semiconductor substrate with a switching circuit to the plurality of layers, such that the first node is electrically connected to the switching circuit and the second node is connectable to a location external to the semiconductor chip device.

[0012] In yet another aspect, the present disclosure relates to a packaged module that includes a packaging substrate and a semiconductor chip mounted on the packaging substrate. The semiconductor chip includes a semiconductor substrate having a switching circuit with a first node, and a plurality of layers configured to support the semiconductor substrate and to provide electrical connections for the switching circuit between a second node connectable to a location external to the semiconductor chip and the first node. The plurality of layers includes a redistribution layer. The semiconductor chip further includes a signal path implemented as a part of the redistribution layer, wherein the signal path includes a copper trace. The signal path has a first end electrically connected to the first node and a second end electrically connected to the second node, and is configured to provide a selected inductance.

[0013] In some examples, the signal path can be configured so that the selected inductance compensates for some or all of parasitic capacitance associated with the switching circuit. In some examples, the semiconductor chip can be implemented as a flip chip device. In some examples, the semiconductor substrate can include a silicon-on-insulator substrate.

[0014] In some examples, the selected inductance compensating for the parasitic capacitance can result in a reduced insertion loss associated with the switching circuit.

[0015] In some examples, the redistribution layer can be positioned away from the semiconductor substrate among the plurality of layers. For example, the redistribution layer can be a layer furthest away from the semiconductor substrate among the plurality of layers.

[0016] In some examples, the packaged module can be implemented as a front-end module or an antenna switching circuit. The second node can be configured to receive an amplified signal from a power amplifier, and the first node can be configured as a pole connectable to one or more of a plurality of throws of the switching circuit.

[0017] In yet another aspect, the present disclosure relates to a wireless device that includes a transceiver, an antenna, and a switching device implemented to be electrically between the transceiver and the antenna. The switching device includes a semiconductor chip that includes a semiconductor substrate having a switching circuit with a first node, and a plurality of layers configured to support the semiconductor substrate and to provide electrical connections for the switching

circuit between a second node connectable to a location external to the semiconductor chip and the first node. The plurality of layers includes a redistribution layer. The semiconductor chip further includes a signal path implemented as a part of the redistribution layer, wherein the signal path includes a copper trace. The signal path has a first end electrically connected to the first node and a second end electrically connected to the second node, and is configured to provide a selected inductance.

[0018] In some examples, the signal path can be configured so that the selected inductance compensates for some or all of parasitic capacitance associated with the switching circuit. In some examples, the semiconductor chip can be implemented as a flip chip device. In some examples, the wireless device can further include a power amplifier implemented to be electrically between the transceiver and the switching device, such that the second node is configured to receive an amplified signal from the power amplifier.

[0019] For purposes of summarizing the disclosure, certain examples, advantages and novel features of the disclosures have been described herein. It is to be understood that not necessarily all such advantages may be achieved in accordance with any particular example of the disclosure. Thus, the disclosure may be embodied or carried out in a manner that achieves or optimizes one advantage or group of advantages as taught herein without necessarily achieving other advantages as may be taught or suggested herein.

BRIEF DESCRIPTION OF THE DRAWINGS

[0020] Figure 1 depicts a packaged radio-frequency (RF) chip device that includes a switching circuit indicated as switches.

[0021] Figure 2 shows that in some embodiments, the RF chip device of Figure 1 can be implemented as a flip chip device.

[0022] Figure 3 shows an example of a conventional flip chip device.

[0023] Figure 4 shows that in some embodiments, a flip chip device can include a switching circuit configured to support transmit and/or receive operations involving one or more frequency bands.

[0024] Figure 5A shows an example layout of a redistribution layer (RDL) inductance that can be implemented for the RDL inductance of Figure 4.

[0025] Figure 5B shows an isolated view of the RDL inductance of Figure 5A.

WHAT IS CLAIMED IS:

1. A semiconductor chip comprising:

a semiconductor substrate having a switching circuit with a first node;

a plurality of layers configured to support the semiconductor substrate and to provide electrical connections for the switching circuit between a second node connectable to a location external to the semiconductor chip and the first node, the plurality of layers including a redistribution layer; and

a signal path implemented as a part of the redistribution layer, the signal path having a first end electrically connected to the first node and a second end electrically connected to the second node, the signal path configured to provide a selected inductance, wherein the signal path includes a copper trace.

2. The semiconductor chip of claim 1 wherein the signal path is configured so that the selected inductance compensates for some or all of parasitic capacitance associated with the switching circuit.

3. The semiconductor chip of claim 2 wherein the semiconductor chip is implemented as a flip chip device.

4. The semiconductor chip of claim 2 wherein the semiconductor substrate includes a silicon-on-insulator substrate.

5. The semiconductor chip of claim 4 wherein the switching circuit includes a plurality of switching transistors, such that at least some of the parasitic capacitance results from one or more switching transistors in an OFF state.

6. The semiconductor chip of claim 2 wherein the selected inductance compensating for the at least some of the parasitic capacitance results in a reduced insertion loss associated with the switching circuit.

7. The semiconductor chip of claim 2 wherein the redistribution layer is positioned away from the semiconductor substrate among the plurality of layers.

8. The semiconductor chip of claim 7 wherein the redistribution layer is a layer furthest away from the semiconductor substrate among the plurality of layers.

9. The semiconductor chip of claim 2 wherein the copper trace has thickness and width values and extends in partial or full winding(s) to provide the selected inductance and a desired Q value.

10. The semiconductor chip of claim 9 wherein the selected inductance is in a range of 0.1 nH to 10 nH, and the desired Q value is greater than 20.

11. The semiconductor chip of claim 10 wherein the selected inductance in a range of 0.8 nH to 1.2 nH, and the desire Q value is at least 25 at a frequency in a range of 2 GHz to 3 GHz.

12. The semiconductor chip of claim 10 wherein the copper trace extends in approximately one winding.

13. The semiconductor chip of claim 2 wherein the second node is configured to receive an amplified signal from a power amplifier.

14. The semiconductor chip of claim 2 wherein the first node is configured as a pole connectable to one or more of a plurality of throws of the switching circuit.

15. A method for manufacturing a semiconductor chip device, the method comprising:

forming a plurality of layers including a redistribution layer, the forming of the redistribution layer including implementing a signal path as part of the redistribution layer such that the signal path provides a selected inductance with a first end electrically connected to a first node and a second end electrically connected to a second node, wherein the signal path includes a copper trace; and

coupling a semiconductor substrate with a switching circuit to the plurality of layers, such that the first node is electrically connected to the switching

circuit and the second node is connectable to a location external to the semiconductor chip device.

16. A packaged module comprising:

a packaging substrate; and

a semiconductor chip mounted on the packaging substrate, the semiconductor chip including a semiconductor substrate having a switching circuit with a first node, and a plurality of layers configured to support the semiconductor substrate and to provide electrical connections for the switching circuit between a second node connectable to a location external to the semiconductor chip and the first node, the plurality of layers including a redistribution layer, the semiconductor chip further including a signal path implemented as a part of the redistribution layer, the signal path having a first end electrically connected to the first node and a second end electrically connected to the second node, the signal path configured to provide a selected inductance, wherein the signal path includes a copper trace.

17. The packaged module of claim 16 wherein the signal path is configured so that the selected inductance compensates for some or all of parasitic capacitance associated with the switching circuit.

18. The packaged module of claim 17 wherein the semiconductor chip is implemented as a flip chip device.

19. The packaged module of claim 17 wherein the semiconductor substrate includes a silicon-on-insulator substrate.

20. The packaged module of claim 17 wherein the selected inductance compensating for the at least some of the parasitic capacitance results in a reduced insertion loss associated with the switching circuit.

21. The packaged module of claim 17 wherein the redistribution layer is positioned away from the semiconductor substrate among the plurality of layers.

22. The packaged module of claim 21 wherein the redistribution layer is a layer furthest away from the semiconductor substrate among the plurality of layers.

23. The packaged module of claim 17 wherein the packaged module is implemented as a front-end module or an antenna switching circuit.

24. The packaged module of claim 23 wherein the second node is configured to receive an amplified signal from a power amplifier.

25. The packaged module of claim 24 wherein the first node is configured as a pole connectable to one or more of a plurality of throws of the switching circuit.

26. A wireless device comprising:

a transceiver;

an antenna; and

a switching device implemented to be electrically between the transceiver and the antenna, the switching device including a semiconductor chip that includes a semiconductor substrate having a switching circuit with a first node, and a plurality of layers configured to support the semiconductor substrate and to provide electrical connections for the switching circuit between a second node connectable to a location external to the semiconductor chip and the first node, the plurality of layers including a redistribution layer, the semiconductor chip further including a signal path implemented as a part of the redistribution layer, the signal path having a first end electrically connected to the first node and a second end electrically connected to the second node, the signal path configured to provide a selected inductance, wherein the signal path includes a copper trace.

27. The wireless device of claim 26 wherein the signal path is configured so that the selected inductance compensates for some or all of parasitic capacitance associated with the switching circuit.

28. The wireless device of claim 27 wherein the semiconductor chip is implemented as a flip chip device.

29. The wireless device of claim 26 further comprising a power amplifier implemented to be electrically between the transceiver and the switching device, such that the second node is configured to receive an amplified signal from the power amplifier.