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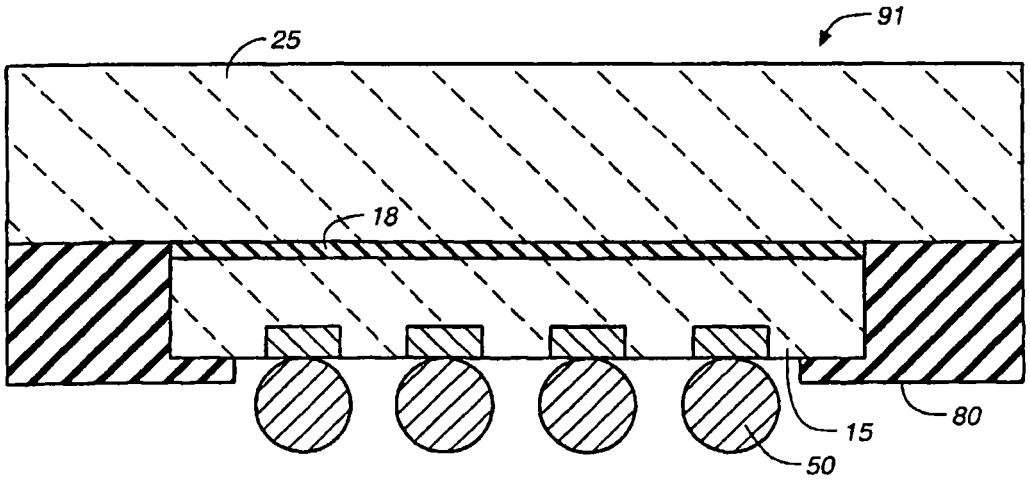
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ACTION

(54) Title: METHOD OF FORMING A STACKED-DIE INTEGRATED CIRCUIT CHIP PACKAGE ON A WAFER LEVEL



(57) Abstract: A wafer level packaging method which produces a stacked dual/multiple die integrated circuit package (91). In the method, the wafer with the smaller sized dice (15) of two wafers is processed through a metal redistribution process and then solder balls are attached. The wafer is then sawed into individual die size ball-grid array packages. On the wafer with the larger sized dice (25), a die attached adhesive material (18) is deposited on the front of each die site location that is intended for the attachment of one of the die-sized BGA packages. The back side of the BGA die package is placed onto the adhesive material and is cured. A wirebonding operation connects the signals from the die-size BGA package to the circuits of the bottom die. A coating material (80), such as epoxy, is disposed on the wafer to cover the wirebond leads and the assembly is then cured. Then, the stacked-die wafer is singulated into individual stacked-die IC packages (91).

WO 01/67511 A3