

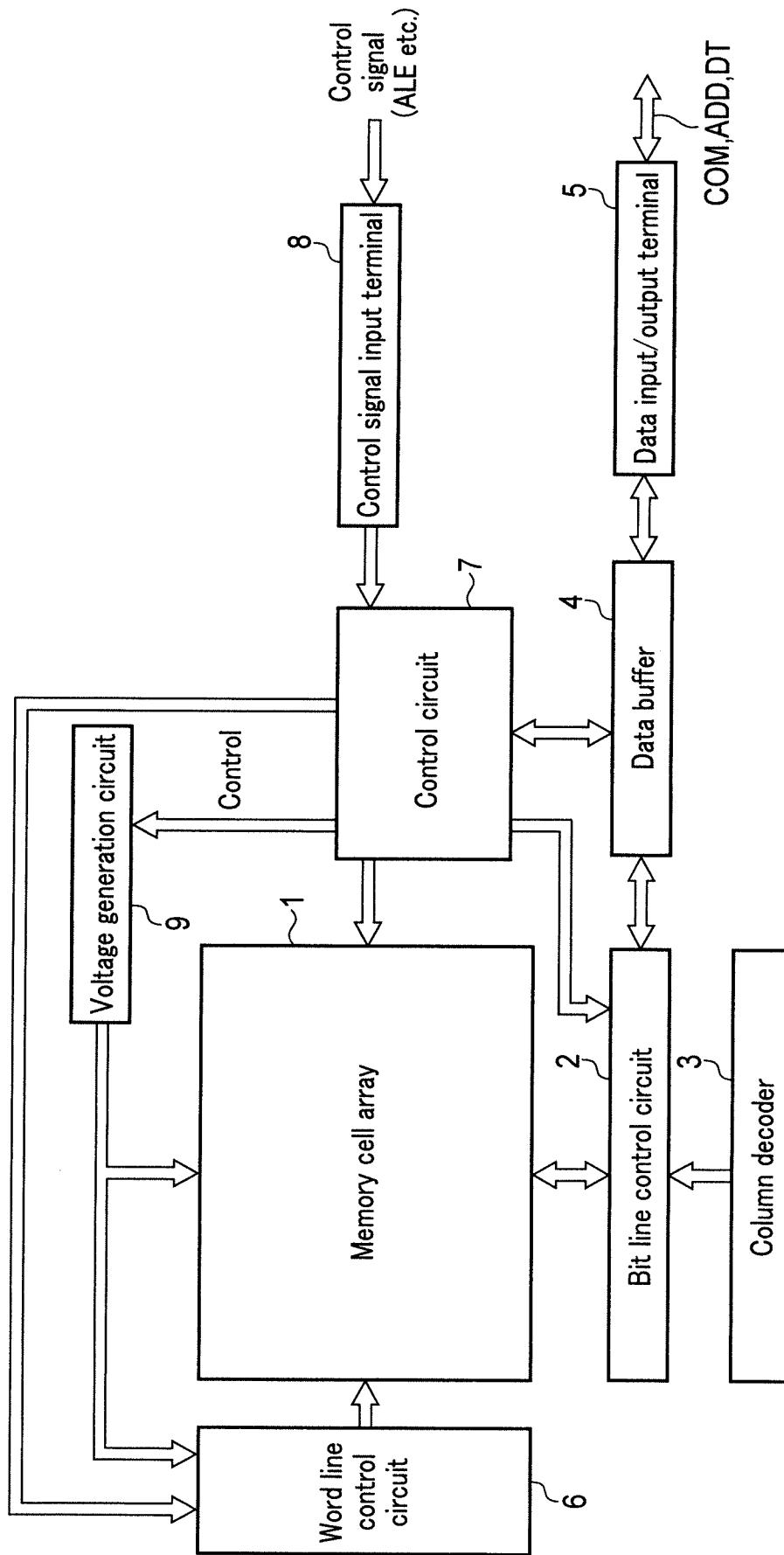


FIG. 1

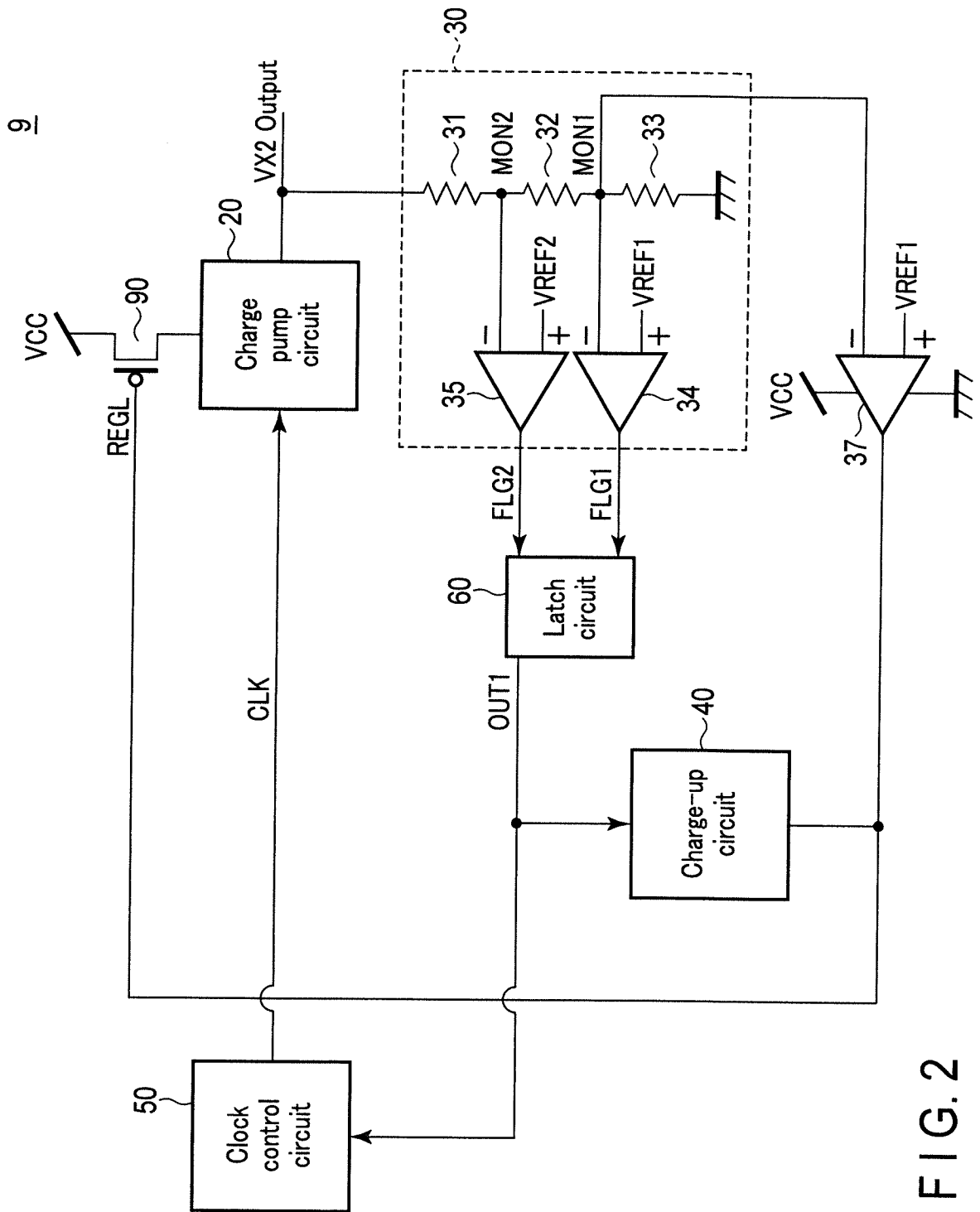


FIG. 2

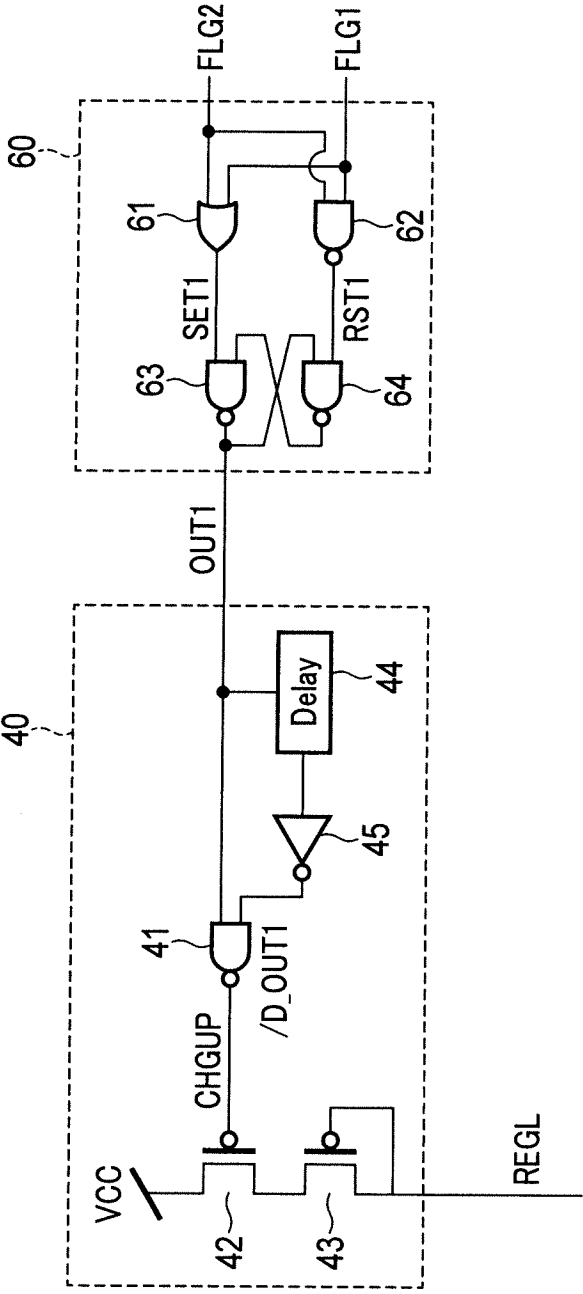


FIG. 3

FLG1	FLG2	SET1	RST1	OUT1
0	0	0	1	1
0	1	1	1	Keep state
1	0	1	1	Keep state
1	1	1	0	0

FIG. 4

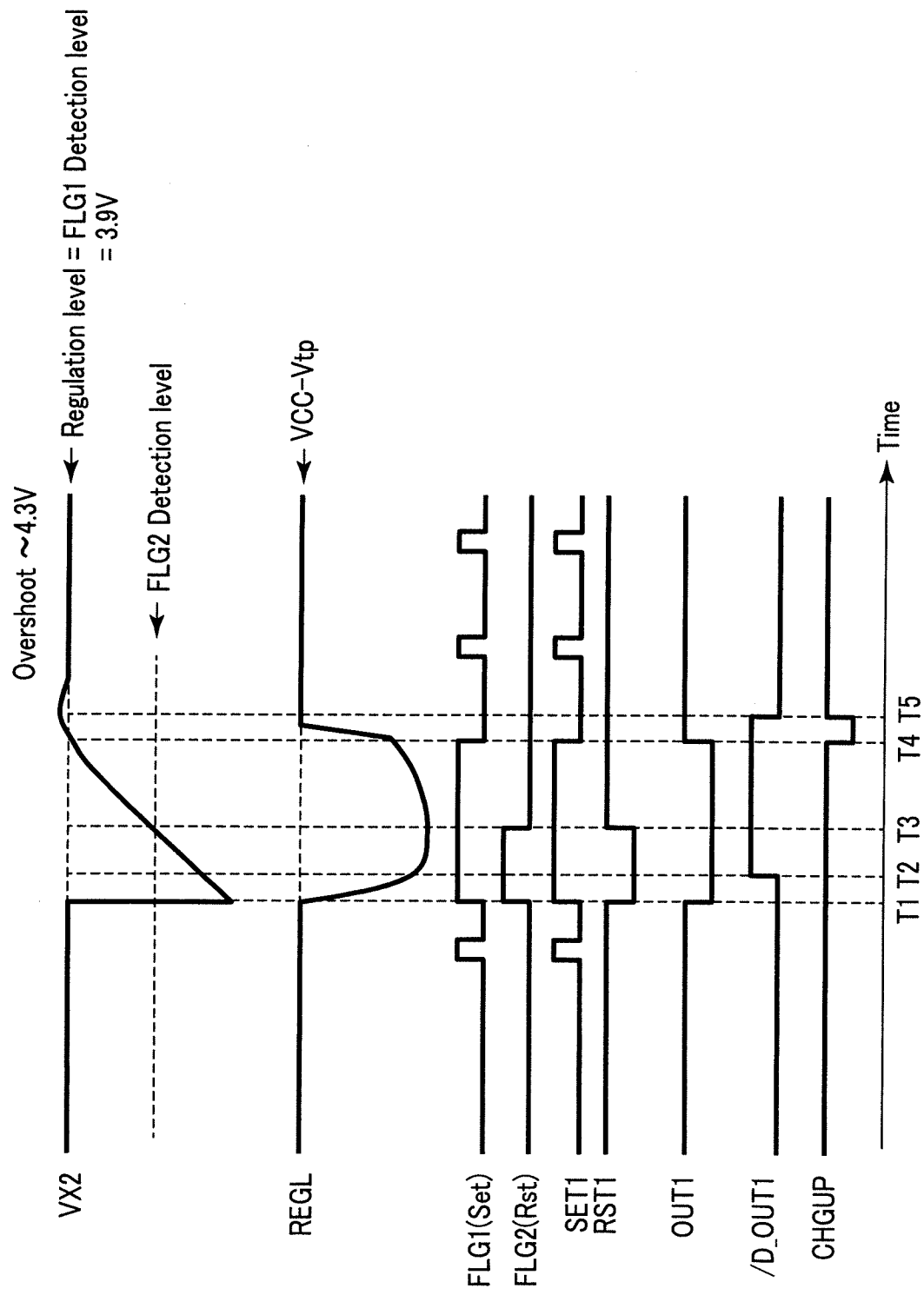


FIG. 5

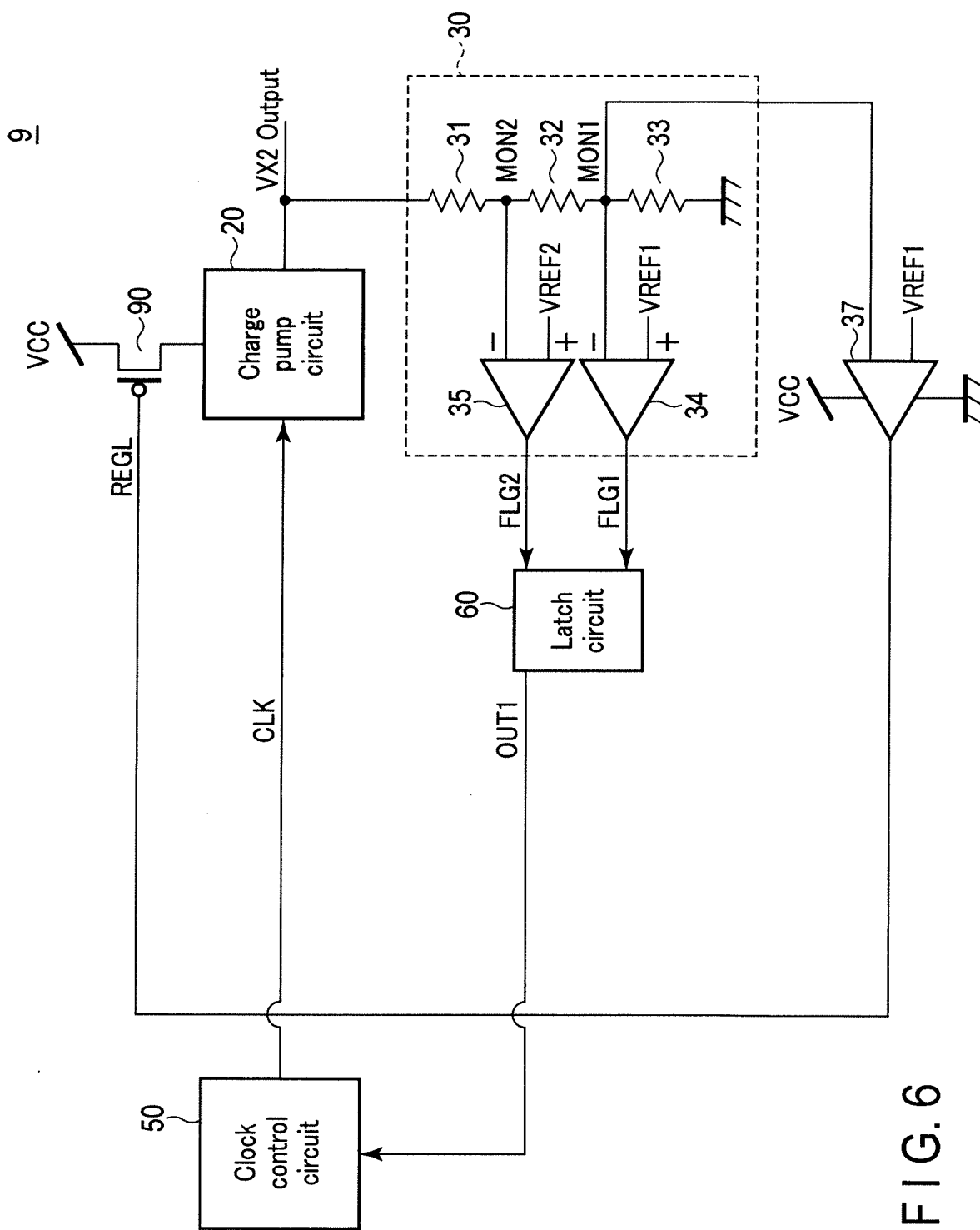


FIG. 6

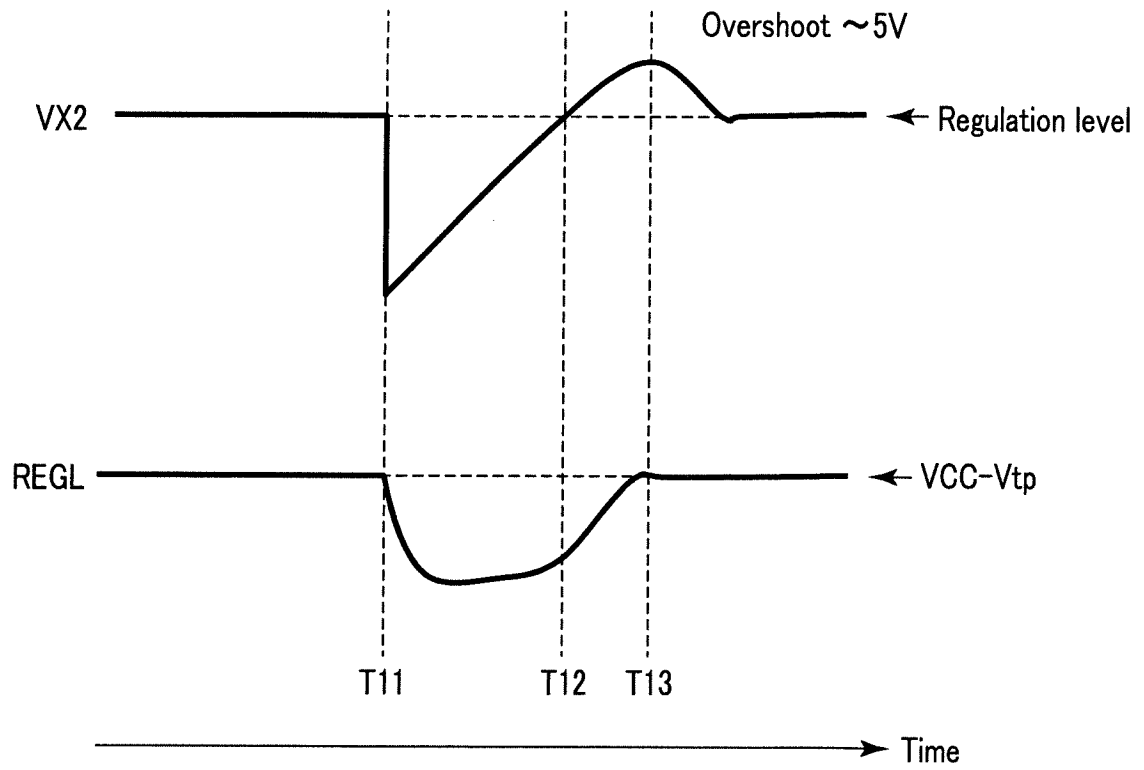
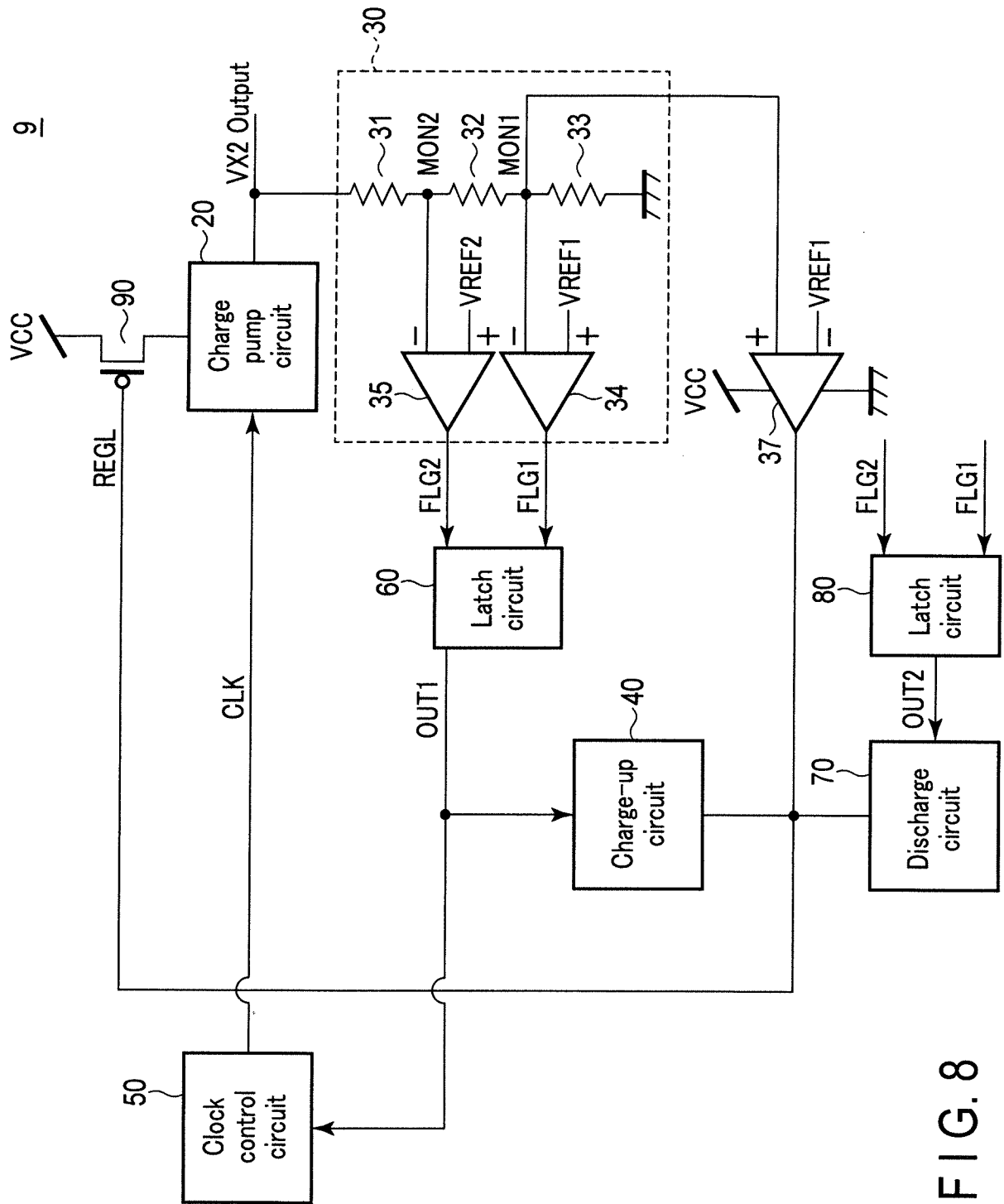


FIG. 7



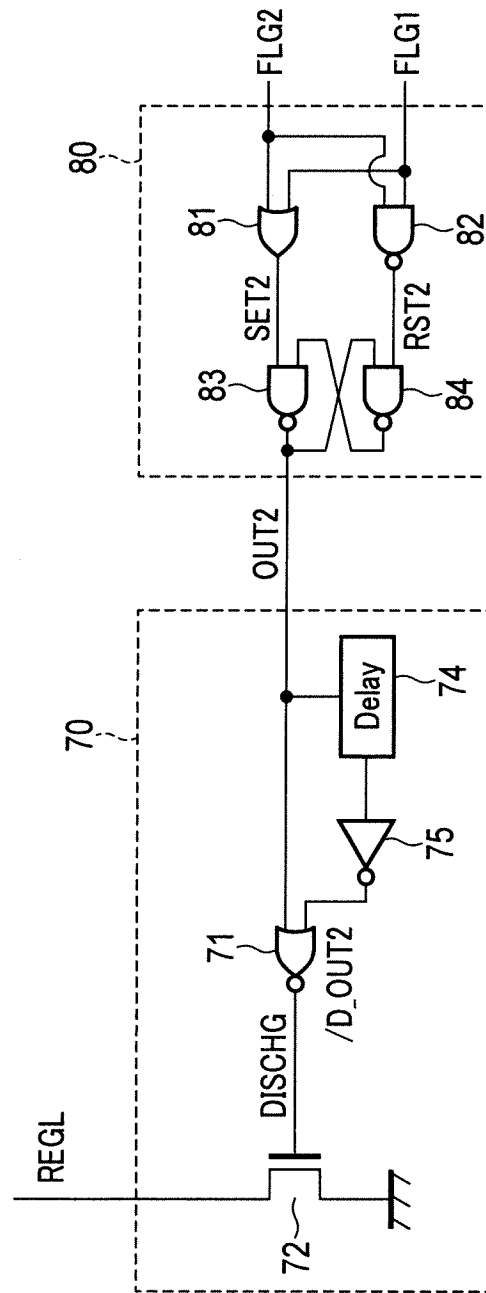


FIG. 9

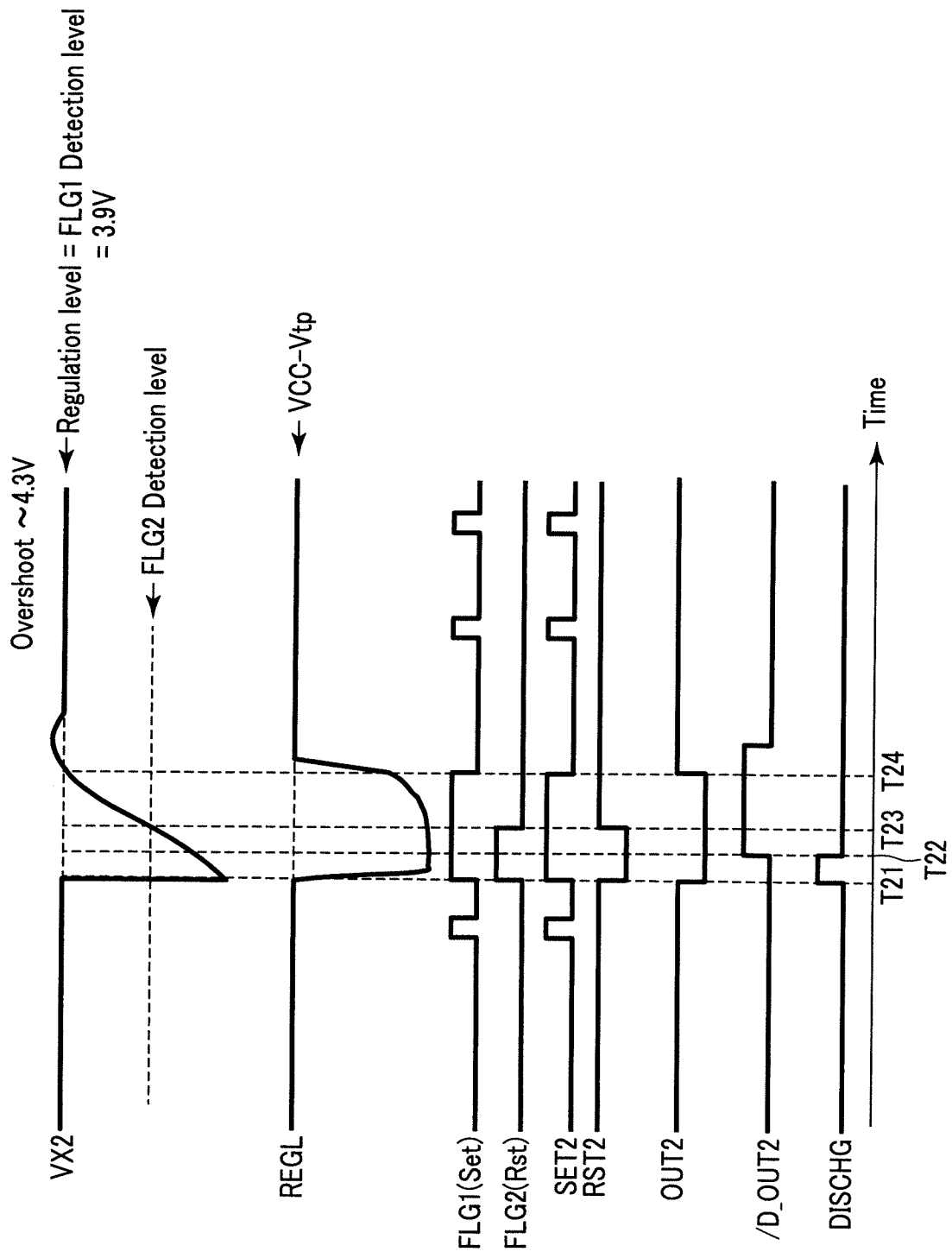


FIG. 10