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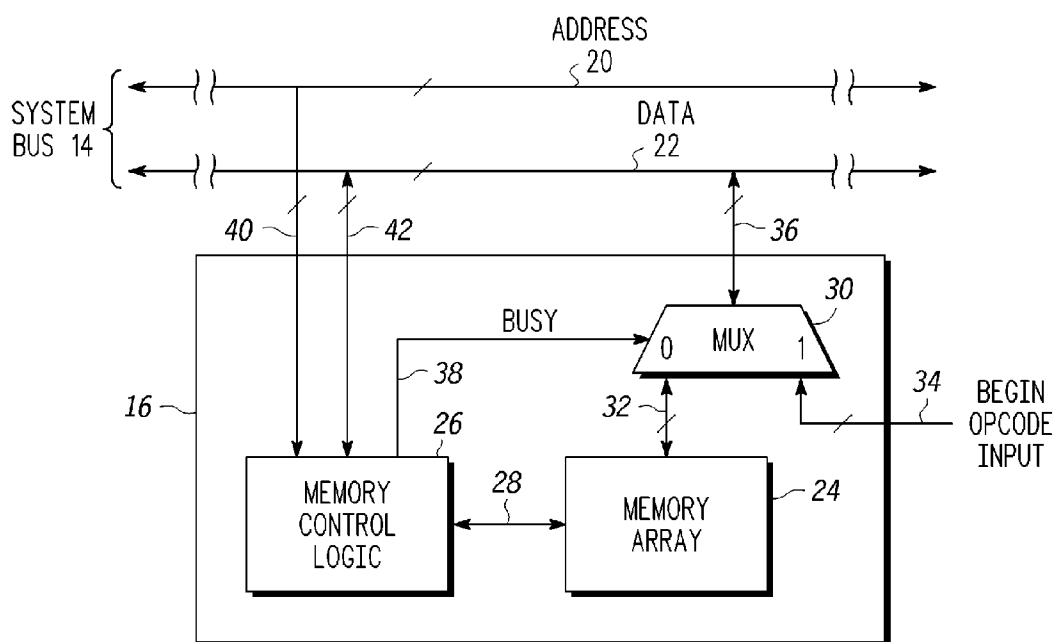
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(57) Abstract: An integrated circuit (10) comprises a processor (12) configured for fetching and executing opcodes, a system bus (14), and a memory (16) coupled to the processor via the system bus. The memory includes logic circuitry (26) for detecting functional states of the memory, wherein the memory (a) supplies one or more programmed opcodes in response to detection of first functional states of the memory, and (b) supplies a hard coded opcode in response to detection of second functional states of the memory.

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