

SUBSTRATE FOR A TEMPERATURE-COMPENSATED SURFACE ACOUSTIC WAVE DEVICE OR BULK ACOUSTIC WAVE DEVICE

FIELD OF THE INVENTION

5 The present invention relates to a substrate for a temperature-compensated surface acoustic wave device or a bulk acoustic wave device as well as a method for manufacture of such a substrate and a surface acoustic wave device or bulk acoustic wave device comprising such a substrate.

10 BACKGROUND TO THE INVENTION

Surface Acoustic Wave devices, generally designated by the acronym SAW devices, find applications in the field of radio-frequency (RF) communications and in particular for filter applications.

A SAW device typically comprises a piezoelectric layer and two electrodes in the
15 form of two interdigitated metallic combs deposited on the surface of said piezoelectric layer.

An electrical signal, such as an electrical voltage change applied to an electrode, is converted into an elastic wave which is propagated at the surface of the piezoelectric layer. The wave is converted once more into an electric signal on reaching the other
20 electrode.

The choice of the piezoelectric material takes into account the electromagnetic coupling coefficient, which expresses the rate of electromagnetic conversion by said material, and the temperature stability of the oscillation frequency of the piezoelectric material.

25 SAW devices are very sensitive to variations in temperature, which induce different degrees of expansion of the piezoelectric layer and of the metallic electrodes due to the different coefficients of thermal expansion of these materials.

More precisely, the Temperature Coefficient of Frequency referred to by the acronym TCF and which is defined as the variation of a given frequency f as a function of
30 the temperature T , is given by the formula:

$$TCF = \frac{1}{f} \frac{\partial f}{\partial T} = TCV - CTE$$

where:

$$TCV = \frac{1}{V} \frac{\partial V}{\partial T}$$

V is the speed of the surface acoustic waves and

CTE is the coefficient of thermal expansion of the piezoelectric material in the direction of propagation of the surface acoustic waves.

Measures already exist for compensating for the effects of temperature on SAW devices.

In particular, the article by Hashimoto et al [1] provides a review of the various temperature compensation techniques for SAW devices.

5 Amongst these different techniques the following can essentially be distinguished:

(1) a so-called "overlay" technique consisting of covering the surface of the piezoelectric layer and the electrodes with a dielectric material (typically silicon oxide (SiO_2)), which exhibits a coefficient of thermal expansion in the opposite sense to that of the piezoelectric layer,

10 (2) a so-called "wafer-bonding" technique consisting of bonding the piezoelectric layer to a support substance whose coefficient of thermal expansion is as low as possible so as to neutralise the thermal expansion of the piezoelectric layer. Said support substrate, which may be made, for example, of silicon, of sapphire, of glass or of spinel (MgAl_2O_4) thus performs a stiffening function of the piezoelectric layer. Given its
15 thickness, the piezoelectric layer is considered to extend to infinity in a direction away from the electrodes, so that the presence of the support substrate does not interfere with the propagation of the surface acoustic waves. Nevertheless, the bonding of the support substrate appears to create spurious resonances at frequencies greater than the principal frequency of the device (see [1], Fig. 5).

20 Of the materials envisaged for the support substrate in this second technique, silicon seems to be the most promising as it allows integration methods for electronic components at the substrate scale (so-called "wafer level") to be implemented.

Nevertheless, a significant difference in thermal expansion coefficients exists between the piezoelectric material and silicon (for a crystal of LiTaO_3 , which is anisotropic,
25 the CTE values are about $4 \times 10^{-6}/^\circ\text{C}$ and $14 \times 10^{-6}/^\circ\text{C}$ whilst the CTE of silicon is of the order of $2.3 \times 10^{-6}/^\circ\text{C}$), which affects the stability of the support substrate / piezoelectric layer stack if the latter is exposed to high temperatures during the subsequent steps in the method for manufacture of the surface acoustic wave device. In the light of such steps, thermal stability of the piezoelectric layer / support substrate stack must be ensured up to
30 a temperature of about 250°C .

A similar problem arises for bulk (volume) acoustic wave filters and resonators, known by the acronym BAW.

Bulk acoustic wave filters and resonators typically comprise a thin piezoelectric layer (that is, with a thickness in general of less than $1 \mu\text{m}$) and two electrodes arranged on
35 each principal face of said thin layer. An electrical signal, such as an electrical voltage change applied to an electrode, is converted into an elastic wave which is propagated through the piezoelectric layer. This wave is converted once more into an electric signal on reaching the electrode located on the opposite face.

BRIEF DESCRIPTION OF THE INVENTION

Embodiments of the present invention seek to provide a substrate for a temperature compensation surface wave acoustic device or bulk acoustic wave device which can overcome the above mentioned drawbacks. In particular, such a substrate can be more stable than the above-mentioned silicon support substrate / piezoelectric layer stack up to a temperature of about 300°C, whilst allowing easy integration of electronic components.

In accordance with an aspect of the present invention, a substrate is proposed for a surface acoustic wave device or bulk acoustic wave device which comprises a support substrate and an piezoelectric layer on said support substrate, characterised in that the support substrate comprises a semiconductor layer on a stiffening substrate which has a coefficient of thermal expansion closer to the coefficient of thermal expansion of the material of the piezoelectric layer than that of silicon, where the semiconductor layer is arranged between the piezoelectric layer and the stiffening substrate.

The stiffening substrate advantageously comprises sapphire, glass and/or spinel (MgAl_2O_4).

The semiconductor layer is preferably formed from one of the following materials: silicon, germanium, SiGe, SiC, a III-V material.

Particularly advantageously, the semiconductor layer comprises at least one electronic component. Said electronic component may in particular be chosen from amongst: a CMOS transistor, a switch and a power amplifier.

According to one embodiment, the ratio of the thickness of the piezoelectric layer to the thickness of the stiffening substrate is less than or equal to 0.125.

For example, the thickness of the piezoelectric layer is less than 50 μm , preferably less than 20 μm , yet more preferably less than 1 μm and the thickness of the stiffener substrate is between 400 and 800 μm .

The substrate comprises a dielectric layer between the piezoelectric layer and the semiconductor layer and a charge trapping layer at the interface between said dielectric layer and the semiconductor layer and/or the interface between the dielectric layer and the piezoelectric layer.

Said charge trapping layer may comprise a polycrystalline silicon layer.

In the case of the piezoelectric layer being anisotropic and therefore exhibiting at least two different coefficients of thermal expansion in a plane parallel to a principal face of the substrate, the coefficient of thermal expansion which results in the greatest discrepancy in relation to the coefficient of thermal expansion of the stiffening substrate is considered.

The invention also relates to a surface acoustic wave device comprising a substrate as described above and two electrodes formed of two interdigitated metallic combs on the surface of the piezoelectric layer.

5 The invention also relates to a bulk acoustic wave device comprising a substrate as described above and two electrodes arranged on either side of the piezoelectric layer.

Another object relates to a method of manufacture of a substrate as described above, characterised in that it comprises:

- providing a first donor substrate comprising a semiconductor layer,
- providing a stiffening substrate which has a coefficient of thermal expansion closer
10 to the coefficient of thermal expansion of the material of the piezoelectric layer than that of silicon,
- transferring the semiconductor layer onto the stiffening substrate from a first donor substrate,
- providing a second donor substrate comprising the piezoelectric layer,
- 15 - transferring the piezoelectric layer onto the semiconductor layer from a second donor substrate
- forming a dielectric layer on one and/or the other of the piezoelectric layer and the semiconductor layer; and
- forming a charge trapping layer at the interface between said dielectric layer and
20 the semiconductor layer and/or the interface between the dielectric layer and the piezoelectric layer.

According to one embodiment at least one of the transfer steps comprises the following sub-steps:

- formation of an embrittlement zone in the first, second donor substrates
25 respectively by the implantation of atomic species;
- bonding of the first, second donor substrates respectively onto the stiffening substrate and semiconductor layer respectively;
- detachment of said first, second substrates respectively along the embrittlement zone.

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BRIEF DESCRIPTION OF DRAWINGS

Other characteristics and advantages of the invention will emerge from the detailed description which follows, with reference to the appended drawings, in which:

- figure 1 is a schematic section view of a temperature compensated surface
35 acoustic wave filter,
- figure 2 is a schematic section view of a temperature compensated bulk acoustic wave resonator,

- figure 3 is schematic section of a substrate according to one embodiment form of the invention,

- figure 4 is a schematic section of a temperature compensated surface acoustic wave filter according to one embodiment of the invention,

5 - figure 5 is a schematic section of a temperature compensated surface acoustic wave filter according to an alternative embodiment of the invention,

- figures 6A to 6E show successive steps in the manufacture of a substrate according to one embodiment of the invention.

10 For readability purposes the elements shown are not necessarily shown to scale. In addition the same components are designated by the same reference symbols on the various figures.

DETAILED DESCRIPTION OF THE EMBODIMENTS OF THE INVENTION

Figure 1 is a schematic view of a surface acoustic wave filter.

Said filter comprises a piezoelectric layer 10 and two electrodes 12, 13 in the form of
5 two interdigitated metallic combs deposited on the surface of said piezoelectric layer. On
the side away from the electrode 12, 13, the piezoelectric layer rests on a support
substrate 11 intended to provide temperature compensation and whose structure will be
described in detail below. The piezoelectric layer 10 preferably has excellent crystalline
quality in order not to cause attenuation of the surface wave. Said layer is therefore
10 monocrystalline. Currently, suitable materials which can be used industrially are quartz,
 LiNbO_3 or LiTaO_3 . The piezoelectric layer 10 is generally obtained by sectioning an ingot
of one of said materials, where the required precision for the thickness of said layer is not
great insofar as the waves must essentially be propagated at its surface.

Figure 2 is a schematic view of a bulk acoustic wave resonator.

15 The resonator comprises a thin piezoelectric layer (that is, with a thickness in
general of less than 20 nm) and two electrodes 12, 13 arranged on either side of said
piezoelectric layer 10. The piezoelectric layer 10 rests on a support substrate 11 whose
structure will be described in detail below. To isolate the resonator from the substrate and
thus avoid propagation of waves into the substrate, a Bragg mirror 14 is interposed
20 between the electrode 13 and the substrate 11. Alternatively (not shown) isolation could
be achieved by arranging a cavity between the substrate and the piezoelectric layer.
These various arrangements are known to those skilled in the art and are therefore not
described in detail in the present description.

For a bulk acoustic wave device the piezoelectric layer 10 has a determined uniform
25 thickness over the entire layer. On the other hand, since crystalline quality does assume
on any particular importance in terms of resonator performance, a polycrystalline
piezoelectric material is acceptable. The piezoelectric layer 10 is therefore in general
formed by deposition onto a support (for example a silicon support). The materials
currently used industrially for such deposition are AlN, ZnO and PZT.

30 Figure 3 is a schematic section view of a substrate used to manufacture a
temperature compensated surface acoustic wave device or bulk acoustic wave device
according to one embodiment form of the invention.

Said substrate 1 comprises a piezoelectric layer 10 intended to receive electrodes in
order to form a surface acoustic wave device or bulk acoustic wave device.

35 The material, the crystalline quality and the thickness of said piezoelectric layer 10
are selected by those skilled in the art depending on the target application. Selection
criteria are themselves known and do not need to be described in detail in the present
description.

If the selected piezoelectric material is anisotropic, the latter has different coefficients of thermal expansion in different directions.

The piezoelectric layer 10 is arranged on a composite support substrate 11, that is, one formed from a stack of several layers of different materials.

5 Said support substrate 11 comprises a so-called stiffening substrate 110, whose function within the substrate 1 is to ensure the rigidity of the stack, in particular during heat treatment operations.

The stiffening substrate 110 advantageously comprises sapphire, glass and/or spinel (MgAl_2O_4).

10 These materials have the advantage of offering a coefficient of thermal expansion closer to the coefficient of thermal expansion of the piezoelectric material than silicon, providing improved temperature stability (up to about 300°C) of the stack, although this increased closeness of the coefficient of thermal expansion is slightly detrimental to the temperature compensation effect.

15 The stiffener substrate 110 moreover exhibits a large thickness, typically of the order of 400 to 800 μm , which is much greater than the thickness of the other layers of the substrate 1 and in particular much greater than the thickness of the piezoelectric layer, which is in general less than 50 μm , preferably less than 20 μm and yet more preferably less than 1 μm . Thus the temperature behaviour of the stiffening substrate predominates
20 compared with that of the other layers.

Due to the relative closeness of the coefficients of thermal expansion of the stiffening substrate 110 and of the piezoelectric layer 10, the stresses due to the difference in coefficients of thermal expansion during the heat treatment that the substrate 1 undergoes are minimised.

25 A semiconductor layer 111 is inserted between the stiffener substrate 110 and the piezoelectric layer 10. Said semiconductor layer may comprise silicon, germanium, SiGe, SiC, or a III-V type material such as GaAs, GaN or InGaN (this list is non-restrictive). Of these materials, germanium and GaAs are less preferable because of their fragility. According to one preferred embodiment form of the invention, the semiconductor layer is
30 a layer of silicon.

Particularly advantageously the semiconductor layer 111 comprises at least one electronic component 112. Said component is manufactured using techniques known in microelectronics. This may be a CMOS transistor, a switch, a power amplifier (this list is not restrictive). Moreover pathways 113 may be made on the interior of the semiconductor
35 layer 111 so as to allow electrical connection of various components. These components and pathways are formed by conventional microelectronic techniques which are not described in detail in the present description.

The semiconductor layer 111 is substantially thinner than the stiffening substrate 110. Thus the semiconductor layer 111 typically has a thickness of between 10 nm and 2 μm . Consequently, even if the material of the semiconductor layer has a difference in coefficient of thermal expansion relative to the piezoelectric material that is greater than
 5 the difference in coefficient of thermal expansion between the material of the stiffening substrate 110 and the piezoelectric material 10, the semiconductor layer 111 is thin enough not to generate mechanical stress in the piezoelectric layer 10 during heat treatment.

Moreover, in comparison with a bulk sapphire substrate, the composite substrate 11
 10 formed of the sapphire stiffening substrate 110 and of the semiconductor layer 111 allow electronic components to be integrated into the rear face of the piezoelectric layer 10.

According to one advantageous but not mandatory embodiment form, a dielectric layer 114 is arranged at the interface between the semiconductor layer 111 and the piezoelectric layer 10. Such a dielectric layer is in general used to promote the bonding of
 15 the piezoelectric layer 10 onto the semiconductor layer 111. The dielectric layer may be formed, prior to the bonding of the piezoelectric layer 10 on the semiconductor layer 111, either on only one of these layers, or on each of them (oxide-oxide type bonding being performed in the latter case). In this event, a charge trapping layer 115 is made beneath the piezoelectric layer, advantageously interposed between the dielectric layer 114 and
 20 the piezoelectric layer 10, or between the semiconductor layer 111 and the dielectric layer 114 in order to trap electric charge present which could interfere with the operation of electronic components arranged within the semiconductor layer 111. Said trapping layer 115 may comprise, for example, a layer of polycrystalline or amorphous silicon. Any other layer (or stack of layers) which fulfils the electric charge trapping function may be used
 25 however.

Figure 4 schematically shows a surface acoustic wave filter formed on the substrate 1 of figure 3. To this end, metallic electrodes 12, 13 have been deposited in the form of two interdigitated combs on the free surface of the piezoelectric layer 10.

According to one embodiment alternative shown in figure 5, the substrate may, after
 30 electrodes 12, 13 are formed on the piezoelectric layer 10, be covered with a layer of dielectric (typically silicon oxide (SiO_2)) in accordance with the "overlay" technique mentioned above. The thickness of the dielectric layer 15 is typically of the order of 100 to 10,000 nm.

Compared with the embodiment in figure 4, the dielectric layer 15 which has a
 35 coefficient of thermal expansion which is in the opposite sense to that of the piezoelectric layer 10, provides improved temperature compensation.

A method of manufacture of a substrate for a surface acoustic wave device or bulk acoustic wave device according to one non-restrictive embodiment of the invention will

now be described with reference to figures 6A to 6E. The method described below involves bonding then thinning of a donor substrate, but other techniques such as a "removable substrate" type as described in document FR 2 816 445 may be employed. Such a "removable" substrate is made before the manufacture of components and
5 contains an embrittlement zone or interface which allows the donor substrate to be broken after assembly on a stiffening substrate.

With reference to figure 6A, a donor substrate 116 is provided which comprises the semiconductor layer 111 wherein electronic components 112 and/or pathways 113 are advantageously incorporated, in accordance with techniques widely used in
10 microelectronics.

With reference to figure 6B, the donor substrate 116 is bonded onto the stiffening substrate 110, so that the semiconductor layer 111 is located at the bonding interface.

With reference to figure 6C, the donor substrate is made thinner though the side away from the semiconductor layer 111 so as to transfer the layer comprising the layer
15 111 onto the stiffening substrate 110. Said thinning may be mechanical (of the polishing type), chemical (etching) or other. If necessary the electronic components and/or pathways are then integrated in said layer.

With reference to figure 6D, a donor substrate 118 is provided made of a piezoelectric material and an embrittlement zone 119 is formed, by implantation of atomic
20 species in said substrate, which demarcates a piezoelectric layer to be transferred, namely the piezoelectric layer 10 of the final substrate shown in figure 3. The implantation conditions are known in the state of the art, namely a dose of the order of 5 to 15×10^{16} and energy of between 20 and 200 keV.

With reference to figure 6E, the donor substrate 118 is bonded onto the stack
25 formed from the stiffening substrate 110 and the semiconductor layer 111, so that the semiconductor layer 111 and the piezoelectric layer 10 are at the bonding interface. As stated above, a dielectric layer (not shown in figure 6E) can be formed beforehand on one and/or the other of these layers in order to promote bonding. If necessary, a charge trapping layer (not shown in figure 6E) may be formed between said dielectric layer and
30 the piezoelectric layer. Said trapping layer is advantageously formed after implantation performed in the piezoelectric substrate 118. Under these conditions a low-temperature method is required. For example a layer of amorphous silicon is deposited on the piezoelectric substrate or a layer of polycrystalline silicon is deposited on a dielectric layer formed on the semiconductor layer 111.

35 In cases where it is wished to form a bulk acoustic wave device, the bonding may be achieved by means of a metallic layer, said layer then fulfilling the role of an electrode buried in the device.

Then the piezoelectric donor substrate 118 is split along the embrittlement zone 119 so as to transfer the piezoelectric layer 10 onto the semiconductor layer 111. Thinning of the piezoelectric layer may be implemented if necessary in order to remove defects associated with the implantation.

5 In the case where the semiconductor layer does not comprise electronic components, the Smart Cut™ method can also be implemented in order to transfer the semiconductor layer 111 onto the stiffening substrate 110. This process is well known to those skilled in the art. In particular, an embrittlement zone is formed by implantation of atomic species in the donor substrate 116, so as to demarcate a layer to be transferred
10 which comprises the layer 111. This implantation also uses hydrogen and/or helium atoms, and those skilled in the art are able to determine the implantation dose and energy depending on the donor substrate material and the depth to be reached. Then, after bonding of the donor substrate onto the stiffening substrate 110, the donor substrate is detached along the embrittlement zone, where this detachment may be initiated
15 mechanically, chemically or by other means.

In the event that it is wished to manufacture a surface acoustic wave device, metallic electrodes in the form of two interdigitated combs are then deposited on the surface of the piezoelectric layer 10.

In the event that it is wished to manufacture a bulk acoustic wave device, the steps
20 described above must be adapted. On the one hand, before the bonding step shown in figure 6E, a first electrode is deposited on the free surface of the piezoelectric layer 10 forming part of the piezoelectric donor layer, where this first electrode is located buried in the final stack. After the transfer of the piezoelectric layer 10 onto the semiconductor layer 111, a second electrode is deposited onto the free surface of the piezoelectric layer that is
25 away from the first electrode. On the other hand, in order prevent propagation of acoustic waves in the semiconductor layer 111 and in the stiffening substrate 110, a means of isolation may be incorporated into the semiconductor layer 111, where the means of isolation can be, for example, a Bragg mirror (as shown in figure 2) or a cavity etched into the semiconductor layer 111.

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REFERENCES

[1] Hashimoto et al, Recent Development of Temperature Compensated SAW Devices, Ultrasonics Symposium (IUS), 18-21 Oct. 2011, pp. 79-86, 2011 IEEE International

35 FR 2 816 445

CLAIMS

1. Substrate (1) for a surface acoustic wave device or bulk acoustic wave device which comprises a support substrate (11) and an piezoelectric layer (10) on said support
5 substrate, characterised in that the support substrate (11) comprises a semiconductor layer (111) on a stiffening substrate (110) which has a coefficient of thermal expansion closer to the coefficient of thermal expansion of the material of the piezoelectric layer (10) than that of silicon, where the semiconductor layer (111) is arranged between the piezoelectric layer (10) and the stiffening substrate (110), the substrate (1) being
10 characterised in that it comprises a dielectric layer (114) between the piezoelectric layer (10) and the semiconductor layer (111) and a charge trapping layer (115) at the interface between said dielectric layer and the semiconductor layer and/or the interface between the dielectric layer and the piezoelectric layer.
- 15 2. Substrate according to claim 1, characterised in that the stiffening substrate (110) comprises sapphire, glass and/or spinel (MgAl_2O_4).
3. Substrate according to one of claims 1 or 2 characterised in that the semiconductor layer (111) is formed from one of the following materials: silicon,
20 germanium, SiGe, SiC, III-V material.
4. Substrate according to one of claims 1 to 3 characterised in that the semiconductor layer (111) comprises at least one electronic component (112).
- 25 5. Substrate according to claim 4, characterised in that said electronic component (112) is chosen from: a CMOS transistor, a switch and a power amplifier.
6. Substrate according to one of claims 1 to 5, characterised in that the ratio of the thickness of the piezoelectric layer (10) to the thickness of the stiffening substrate
30 (110) is less than or equal to 0.125.
7. Substrate according to one of claims 1 to 6 characterised in that the thickness of the piezoelectric layer (10) is less than 50 μm , preferably less than 20 μm , yet more preferably less than 1 μm , and the thickness of the stiffener substrate (110) is between
35 400 and 800 μm .
8. Substrate according to one of claims 1 to 7, characterised in that said charge trapping layer (115) comprises a layer of polycrystalline silicon.

9. Surface acoustic wave device comprising a substrate (1) according to one of claims 1 to 8 and two electrodes (12, 13) formed of two interdigitated metallic combs on the surface of the piezoelectric layer (10).

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10. Bulk acoustic wave device comprising a substrate (1) according to one of claims 1 to 8 and two electrodes (12, 13) arranged on either side of the piezoelectric layer (10).

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11. Method of manufacturing a substrate (1) for a surface acoustic wave device or bulk acoustic wave device which comprises a support substrate (11) and a piezoelectric layer (10) on said support substrate, characterised in that it comprises:

- providing a first donor substrate (116) comprising a semiconductor layer (111),
- providing a stiffening substrate (110) which has a coefficient of thermal expansion
- 15 closer to the coefficient of thermal expansion of the material of the piezoelectric layer (10) than that of silicon,
- transferring the semiconductor layer (111) onto the stiffening substrate (110) from a first donor substrate (116),
- providing a second donor substrate (118) comprising the piezoelectric layer (10),
- 20 - transferring the piezoelectric layer (10) onto the semiconductor layer (111) from the second donor substrate (118);
- forming a dielectric layer (114) on one and/or the other of the piezoelectric layer (10) and the semiconductor layer (111); and
- forming a charge trapping layer (115) at the interface between said dielectric layer
- 25 and the semiconductor layer and/or the interface between the dielectric layer and the piezoelectric layer.

12. Method according to claim 11, wherein at least one of the transfer steps comprises the following sub-steps:

- 30 - formation of an embrittlement zone in the first, second donor substrate respectively by the implantation of atomic species;
- bonding of the first, second donor substrate respectively onto the stiffening substrate and semiconductor layer respectively;
- detachment of said first, second substrates respectively along the embrittlement
- 35 zone.