

Description

The present invention relates to a method of manufacturing a bipolar semiconductor device, comprising the steps of: selectively forming a buried layer of a second conductivity type in a surface region of a semiconductor substrate of a first conductivity type opposite to said second conductivity type; forming at least one insulating film on said semiconductor substrate; and forming at least one monocrystalline silicon layer of the second conductivity type on said buried layer in an opening of said insulating film, said monocrystalline silicon layer having a base region of the first conductivity type and an emitter region of the second conductivity type formed in said base region of the first conductivity type, and forming a conductive layer buried in said insulating film and connected to said base region of the first conductivity type.

Such a method is known from EP-A-0 102 075.

Various conventional techniques have been proposed to improve the high-speed, high-frequency characteristics of a bipolar semiconductor device. Examples of these techniques include selective epitaxy and a combination of a super self-aligned structure, wherein polycrystalline silicon is used as an electrode for connection with a base region, and trench isolation technique. The latter combination is described, e.g. in the following: "Gigabit Logic Bipolar Technology, Advanced Super Self-Aligned Process Technology", Electronics Letters, Vol. 19, No. 18 (1983); "1.25 μm Deep-Groove-Isolated Self-Aligned ECL Circuits", ISSCC82, IBM; and S.K. Wiedmann, "Status and Trends of PL/MTL Technology", IEDM Tech. Dig. pp. 47-50 (1983). Selective epitaxy is described, e.g. in H.J. Voss et al. "Device Isolation Technology by Selective Low-Pressure Silicon Epitaxy", IEDM Tech. Dig. pp. 35-38 (1983). N. Ohuchi et al. "A New Self-Aligned Transistor Structure for High-Speed and Low-Power Bipolar LSIs", IEDM Tech. Dig. pp. 55-58 (1983) describes a technology using both techniques mentioned above.

A bipolar transistor of a super self-aligned structure has been proposed which uses polycrystalline silicon as an electrode for connection with the base. Such a bipolar transistor is described, e.g. in N. Sasaki et al. "Bipolar Process Technology Evaluation by 3-Dimensional Device Simulation", IEDM Tech. Dig. pp. 546-549 (1983).

In the high-speed bipolar semiconductor devices described in the above texts, base resistance r_{bb} influences the operation speed of the circuit most (i.e. it has the largest sensitivity coefficient) among device constants (see Sotomura and Yamazaki, "Development and Mass Production of Ultra High-Speed ECL Logic HD100K Series", Hitachi Rompyo, pp. 59-62 (1982). Therefore, it is

desirable to further reduce the base resistance r_{bb} in order to improve the operation speed and high-frequency characteristics of the bipolar transistor.

When polycrystalline silicon is used as an electrode for connection with a base region, however, further micropatterning of presently available semiconductor devices is difficult since the sheet resistance of polycrystalline silicon is several tens to several hundreds of $\Omega/\square$.

According to another conventional technique, a high-melting metal or a silicide thereof such as MoSi_2 , which has a low sheet resistance, is used in the super self-aligned structure as an electrode for connection with the base in place of polycrystalline silicon, thereby decreasing base resistance r_{bb} .

However, these techniques are not practical because ohmic contact between such an alternative material and the base region is difficult to obtain. In addition, it is difficult to use these alternative materials as diffusion sources for the formation of external base regions.

It is an object of the present invention to provide a method of manufacturing a semiconductor device having a small base resistance.

According to the invention, the method initially defined is characterized in that the step of forming said monocrystalline silicon layer and said conductive layer comprises the steps of: forming in a first step a semiconductor layer to be buried in said insulating film and containing an impurity of the first conductivity type, and forming a conductive layer connected thereto in order to decrease base connection resistance, the semiconductor layer lying on a side wall of said conductive layer; subsequently forming a monocrystalline silicon layer to be buried in the insulating layer on said buried layer, said monocrystalline silicon layer being in contact with said semiconductor layer, and diffusing the impurity of the first conductivity type contained in said semiconductor layer into said monocrystalline silicon layer, thus forming at least a portion of said base region of the first conductivity type.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Figs. 1 to 12 are sectional views showing steps of manufacturing a semiconductor device according to an embodiment of the present invention;

Fig. 13 is a sectional view of a semiconductor device which is manufactured by a method according to an embodiment of the present invention;

Fig. 14 is a plan view of the semiconductor device shown in Fig. 13; and

Fig. 15 is a sectional view of a semiconductor

device manufactured by a method according to another embodiment of the present invention.

A method of manufacturing a semiconductor device according to an embodiment of the present invention will be described with reference to Figs. 1 to 14. In Figs. 1 to 14, polycrystalline silicon portions are dotted to distinguish them from monocrystalline silicon portions.

(1) An n-type impurity such as antimony (Sb) is selectively diffused into part of p-type silicon substrate 1 with an impurity concentration of 10^{14} to $10^{15}/\text{cm}^2$ and a resistivity of 20 to 50 $\Omega\cdot\text{cm}$ to form n⁺-type buried layer 3. Silicon oxide film 5 having a thickness of 0.5 to 1 μm is formed on the entire surface of the resultant structure by, e.g., a CVD method. A molybdenum silicide film (to be referred to as MoSi_2 film hereinafter) having a thickness of 0.5 to 2 μm is formed on the resultant structure by sputtering. The film is patterned to form MoSi_2 pattern 7, part of which is left to serve as part of a base connection electrode to be described later. Note that pattern 7 has a sheet resistance of about 2 $\Omega/\square$. The structure shown in Fig. 1 is thus obtained.

(2) Oxide film 9 of 1 to 2 μm thickness is deposited on the entire surface of the structure shown in Fig. 1 by, e.g., a CVD method. Photoresist R1 is applied thereon, resulting in the structure shown in Fig. 2.

(3) Photoresist R1 and film 9 are etched using reactive ion etching (RIE) under the condition that the etching rate of photoresist R1 is virtually identical with that of film 9. The entire surfaces of photoresist R1 and film 9 are thus etched back so that the surfaces of pattern 7 and film 9 are virtually flush. This results in the structure shown in Fig. 3. Note that pattern 7 is buried in film 9 as shown in Fig. 3.

(4) The portion of pattern 7 corresponding to the prospective base-emitter formation region is selectively etched by RIE or chemical dry etching (CDE) to form opening 11 with a width of about 4 μm in film 7, resulting in the structure shown in Fig. 4.

(5) Polycrystalline silicon film 13, having a thickness of 0.5 μm , is formed on the entire surface of the structure shown in Fig. 4 by, e.g., LP (low pressure) CVD. Boron is ion-implanted into film 13 at an acceleration energy of 30 to 40 keV and a dose of about 10^{15} to $10^{16}/\text{cm}^2$. The resultant structure is annealed in an N_2 atmosphere at 800 to 1,000 $^\circ\text{C}$, thereby activating the boron in film 13. In this case, the boron is diffused at a considerable speed and distributed uniformly in film 13. As a result, the sheet resistance of film 13 is about 50 to 500 $\Omega/\square$. The resultant structure is shown in Fig. 5.

(6) Polycrystalline silicon film pattern 13 is etched by RIE so that the only remaining portion lies on a side wall of pattern 7. This can be easily done by anisotropically etching film 13. Photoresist pattern R2 is formed on the resultant structure excluding at least a prospective collector formation region, resulting in the structure shown in Fig. 6.

(7) Film 5 is etched by RIE using photoresist pattern R2, remaining film 13, and pattern 7 as masks so that portions of layer 3 are exposed. Opening 15 is formed over a prospective base-emitter formation region and opening 17, over a prospective collector connection formation region. This results in the structure shown in Fig. 7.

(8) Monocrystalline silicon layers (epitaxial layers) 19 and 21 having thicknesses of about 1 μm are grown in openings 15 and 17 on layer 3 by selective epitaxy. In the same step, polycrystalline silicon layer 23, having a thickness of about 0.3 μm , is formed on films 9 and patterns 7 and 13. Layer 23 has a resistivity of 1.5 to 2 $\Omega\cdot\text{cm}$. Note that the dashed line in Fig. 8 indicates a boundary between the monocrystalline silicon layer and the polycrystalline silicon layer, i.e., a transition region.

Phosphorus is ion-implanted in layer 21, which serves as a collector connection region. Annealing is then performed to form an n⁺-type collector connection region (21) reaching buried layer 3. Simultaneously, boron is diffused from remaining films 13 and 23 into layer 19 to form p-type graft (external) base region 25 having a width of about 0.5 μm . The resultant structure is shown in Fig. 8.

(9) Thermal oxidation is performed to form thermal oxide film 27 having a thickness of about 50 to 100 nm on the surfaces of layers 19, 21, and 23. Silicon nitride film 29 is formed on the entire surface of the resultant structure to a thickness of 50 to 100 nm by a CVD method. Photoresist R3 is applied thereon (as indicated by the dashed line in Fig. 9), and is baked to etch back the resultant structure. Photoresist pattern R3 thus remains only on the (recessed) portions of film 29 corresponding to layers 19 and 21, resulting in the structure shown in Fig. 9.

(10) Film 29 is removed by a CDE method using pattern R3 as a mask. Exposed portions of film 27 are removed using a dilute oxygen fluoride solution. Films 27 and 29 and pattern R3 thus remain only on layers 19 and 21. Pattern R3 is then removed. Using remaining film 29 as an oxidation resistant mask, selective oxidation is performed in a hydrogen combustion atmosphere at 950 to 1,000 $^\circ\text{C}$ to convert most of layer 23 and portions of the surface regions of

layers 19 and 21 into thermal oxide film 31. The resultant structure is shown in Fig. 10.

(11) Films 29 are removed. Photoresist pattern R4 is formed to cover collector connection region 21 (as indicated by the dashed line in Fig. 11). Using pattern R4 and film 31 as masks, boron is ion-implanted into layer 19 through films 27 at an acceleration energy of 30 to 40 keV and a dose of 1 to $2 \times 10^{14}/\text{cm}^2$. Pattern R4 is then removed. Annealing is performed at a temperature of 800 to 1,000°C to activate the boron in monocrystalline silicon layer 19. P-type active base region 33 is thus formed. The remaining portion of layer 19 becomes the collector of the transistor. The resultant structure is shown in Fig. 11.

(12) Films 27 are washed out to form (exposed) emitter opening portion 35 and collector opening portion 37 having widths of about 2 μm . Arsenic or phosphorus is ion-implanted in the entire surface of the structure or selectively in opening 35 at an acceleration energy of 40 to 80 keV and a dose of 5×10^{15} to $2 \times 10^{16}/\text{cm}^2$. Annealing is then performed in a dry oxide atmosphere to activate the impurity, thereby obtaining desired current amplification ratio β and forming n⁺-type emitter region 39. The resultant structure is shown in Fig. 12.

(13) Part of film 31 is selectively etched to form opening 41 on pattern 7 for connection with the base. Pretreatment is performed for forming an electrode. An aluminum-silicon (1.2%) alloy film is formed on the entire surface of the resultant structure by sputtering. The alloy film is patterned and sintered to form emitter electrode 43, base electrode 45, and collector electrode 47. This results in an npn bipolar transistor, of which a sectional view is shown in Fig. 13 and a plan view is shown in Fig. 14. Fig. 14 shows positional relationships among respective portions, so portions unnecessary for the explanation are omitted for the sake of clarity. The sectional view of Fig. 13 is taken along the line A - A of Fig. 14.

By the above-mentioned steps, a semiconductor device is obtained which has: p-type semiconductor substrate 1; n⁺-type buried layer 3 formed in the surface region of substrate 1; insulating films 5 and 9 formed on substrate 1 and having openings 15 and 17; n⁺-type monocrystalline silicon layer 21 buried in opening 17 to be directly connected to buried layer 3; n-type monocrystalline silicon layer 19 which is buried in opening 15, is directly connected to layer 3, and serves as a collector connection region; p-type diffusion layers 25 and 33 selectively formed in layer 19 and serving as bases; n⁺-type diffusion layer 39 selectively formed in layers 25 and 33 and serving as an

emitter; p-type polycrystalline silicon layer 13 which is formed on the surface regions of films 5 and 9 to be buried in films 5 and 9, is connected to regions 25 and 33, and serves as part of the base connection region; MoSi₂ layer 7 which is formed on the surface region of films 5 and 9, is connected to layer 13, and serves as part of the base connection region; emitter electrode 32; base electrode 45; and collector electrode 47.

In the bipolar transistor having the above structure, film 13 is provided between layer 19 and film 7 as a kind of buffer. Assume that most of the base region connection region (electrode) is constituted by pattern 7, which cannot easily maintain ohmic contact with layer 19. In this case, good ohmic contact can be obtained between graft base region 25 and film 7 because of the presence of film 13 therebetween. In addition, most of the base region connection region (electrode) is constituted by pattern 7, which has a small sheet resistance. Therefore, the resistance of the base connection region and hence the base resistance can be greatly reduced. High-speed and high-frequency characteristics of the bipolar semiconductor device are improved accordingly over conventional bipolar semiconductor devices. Layer 13 serves as a diffusion source for forming graft base region 25. In this manner, the structure is more effective than that which would be obtained by merely replacing the polycrystalline silicon base connection region with an MoSi₂ base connection region.

The effect of reducing the base resistance will be described with reference to Fig. 14. Assume that emitter stripe length X is 4 μm , width W of film 7 is 8 μm , and distance L between pattern 13 and contact hole 41 for base electrode 45 is 4.5 μm .

In Fig. 14, assume that the sheet resistances of region 33 and region 25 are 1 k $\Omega/\square$ and 50 $\Omega/\square$, respectively, which are the same as those of a conventional bipolar semiconductor device. In the present device pattern 7 replaces the polycrystalline silicon layer between film 13 and contact hole 41 for base electrode 45. Note that sheet resistance p1 of film 13 is 100 $\Omega/\square$ and sheet resistance p2 of pattern 7 is about 2 $\Omega/\square$. The decrease in base resistance rbb can thus be approximated as:

$$\begin{aligned}\Delta r_{bb} &= (p_1 - p_2)L/W \\ &= 98 \times 4.5 / 8 \\ &= 55 \Omega\end{aligned}$$

In practice, the entire base region is surrounded by pattern 7 so that base resistance rbb is further reduced. A bipolar transistor having this structure and one having the conventional structure (i.e., one in which the base connection region is made of polycrystalline silicon) were prepared, and the base resistances of both were compared. Base resistance rbb of the conventional device was 150 Ω whereas that of the present device was 80 Ω ,

about half that of the conventional device. Note that the shorter emitter stripe length X, the larger the L/W ratio. Base resistance reduction is thus enhanced in this case.

In the above embodiment, a washed emitter technique is used to form region 39 and electrode 43. In devices obtained using the washed emitter technique, the base and the emitter may short-circuit. In order to prevent this, the semiconductor device may be manufactured in the following manner. Polycrystalline silicon film pattern 51, doped with an n-type impurity, is formed after the formation of active base region 33. Protection film 53 is deposited on the entire surface of the resultant structure. An impurity is diffused from pattern 51 to form emitter region 39. After the formation of contact holes 55, 57, and 59, emitter, base, and collector electrodes 43, 45, and 47 are formed. The resultant semiconductor device is shown in Fig. 15.

In the above embodiment, p-type polycrystalline silicon layer 13 is formed to serve as a p-type impurity diffusion source and allow ohmic contact between monocrystalline silicon and a high-melting metal. However, the present invention is not limited to polycrystalline silicon.

In the above embodiment, monocrystalline silicon constitutes the collector connection region. However, the present invention is not limited to this. High-melting metals such as Mo, Ti and W or silicides thereof which are resistant to high-temperature annealing at about 1,200°C can be used in place of monocrystalline silicon. Polycrystalline silicon can also be used.

An n-type impurity may be rediffused from buried layer 3 into monocrystalline silicon layer 19 during diffusion of an n-type impurity into monocrystalline silicon layer 21, thereby reducing the emitter-collector breakdown voltage. In order to prevent this, the collector connection region may be formed, e.g. by polycrystalline silicon, a high-melting metal, or a silicide thereof. Opening 15 is formed for the formation of the transistor, and monocrystalline silicon layer 19 is then grown.

With the above structure, a portion of the base connection region (connection electrode) is made of a material such as a high-melting metal or a silicide thereof, both of which have good conductivity. Resistance of the base connection region and hence the base resistance is thus greatly decreased. Therefore, high-speed, high-frequency characteristics can be greatly improved over conventional bipolar semiconductor devices. In addition, the electrode for connection with the base can have substantial ohmic contact with the base region, and the base connection region can be used as a diffusion source for formation of the base. This benefit cannot be obtained by merely replacing a conventional base connection region with a high-

melting metal.

The conductivity types of the respective portions of the semiconductor device according to the present invention are not limited to those employed in this embodiment. P- and n-type conductivity types can be exchanged to obtain the same effect. The present invention is not limited to a device having a single collector or a single emitter structure but can be applied to a device having a multi-emitter or multi-collector structure. The values indicated in the above embodiment are merely examples and should not be taken as fixed values.

Claims

1. A method of manufacturing a bipolar semiconductor device, comprising the steps of:

selectively forming a buried layer (3) of a second conductivity type in a surface region of a semiconductor substrate (1) of a first conductivity type opposite to said second conductivity type;

forming at least one insulating film (5,9) on said semiconductor substrate (1); and

forming at least one monocrystalline silicon layer (19) of the second conductivity type on said buried layer (3) in an opening of said insulating film (5,9), said monocrystalline silicon layer (19) having a base region (25,33) of the first conductivity type and an emitter region (39) of the second conductivity type formed in said base region of the first conductivity type, and forming a conductive layer (7,13) buried in said insulating film (5,9) and connected to said base region (25,33) of the first conductivity type; characterized in that the step of forming said monocrystalline silicon layer and said conductive layer comprises the steps of:

forming in a first step a semiconductor layer (13) to be buried in said insulating film (5,9) and containing an impurity of the first conductivity type, and forming a conductive layer (7) connected thereto in order to decrease base connection resistance, the semiconductor layer lying on a side wall of said conductive layer;

subsequently forming a monocrystalline silicon layer (19) to be buried in the insulating layer on said buried layer (3), said monocrystalline silicon layer (19) being in contact with said semiconductor layer (13), and diffusing the impurity of the first conductivity type contained in said semiconductor layer (13) into said monocrystalline silicon layer (19), thus forming at least a portion (25) of said base region (25,33) of the first conductivity type.



about half that of the conventional device. Note that the shorter emitter stripe length X, the larger the L/W ratio. Base resistance reduction is thus enhanced in this case.

In the above embodiment, a washed emitter technique is used to form region 39 and electrode 43. In devices obtained using the washed emitter technique, the base and the emitter may short-circuit. In order to prevent this, the semiconductor device may be manufactured in the following manner. Polycrystalline silicon film pattern 51, doped with an n-type impurity, is formed after the formation of active base region 33. Protection film 53 is deposited on the entire surface of the resultant structure. An impurity is diffused from pattern 51 to form emitter region 39. After the formation of contact holes 55, 57, and 59, emitter, base, and collector electrodes 43, 45, and 47 are formed. The resultant semiconductor device is shown in Fig. 15.

In the above embodiment, p-type polycrystalline silicon layer 13 is formed to serve as a p-type impurity diffusion source and allow ohmic contact between monocrystalline silicon and a high-melting metal. However, the present invention is not limited to polycrystalline silicon.

In the above embodiment, monocrystalline silicon constitutes the collector connection region. However, the present invention is not limited to this. High-melting metals such as Mo, Ti and W or silicides thereof which are resistant to high-temperature annealing at about 1,200°C can be used in place of monocrystalline silicon. Polycrystalline silicon can also be used.

An n-type impurity may be rediffused from buried layer 3 into monocrystalline silicon layer 19 during diffusion of an n-type impurity into monocrystalline silicon layer 21, thereby reducing the emitter-collector breakdown voltage. In order to prevent this, the collector connection region may be formed, e.g. by polycrystalline silicon, a high-melting metal, or a silicide thereof. Opening 15 is formed for the formation of the transistor, and monocrystalline silicon layer 19 is then grown.

With the above structure, a portion of the base connection region (connection electrode) is made of a material such as a high-melting metal or a silicide thereof, both of which have good conductivity. Resistance of the base connection region and hence the base resistance is thus greatly decreased. Therefore, high-speed, high-frequency characteristics can be greatly improved over conventional bipolar semiconductor devices. In addition, the electrode for connection with the base can have substantial ohmic contact with the base region, and the base connection region can be used as a diffusion source for formation of the base. This benefit cannot be obtained by merely replacing a conventional base connection region with a high-

melting metal.

The conductivity types of the respective portions of the semiconductor device according to the present invention are not limited to those employed in this embodiment. P- and n-type conductivity types can be exchanged to obtain the same effect. The present invention is not limited to a device having a single collector or a single emitter structure but can be applied to a device having a multi-emitter or multi-collector structure. The values indicated in the above embodiment are merely examples and should not be taken as fixed values.

Claims

1. A method of manufacturing a bipolar semiconductor device, comprising the steps of:

selectively forming a buried layer (3) of a second conductivity type in a surface region of a semiconductor substrate (1) of a first conductivity type opposite to said second conductivity type;

forming at least one insulating film (5,9) on said semiconductor substrate (1); and

forming at least one monocrystalline silicon layer (19) of the second conductivity type on said buried layer (3) in an opening of said insulating film (5,9), said monocrystalline silicon layer (19) having a base region (25,33) of the first conductivity type and an emitter region (39) of the second conductivity type formed in said base region of the first conductivity type, and forming a conductive layer (7,13) buried in said insulating film (5,9) and connected to said base region (25,33) of the first conductivity type; characterized in that the step of forming said monocrystalline silicon layer and said conductive layer comprises the steps of:

forming in a first step a semiconductor layer (13) to be buried in said insulating film (5,9) and containing an impurity of the first conductivity type, and forming a conductive layer (7) connected thereto in order to decrease base connection resistance, the semiconductor layer lying on a side wall of said conductive layer;

subsequently forming a monocrystalline silicon layer (19) to be buried in the insulating layer on said buried layer (3), said monocrystalline silicon layer (19) being in contact with said semiconductor layer (13), and diffusing the impurity of the first conductivity type contained in said semiconductor layer (13) into said monocrystalline silicon layer (19), thus forming at least a portion (25) of said base region (25,33) of the first conductivity type.



2. A method according to claim 1, characterized in that the step of forming said semiconductor layer (13) and said conductive layer (7) comprises the steps of:

forming a conductive layer (7) in the surface region of said insulating film (5,9) to be buried therein;

forming an opening in said conductive layer (7);

forming a semiconductor layer (13) containing an impurity of the first conductivity type in at least said opening (11); and

forming an opening in said semiconductor layer (13) above said buried layer (3); and the step of forming said monocrystalline silicon layer (19) comprises the steps of:

forming an opening (15) in said insulating film (5) under said opening in said semiconductor layer (13) using said semiconductor layer (13) as a mask; and

growing a monocrystalline silicon layer (19) in said opening (15) of said insulating film (5) on said buried layer (3), allowing said monocrystalline silicon layer (19) to contact said semiconductor layer (13), and diffusing the impurity of the first conductivity type contained in said semiconductor layer (13) into said monocrystalline silicon layer (19).

3. A method according to claim 1 or 2, characterized in that said semiconductor layer (13) is made of polycrystalline silicon capable of substantial ohmic contact with said base region (25,33) of the first conductivity type, and said conductive layer (7) is made of a member selected from the group consisting of high-melting metals and silicides thereof that are capable of substantial ohmic contact with said polycrystalline silicon constituting said semiconductor layer (13).

Patentansprüche

1. Ein verfahren zum Herstellen einer bipolaren Halbleitervorrichtung, welche folgende Schritte umfaßt:
 selektives Bilden einer beerdigten Schicht (3) eines zweiten Leitungstyps in einer Oberflächenregion eines Halbleitersubstrats (1) eines ersten dem zweiten Leitungstyp entgegengesetzten Leitungstyps;
 Bilden von zumindest einem isolierenden Film (5, 9) auf dem Halbleitersubstrat (1); und
 Bilden zumindest einer monokristallinen Siliziumschicht (19) des zweiten Leitungstyps auf der beerdigten Schicht (3) in einer Öffnung des isolierenden Films (5, 9), wobei die monokristalline Siliziumschicht (19) eine Basisregion

(25, 33) des ersten Leitungstyps und eine Emitterregion (39) des zweiten Leitungstyps, die ausgebildet ist in der Basisregion des ersten Leitungstyps, hat, und Bilden einer leitenden Schicht (7, 13) beerdigt in dem isolierenden Film (5, 9) und verbunden mit der Basisregion (25, 33) des ersten Leitungstyps;

dadurch **gekennzeichnet**, daß der Schritt des Bildens der monokristallinen Siliziumschicht und der leitfähigen Schicht folgende Schritte aufweist:

Bilden in einem ersten Schritt einer in dem isolierenden Film (5, 9) zu beerdigenden Halbleiterschicht (13), welche Fremdatome des ersten Leitungstyps enthält, und Bilden einer damit verbundenen leitenden Schicht (7), um den Basisverbindungswiderstand abzusinken, wobei die Halbleiterschicht an einer Seitenwand der leitenden Schicht liegt;

anschließendes Bilden einer in der isolierenden Schicht auf der beerdigten Schicht (3) zu beerdigenden monokristallinen Siliziumschicht (19), wobei die monokristalline Siliziumschicht (19) in Kontakt mit der Halbleiterschicht (13) ist, und Diffundieren der Fremdatome des ersten Leitungstyps, welche in der Halbleiterschicht (13) enthalten sind, in die monokristalline Siliziumschicht (19), wobei zumindest ein Teil (25) der Basisregion (25, 33) des ersten Leitungstyps gebildet wird.

2. Verfahren nach Anspruch 1, dadurch **gekennzeichnet**, daß der Schritt des Bildens der Halbleiterschicht (13) und der leitenden Schicht (7) die folgenden Schritte umfaßt:

Bilden einer leitenden Schicht (7) in der Oberflächenregion des isolierenden Films (5, 9), um darin begraben zu werden;

Bilden einer Öffnung in der leitenden Schicht (7);

Bilden einer Halbleiterschicht (13), welche Fremdatome des ersten Leitungstyps enthält, in zumindest der Öffnung (11); und

Bilden einer Öffnung in der Halbleiterschicht (13) über der begrabenen Schicht (3); und der Schritt des Bildens der monokristallinen Siliziumschicht (19) folgende Schritte umfaßt:

Bilden einer Öffnung (15) in dem isolierenden Film (5) unter der Öffnung in der Halbleiterschicht (13) unter Benutzung der Halbleiterschicht (13) als Maske; und

Züchten einer monokristallinen Siliziumschicht (19) der Öffnung (15) des isolierenden Films (5) auf der begrabenen Schicht (3), wobei die monokristalline Siliziumschicht (19) die Halbleiterschicht (13) kontaktieren darf, und Diffundieren der Fremdatome des ersten Leitungstyps,



die in der Halbleiterschicht (13) enthalten sind, in die monokristalline Siliziumschicht (19).

3. Verfahren nach Anspruch 1 oder 2, dadurch **gekennzeichnet**, daß die Halbleiterschicht (13) hergestellt ist aus polykristallinem Silizium und fähig zu substantiell ohm'schen Kontakt mit der Basisregion (25, 33) des ersten Leitungstyps, und die leitende Schicht (17) hergestellt ist aus einem Element ausgewählt aus der Gruppe bestehend aus hochschmelzenden Metallen und deren Siliziden, welche fähig sind zu im wesentlichen ohm'schen Kontakt mit dem polykristallinen Silizium, welches die Halbleiterschicht (13) bildet.

Revendications

1. Procédé de fabrication d'un dispositif à semi-conducteur bipolaire, comprenant les étapes de :

formation de façon sélective d'une couche enterrée (3) d'un second type de conductivité dans une région de surface d'un substrat semi-conducteur (1) d'un premier type de conductivité opposé audit second type de conductivité ;

formation d'au moins un film isolant (5, 9) sur ledit substrat semi-conducteur (1) ; et

formation d'au moins une couche de silicium monocristallin (19) du second type de conductivité sur ladite couche enterrée (3) dans une ouverture dudit film isolant (5, 9), ladite couche de silicium monocristallin (19) comportant une région de base (25, 33) du premier type de conductivité et une région d'émetteur (39) du second type de conductivité formée dans ladite région de base du premier type de conductivité, et formation d'une couche conductrice (7, 13) enterrée dans ledit film isolant (5, 9) et connectée à ladite région de base (25, 33) du premier type de conductivité ;

caractérisé en ce que l'étape de formation de ladite couche de silicium monocristallin et de ladite couche conductrice comprend les étapes de :

formation lors d'une première étape d'une couche semiconductrice (13) qui doit être enterrée dans ledit film isolant (5, 9) et qui contient une impureté du premier type de conductivité et formation d'une couche conductrice (7) qui lui est connectée afin de diminuer une valeur de résistance de connexion de base, la couche semiconductrice reposant sur une paroi latérale de ladite couche conductrice ;

formation ensuite d'une couche de silicium

monocristallin (19) qui doit être enterrée dans la couche isolante, sur ladite couche enterrée (3), ladite couche de silicium monocristallin (19) étant en contact avec ladite couche semiconductrice (13), et diffusion de l'impureté du premier type de conductivité contenue dans ladite couche semiconductrice (13) dans ladite couche de silicium monocristallin (19), d'où la formation d'au moins une partie (25) de ladite région de base (25, 33) du premier type de conductivité.

2. Procédé selon la revendication 1, caractérisé en ce que l'étape de formation de ladite couche semiconductrice (13) et de ladite couche conductrice (7) comprend les étapes de :

formation d'une couche conductrice (7) dans la région de surface dudit film isolant (5, 9) afin qu'elle soit enterrée dedans ;

formation d'une ouverture dans ladite couche conductrice (7) ;

formation d'une couche semiconductrice (13) contenant une impureté du premier type de conductivité dans au moins ladite ouverture (11) ; et

formation d'une ouverture dans ladite couche semiconductrice (13) au-dessus de ladite couche enterrée (3) ; et

l'étape de formation de ladite couche de silicium monocristallin (19) comprend les étapes de :

formation d'une ouverture (15) dans ledit film isolant (5) au-dessous de ladite ouverture ménagée dans ladite couche semiconductrice (13) en utilisant ladite couche semiconductrice (13) en tant que masque ; et

obtention par croissance d'une couche de silicium monocristallin (19) dans ladite ouverture (15) dudit film isolant (5) sur ladite couche enterrée (3), ceci permettant l'entrée en contact de ladite couche de silicium monocristallin (19) avec ladite couche semiconductrice (13), et diffusion de l'impureté du premier type de conductivité contenue dans ladite couche semiconductrice (13) dans ladite couche de silicium monocristallin (19).

3. Procédé selon la revendication 1 ou 2, caractérisé en ce que ladite couche semiconductrice (13) est réalisée en un silicium polycristallin qui permet un contact ohmique significatif avec ladite région de base (25, 33) du premier type de conductivité et ladite couche conductrice (7) est réalisée en un élément choisi dans le groupe constitué par des métaux à point de fusion élevé et par des siliciures de ces métaux qui permettent un contact ohmique significatif avec ledit silicium polycristallin qui consti-



tue ladite couche semiconductrice (13):

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