CLAIMS

~~What is claimed is:~~

1. A method of making a semiconductor device, comprising:

providing a semiconductor die comprising a spacer element coupled to a first surface of the semiconductor die;

coupling the ~~constructing a~~ spacer element to a carrier to create a gap between the first surface of ~~coupled with a surface of a semiconductor die unit, wherein the spacer element is configured to create a gap between~~ the semiconductor die ~~unit and a surface of a~~ and the carrier; ~~and~~

disposing a mold compound around ~~encapsulating~~ the semiconductor die ~~unit within a mold compound, wherein the encapsulating comprises introducing the mold compound into~~ and within the gap; and

uncoupling the spacer element from the carrier after the mold compound is disposed around the semiconductor die.

2. The method of claim 1, further comprising attaching the spacer element to the carrier prior to introducing the mold compound into the gap.

3. The method of claim 1, further comprising:

prior to disposing mold compound around ~~encapsulating~~ the semiconductor die ~~unit~~, thinning a semiconductor wafer on which the semiconductor die ~~unit~~ is constructed; and

dicing the semiconductor wafer to separate the semiconductor die ~~unit~~ from a plurality of other semiconductor die ~~units~~.

4. The method of claim 1, wherein disposing mold compound around ~~encapsulating~~ the semiconductor die ~~within the mold compound~~ further comprises performing a compression molding process.

5. The method of claim 1, wherein a first thickness of the mold compound on the top of the semiconductor die ~~unit~~ is less than three times a second thickness of the mold compound under the bottom of the semiconductor die ~~unit~~.

6. The method of claim 1, wherein the spacer element comprises at least one conductive post that is electrically coupled with at least one bond pad of the semiconductor die ~~unit~~.

7. The method of claim 6, further comprising exposing the at least one conductive post at an exterior surface of the mold compound.

8. The method of claim 6, further comprising, prior to encapsulating the semiconductor die ~~unit~~ within the mold compound, constructing a fan-in redistribution layer (RDL) structure that is electrically coupled with a plurality of bond pads of the semiconductor die ~~unit~~, wherein the at least one conductive post is plated onto the fan-in RDL structure.

9. The method of claim 8, further comprising constructing a fan-out redistribution layer (RDL) structure on a surface of the mold compound, wherein the fan-out RDL is electrically coupled with the at least one conductive post.

10. The method of claim 6, further comprising applying a plurality of solder balls to the fan-out RDL structure to create a ball-grid array (BGA) package.

11. The method of claim 1, further comprising, after encapsulating the semiconductor die ~~unit~~ within the mold compound, separating the encapsulated semiconductor die unit from a plurality of other encapsulated semiconductor die units.

12. A semiconductor device package, comprising:

a semiconductor die unit;

a first redistribution layer (RDL) disposed over a surface of the semiconductor die unit and electrically coupled with one or more bond pads on an active first surface of the semiconductor die unit;

a plurality of conductive posts electrically coupled with the first RDL ~~one or more bond pads on an active surface of the semiconductor die unit~~; and

mold compound substantially covering the active first surface of the semiconductor die unit, wherein the plurality of conductive posts are electrically coupled by a second RDL ~~redistribution layer (RDL)~~ to conductive material exposed outside the mold compound, and wherein the conductive posts are disposed between the first RDL and second RDL.

13. The semiconductor device package of claim 12, wherein the second RDL ~~redistribution layer (RDL)~~ structure is a fan-out RDL and is electrically coupled with the plurality of conductive posts.

14. The semiconductor device package of claim 12, wherein the conductive material exposed outside the mold compound comprises a plurality of solder balls electrically coupled to the fan-out RDL structure, wherein the semiconductor device package is a ball-grid array (BGA) package.

15. The semiconductor device package of claim 12, wherein the first RDL further comprises ~~comprising~~ a fan-in RDL ~~redistribution layer (RDL)~~ connecting the one or more bond pads to the plurality of conductive posts.

16. A method, comprising:

providing a carrier;

constructing a spacer element coupled with an active surface of a semiconductor die unit;

disposing the semiconductor die unit face down on the carrier with the spacer element creating a gap between the active surface of the semiconductor die unit and the carrier; ~~device package by substantially encapsulating a semiconductor die unit within a mold compound; and~~

constructing a redistribution layer (RDL) structure coupled to the active surface of ~~electrically connecting bond pads of~~ the semiconductor die unit; and ~~to conductive material at an exterior surface of the semiconductor device package~~

encapsulating the semiconductor die unit within a mold compound after constructing the RDL, wherein the encapsulating comprises introducing the mold compound into the gap.

~~17. The method of claim 16, wherein encapsulating the semiconductor die unit within the mold component comprises:~~

~~creating a gap between the semiconductor die unit and a surface of a carrier supporting the semiconductor die unit; and~~

~~filling the gap with the mold compound.~~

~~18. The method of claim 16, further comprising:~~

~~constructing a plurality of conductive posts electrically coupled with the bond pads of the semiconductor die unit~~

~~attaching the conductive posts to a surface of a carrier, wherein the plurality of conductive posts are configured to maintain a gap between the semiconductor die unit and the surface of the carrier.~~

~~19~~17. The method of claim ~~18~~16, further comprising constructing the RDL as a fan-in RDL ~~redistribution layer (RDL)~~ structure ~~on a surface of the semiconductor die unit, wherein the fan-in RDL is configured to electrically couple the bond pads to the plurality of conductive posts~~.

~~20~~18. The method of claim 17 ~~18~~, further comprising forming a fan-out RDL over the fan-in RDL, after substantially encapsulating the semiconductor die unit within the mold compound~~, electrically coupling the RDL structure with the plurality of conductive posts, wherein the RDL structure is a fan-out RDL~~.