

APPARATUS FOR NOISE REDUCING COMPOSITE VIDEO SIGNAL

This invention relates to circuitry for performing noise reduction of video signals using recursive filtering techniques.

5 Recursive filter arrangements are known wherein incoming television signals are proportioned and added to weighted signals from previous frames of television signals that were proportioned in like manner. Recursive filtering may be performed on component video signals,
10 i.e. luminance and color difference signals, or chrominance or on composite video signals. If recursive filtering is performed on component signals, significantly more memory or storage devices is required over a system which recursively filters composite video signal.
15 However, if composite video is to be recursively filtered, e.g. using one frame of delay, the chrominance component of the composite video signal must be phase inverted since the chrominance component is 180° out of phase from frame-to-frame (NTSC). Heretofore, chrominance phase
20 inversion has required separation of the luminance and chrominance components, inversion of the chrominance component and recombination of the luminance and inverted chrominance component. It is an object of the present invention to provide simplified chrominance phase
25 inverting circuitry for composite video recursive filter systems.

The recursive filter of the present invention includes circuitry for proportioning and combining incoming signal and signal from delayed image segments
30 which has been previously processed by the proportioning and combining circuitry. A delay element is coupled to the output of the proportioning and combining circuitry to provide signal delays of substantially integral image intervals. Nearest neighbor signal samples delayed
35 slightly more or less than exactly one image interval, are

1 fed back from the delay element to the proportioning and combining circuit.

In the following description, for which video signals in NTSC format are assumed, reference is made to the accompanying drawings in which:

FIGURE 1 is a diagrammatic representation of interlaced video signals in three dimensions.

FIGURE 2 shows two dimensional arrays of a portion of signal samples from the successive frames of composite video and the superposition of samples from two successive fields of interlaced composite video signal.

FIGURES 3, 5, 6, and 7 are block diagrams of video recursive filters embodying the present invention.

FIGURE 4 is a logic diagram of comparison circuitry which may be substituted in the FIGURE 3 recursive filter.

FIGURE 8A is a block diagram of arbitration circuitry for selecting one of several signals for application in the recursion algorithm.

FIGURE 8B is a table of codewords used by the circuitry of FIGURE 8A.

The invention may be practiced on either analog or digital signals with the appropriate choice of hardware. The individual hardware elements, i.e. adders, scalers, memories, etc. are of conventional design. One assumption is made, and that is that the signal is in sampled data format for both analog and digital signals. The samples operated on are phase locked to the color subcarrier and, for convenience of the description that follows, taken at four times the subcarrier frequency. Samples are presumed to be taken along the I and Q color difference signal phase axes so that the samples occur in the sequence $(Y-Q)_{n-1}$, $(Y+I)_n$, $(Y+Q)_n$, $(Y-I)_n$, $(Y-Q)_n$, $(Y+I)_{n+1}$, etc. where Y represents the luminance component of composite video signal and I and Q represent the color difference contributions of the chrominance component of composite video and the subscripts denote successive cycles of the color subcarrier.

In the NTSC signal format the chrominance component is 180° out of phase line-to-line within a field and is also 180° out of phase from frame-to-frame.

Referring to FIGURE 1, portions of three fields of composite video signal are illustrated diagrammatically in a three dimensional representation. The x and y axes represent the video signals which contribute to the horizontal and vertical dimensions of a reproduced image. The t axis represents time or the field sequence of the displayed image. The lines parallel to the x axis and numbered $n+i$ represent horizontal lines of information as displayed. The + or - sign represents the relative phase of the color subcarrier for the particular line. Lines $n-3$ to $n+2$ correspond to a portion of the lines from field M-1 of frame J-1. Lines $n+522$ to $n+527$ are the corresponding horizontal lines in frame J. Frame J is the current frame and frame J-1 the immediately preceding frame. The dots on particular lines represent signal samples corresponding to picture elements (pixels). Successive samples along a particular line occur at 90° phase intervals relative to the color subcarrier. Points R, S, T, U and W in field M+1 correspond to the pixels R', S', T', U' and W' of field M-1 and are separated by one frame interval. The chrominance phase of points R, S, T, U and W are antiphase with points R', S', T', U' and W' respectively. The phase relationship is illustrated in FIGURE 2.

In FIGURE 2, samples from portions of three lines from frame J and corresponding samples from frame J-1 are shown. The samples each include a luminance component Y and a color difference component I or Q. The $\pm$ signs indicate the sampling phase and not signal polarity. The sampling phase of a +I (+Q) sample is 180° from the sampling phase of a -I (-Q) sample. In FIGURE 2, the exemplary samples R, S, T, U and W from frame J are circled and labelled. Similarly, the samples R', S', T', U' and W' from frame J-1 are circled and labelled. The

antiphase chrominance of corresponding pixels from frame-to-frame is evident.

Consider sample W. Conventional video recursive filters combine a fraction of sample W with a
5 complementary fraction of sample W' (assuming frame J-1 has been previously subjected to recursive filtering). Unless the chrominance phase (i.e. the I phase) of either sample W or W' is inverted, the I component will be partially cancelled. Thus, the necessity of a chrominance
10 inversion circuit.

Examining samples from frame J-1 in FIGURE 2 reveals that the samples R', S', T' and U' all contain the same chrominance phase as sample W from frame J. Any of these samples may be recursively combined with sample W
15 without requiring chrominance phase inversion. The question that immediately arises is, will such an arrangement produce a like response as the conventional composite video recursive filter. Experiments have shown the answer to be yes. The principles of video recursive
20 filtering for in-band noise reduction depend upon corresponding samples from successive frames representing the same or coherent image information, and that the noise introduced in the signal be random for corresponding samples. It is known that video signals contain a large
25 percentage of redundant information. Vertically aligned samples on successive lines will contain like information a large percentage of time. If the information in sample W' is the same as the information in sample W, then it is highly probable that the information of sample R' or T'
30 will be the same as sample W. Therefore, sample R' or T' can be substituted for sample W' without affecting the noise reducing performance of the recursive filter.

Similarly there is a high probability that the scene information in at least one of the samples U' or S'
35 will be the same as the scene information of sample W'. Thus, sample U' or S' may be substituted for sample W' in the recursion process without deleterious effect on the noise reduction.

One embodiment of this invention operates on these principles. Samples R' and T' and/or S' and U' are separately compared with sample W from the current frame. The sample R', T' and/or S', U' having an amplitude value closest to the amplitude value of sample W is used in the recursion process in place of sample W'. The apparatus to perform this function will be described hereinafter with reference to FIGURE 3.

A second embodiment of the invention utilizes similar principles but requires only one field of signal storage rather than a full frame. Refer to FIGURE 1 and in particular to the lines designated field M. In the drawing, line n+525 from field M+1 has been translated into field M in the position at which it is displayed. The pixel W on line n+525 is spatially displaced from pixels P and E on lines n+262 and n+263 respectively by half the spatial distance it is displaced from pixels R and T on lines n+524 and n+526 (or R' and T' on lines n-1 and n+1). Because of this lesser spacing it is more probable that pixels P and E contain similar information to pixel W than pixels R' and T'. In addition, because samples P and E are closer in time to pixel W than pixels R' and T', it is more probable that pixels P and E will have been subjected to less scene motion relative to pixel W than pixels R' and T'. Therefore, a recursive filter operating on field delayed signals, e.g. pixels P and E, should provide at least as good noise reduction properties as a frame recursive filter which utilizes frame delayed substitute pixels, e.g. R' and T'.

Experiments have shown that a field recursive filter which operates on samples delayed by one field plus one-half line, (263 lines for NTSC signal) does in fact provide significant noise reduction. Sample E cannot be used directly in this manner because it does not have the appropriate chrominance phase. This may be seen in FIGURE 2 in the sample array designated Field M plus Field M+1. This array is the superposition of portions of two successive fields as they would be displayed by interlaced

scanning. Alternate lines are from field M+1 and intervening lines from field M. Pixel P in line n+263 is seen to be vertically aligned and in phase with pixel W in line n+525. The closest samples in line n+262 which are in phase with sample W are samples C and G. In a further embodiment of the invention samples C and G are averaged together to provide a pixel for recursion. The averaged sample and sample P are both compared to the current sample W. The averaged sample or sample P having an amplitude most similar to sample W is used in the recursion process.

A still further embodiment generates a sample for recursion from samples D, E and F. Samples D and F are summed to substantially cancel the chrominance component. Note both samples are taken within one cycle of the color subcarrier, thus, the chrominance information in both samples must be substantially identical. Sample E is subtracted from the sum of samples D and F to yield the desired sample. This process is made clear by the following equations.

$$(Y-Q)_D + (Y+Q)_F = 2Y \quad (1)$$

$$2Y - (Y+I)_E = (Y-I) \quad (2)$$

The apparatus to perform these latter embodiments will be described hereinafter with reference to FIGURE 5.

One further embodiment is the combination of one or more of the latter described embodiments with the first mentioned embodiment. This embodiment is illustrated in FIGURE 6.

FIGURE 3 is a frame recursive filter circuit for practicing the first embodiment of the invention. In the figure, letters adjacent circuit connections correspond to signal samples designated in FIGURES 1 and 2. The FIGURES 3, 5 and 6 circuits are arranged to process NTSC signals. However, it will be appreciated by those skilled in the art that the invention is applicable to PAL signal processing with the appropriate selection of delay stages. For example, a PAL embodiment of the FIGURE 3 circuitry

requires two PAL frames of memory rather than a single NTSC frame of memory for NTSC signal processing.

Baseband composite video signal is applied to terminal 10, from, for example, the tuner-IF section of a television receiver. This signal (W) is coupled to one input of a known recursive filter signal/combining circuit 20. Delayed signal S_2 from multiplexer 33 is coupled to a second input of circuit 20. The output signal, OUT, from circuit 20 may be represented by the equation:

$$\text{OUT} = KW + (1-K)S_2$$

where K is a scaling factor and W and S_2 are the amplitudes of the input signal W and the delayed signal S_2 respectively. A detailed description of this circuitry may be found in U.S. Patent No. 4,240,106. Circuitry 20 also includes optional motion detection circuitry 24 which changes the value of the scaling factor K as a function of the difference in magnitudes of signals W and S_2 .

The output signal from circuit 20 is coupled to the input of delay element 26. Delay element 26 delays the signal, OUT, by one video frame interval less one line interval and less a small interval τ_1 . The delay interval τ_1 is equal to the delay incurred by delayed signal S_2 in coursing through multiplexer 33 and scaling/combining circuit 20. In other words, element 26 is selected to provide a signal delay, such that signal T' coupled from the output of delay element 26 to the point S_2 , via multiplexer 33, will be delayed by exactly one frame less one horizontal line interval with respect to input signal W.

The output from delay element 26 is coupled to a tapped delay line 28. Line 28 consists of the cascade connection of delay elements 30, 31 and 32. Delay element 30 provides a delay interval of one horizontal line less two sample periods. Delay element 31 provides a delay interval of four sample periods and delay element 32 provides a delay interval of one horizontal line period less two sample periods. The total delay interval provided by the tapped delay line 28 is two horizontal

line intervals. The signal available at the output of delay element 26 (and input of delay element 28) corresponds to the sample T' illustrated in FIGURES 1 and 2. The sample R' which occurred exactly two horizontal lines before sample T' is concurrently available at the output of delay element 32. The sample S' which occurred one horizontal line less two sample periods before sample T' is concurrently available at the output of delay element 30, and sample U' which occurred four sample periods before sample S' is concurrently available at the output of delay element 31.

Samples R' and T' and, if desired, samples S' and U' are coupled to respective signal input terminals of multiplexer 33. Multiplexer 33 responsive to a control signal from comparator circuit 34 selectively applies one of samples R' and T' (or samples R', T', S' and U') as signal S_2 to the scaling/combining circuit 20.

Delayed samples R', T', S', U' and input samples W are applied to respective input terminals of comparator circuit 34. Circuit 34 compares each of the delayed samples R', T', S', U' to the input samples W to determine which of the delayed samples has the amplitude value closest to the amplitude value of sample W. Responsive to this determination, comparator circuit 34 develops the control signal that is applied to multiplexer 33.

FIGURE 4 is exemplary comparator circuitry 34' which may be used in a binary signal implementation of the recursive filter of FIGURE 3. The samples are presumed to be in parallel-bit two's complement format. Comparator circuit 34' includes two subtracter circuits 40 and 41 to which input samples W are applied as minuends. Samples T' and R' are applied as subtrahends to subtracters 40 and 41 respectively. The output of subtracter 40 is the difference (W-T') and the output of subtracter 41 is the difference (W-R'). The output of subtracter 40 is applied to a magnitude detector 42 and the output of subtracter 41 is applied to a magnitude detector 43. Magnitude detectors 42 and 43 are exclusive OR gate circuits which

are responsive to the respective sign bits of the differences to one's complement the negative difference values. This causes all of the sample differences from both subtracters 40 and 41 to have a single polarity.

5 (For greater accuracy it may be desirable to substitute the polarity selective one's complementing exclusive OR circuits 42 and 43 with polarity selective two's complementing circuits.)

10 The outputs of exclusive OR's 42 and 43 are coupled to subtracter 44 as minuend and subtrahend input signals. Only the sign bit is required from subtracter 44 if the system is only to use either sample R' or T'. The output of exclusive OR circuits 42 and 43 are $|W-T'|$ and $|W-R'|$ respectively. The output of subtracter 44 is
15 $|W-T'| - |W-R'|$. If $|W-T'|$ is greater than $|W-R'|$ the difference is positive and the subtracter sign bit is a zero. Thus, a zero sign bit output is indicative of the amplitude of sample R' being closer to the amplitude of W. Conversely, a "one" sign bit output indicates that sample
20 T' has the amplitude closer to sample W. In this example, the sign bit output from subtracter 44 is the control signal.

If it is desired to select between, e.g., the four samples R', T', U' and S' on a similar basis, the
25 circuit of FIGURE 4 can readily be expanded to accommodate the four samples.

FIGURE 5 illustrates field composite video recursive filter circuitry including at least four delayed signal feedback options. In FIGURE 5, incoming baseband
30 composite video signal applied at terminal 10 is coupled to one input of a known signal scaling/combining circuit 20'. Delayed signal S_3 from multiplexer 69 is coupled to a second input of circuit 20', which develops an output signal (OUT) given by:

35
$$OUT = (1-K)W + KS_3$$

where K is a scaling factor and W and S_3 are the amplitudes of the incoming and delayed signals respectively. A detailed description of this signal

scaling/combining circuit 20' may be found in U.S. Patent No. 4,240,106. Circuit 20' also includes an optional motion detector 53 for varying the scale factor K as a function of the amplitude differences between signals W and S₃.

The output signal OUT is applied to the input terminal of delay element 55. Delay element 55 delays signal applied thereto by one field interval less one-half of one horizontal line (i.e. 262 lines for NTSC) and less a small delay interval τ_C . The delay interval τ_C compensates for the processing delays of circuit 20' and multiplexer 69. In other words, the delay period provided by delay element 55 is selected so that signal coupled from the output of delay element 55 to the second input of circuit 20' via multiplexer 69 is delayed by exactly one field less ^{one half of} one horizontal line period relative to the incoming sample W with which it is combined in circuit 20'.

The output of delay element 55 is coupled to the input of circuitry 60 which provides several alternative delayed signals to multiplexer 69. Circuitry 60 consists of a tapped delay line including the cascade connection of delay elements 61-65, and signal combining means 67 and 66. Delay element 61 provides a signal delay interval of one horizontal line interval less two sample periods. Delay elements 62-65 each provide a signal delay interval of one sample period. The respective outputs of delay element 55 and delay elements 61-65 concurrently provide samples corresponding to samples P, G, F, E, D and C illustrated in FIGURES 1 and 2.

In a first optional embodiment, signal P from the output of delay element 55 may be coupled continuously to the signal scaling/combining circuitry 20'.

In a second optional embodiment, signal samples G and C from the outputs of delay elements 61 and 65 are summed in combining circuit 67. The output signal from combining circuit 67 is applied to a divide-by-two circuit 68 which develops a signal corresponding to the average of

signals G and C. In this option, the signal from divide-by-two circuit 68 is applied continuously to the second input of signal scaling/combining circuit 20'.

5 In a third optional embodiment, signals F, E and D are applied to combining circuit 66 which develops the signal $(D+F-E)$. In this option the signal from the output of combining circuit 66 is applied continuously to the second input of signal scaling/combining circuit 20'.

10 In a fourth and preferred optional embodiment, signal P from the output of delay element 55 and the signal $(D+F-E)$ from combining circuit 66 are selectively coupled to the second input of signal scaling/combining circuit 20' by multiplexer 69. Signals P and $(D+F-E)$ are applied to signal input terminals of multiplexer 69 and to
15 input terminals of comparator circuit 70. Incoming signal from input terminal 10 is also applied to comparator circuit 70. Responsive to the signals P, $(D+F-E)$ and W, comparator circuit 70 develops a control signal which indicates which signal, P or $(D+F-E)$ has an amplitude
20 closer to the amplitude of signal W. This control signal is coupled to the control input C of multiplexer 69 to couple the appropriate signal to circuit 20'.

In a further embodiment, the three signals P, $(D+F-E)$ and the average of G and C are tested in
25 comparator circuit 70 and selectively coupled to circuit 20' by multiplexer 69 according to which signal has an amplitude closest to the amplitude of signal W.

FIGURE 6 illustrates circuitry which combines the embodiments of FIGURES 3 and 5. In the figure,
30 incoming baseband composite video signal applied at input terminal 10 is coupled to a signal scaling/combining circuit 20" which may be similar to circuit 20 or circuit 20'. The output of circuit 20" is coupled to a delay element 55 similar to the delay element 55 in FIGURE 5.
35 The output of delay element 55 is coupled to circuitry 60' which may be similar to circuitry 60 of FIGURE 5. Circuit 60' provides output signals P, $(D+F-E)$ and $(G+C)/2$, which are applied to respective signal input terminals of

5 multiplexer 84 and to respective input terminals of comparator circuit 82. Output signal from delay element 55 is also applied to the input terminal of a delay element 80 which delays signal by one field interval less one-half of one horizontal line period. The total signal delay provided by the cascade connection of delay elements 55 and 80 is equal to the delay provided by delay element 26 in FIGURE 3.

10 The output of delay element 80 is coupled to a tapped delay line 28' which may be similar to the tapped delay line 28 in FIGURE 3. Tapped delay line 28' provides the output signals R', U', S' and T' which are coupled to respective signal input terminals of multiplexer 84 and to respective input terminals of comparator 82. The input
15 signal, W, is also coupled to a signal input terminal of comparator 82 which develops a control signal indicative of which of the signals applied to its input has an amplitude closest to the amplitude of the input signal W. Responsive to the control signal, multiplexer 84
20 selectively couples the appropriate delayed signal to a second input terminal of signal scaling/combining circuit 20" for recursion.

In FIGURE 6, all of the discussed signals are shown coupled to the multiplexer 84 and comparator circuit
25 82. It should be understood, however, that in a particular application, less than all of the illustrated signals may be coupled to the multiplexer.

Image changes occur wherein the differences between the alternate delayed signals and the current
30 signal are all relatively large. Under these conditions, feeding back any of the alternate samples may deleteriously affect the resulting image. In addition, it has been determined that if the signal conditions are such that a particular signal (such as the frame delayed
35 signals T' or R') is repeatedly selected for recursion, subdued undesirable comet tails are introduced into the image. These artifacts give the appearance of correlated noise. The latter effect may be cured by requiring that

each of the alternate signals used for recursion be developed from samples substantially symmetrically disposed spatially about the corresponding delayed picture point. Desirably, the symmetry should be in both the horizontal and vertical dimensions. However, substantial vertical symmetry is the more important condition. The former problem is improved by providing a further alternate signal for recursion which is developed from the current image field.

Refer to FIGURES 1 and 2. Let the picture points between U' and W' and between W' and S' be designated X' and Y' respectively. Similarly designate the corresponding picture points between U, W and S in frame J, as X and Y. The picture points R, U, X, Y, S and T of the current frame J correspond to samples (Y+I), (Y+I), (Y+Q), (Y-Q), (Y+I) and (Y+I) respectively. Summing the X and Y samples, i.e. (Y+Q) and (Y-Q) produces a luminance sample of twice amplitude (2Y) assuming the magnitudes of the $\pm Q$ component are equal. Summing the samples corresponding to points R, S, T and U yields $4(Y+I)$. If this value is divided by four and subtracted from the sum of signals from points X and Y the result is (Y-I). The amplitude of the luminance component of the result tends toward the weighted mean of the amplitudes of the luminance component of the six samples, and the phase of the chrominance component tends to correspond to the phase of the chrominance component of the current sample, W. The signal

$$F1 = (X+Y-\frac{1}{4}(R+S+U+T)) \quad (3)$$

where X, Y, R, S, U and T correspond to the values of the designated samples, being produced from samples from the same field and which are symmetrically disposed about the current sample W, will have a magnitude similar to sample W, and thus is suitable for use in the recursion algorithm when the amplitudes of the alternate frame and field signals diverge significantly from the amplitude of the current sample. Unfortunately, averaging over five samples in the horizontal direction tends to limit

horizontal bandwidth. Therefore, signal F1 is employed in the recursion algorithm on a relatively limited basis. For example, if signal F1 is made available as one of the alternate recursion signals in the FIGURE 3 apparatus, i.e. F1 is coupled to multiplexer 33 and comparator circuit 34, the difference (W-F1) developed for arbitrating between the respective alternate signals may be weighted to favor the other alternate signals.

The condition of substantial vertical symmetry of the delayed signals may be realized by developing the alternate recursion signals from a number of samples. For example, a field delayed recursion signal may be developed from samples D, E, F and P which form a triangle about sample W. This signal, F2, may be derived from

$$F2 = (P+D+F-E)/2 \quad (4)$$

where P, D, E and F are the amplitude values of samples P, D, E and F.

A frame delayed recursion signal, F3, may be derived from samples W', X' and Y', i.e.

$$F3 = X'+Y'-W' \quad (5)$$

where X', Y' and W' are the amplitude values of samples X', Y' and W' respectively. The signal F3 is vertically symmetric about point W' since each of the contributing samples are from the same line as point W' and disposed horizontally thereabout. An alternate frame delayed signal may be derived by averaging points R' and T'.

From FIGURE 2

$$F2 = [(Y-I)+(Y-Q)+(Y+Q)-(Y+I)]/2 = (Y-I) \quad (6)$$

$$\text{and } F3 = (Y-Q)+(Y+Q)-(Y+I) = (Y-I). \quad (7)$$

It can be seen from equations (6) and (7) that the chrominance components of both of the signals F2 and F3 are of like phase as the current sample W and thus are suitable for recursion.

Circuitry to incorporate these features in a composite video signal recursive filter is illustrated in FIGURE 7. In FIGURE 7, incoming composite video signal 100 is applied to a delay element 102 having output taps for providing delayed signals S, Y, W, X, U and R. The

incoming signal, which, relative to the tapped output signals corresponds to signal T, and the signals S, Y, X, U and R are coupled to the arithmetic circuit 104.

Arithmetic circuit 104 combines the signals applied thereto to develop signal F1 according to equation (3).

The tapped output signal W is coupled to one input terminal of circuit element 20" which may be similar to circuits 20 and 20' in FIGURES 3 and 5 respectively. Circuit 20" scales and combines signal W and the selected recursion signal in predetermined proportions to produce a noise reduced composite video signal. The output of circuit 20" is coupled to the delay element 106 which provides, at respective taps, the field delayed signals P, F, E and D. These field delayed signals are coupled to respective input terminals of the arithmetic circuit 112,. Circuit 112 combines the signals P, F, E and D to form signal F2 according to equation (4).

The delayed signal D is also coupled to a further delay element 114. Delay element 114 delays signals by approximately a further field period to provide the frame delayed signals X', Y' and W' at respective output taps. The signals X', Y' and W' are coupled to the arithmetic circuit 116 which combines these signals to form signal F3 according to equation (5).

The signals F1, F2 and F3 produced by arithmetic circuits 104, 112 and 116 are coupled to the multiplexer 108 and to the control circuit 110. In addition, the signal W from delay element 102 is coupled to the control circuit 110. Control element 110 develops a control signal that is coupled to multiplexer 108 and controls which of signals F1, F2 and F3 are applied to circuit 20".

Control circuit 110 may be similar to the comparator circuit 34 described with reference to FIGURE 3. Generally control circuit 110 should tend to favor signal F3 over signals F2 and F1, and signal F2 over signal F1 because the order of most-to-least signal correlation with the current signal W (at least for still pictures) and because the order of widest to narrowest

bandwidth recursion signals is F3, F2, F1. This priority may be achieved by weighting the signal differences $|W-F_i|$ before making the comparisons. While the three signals F1, F2 and F3 tend to be the preferred signals used for recursion, others of the signals illustrated with reference to FIGURES 3, 5 and 6 may also be utilized in the arbitration and feedback process of the FIGURE 7 apparatus.

FIGURE 8A shows an example of alternate circuitry which may be implemented for the multiplexer 108 and control circuit 110 of FIGURE 7. In FIGURE 8A the three recursion signals F1, F2 and F3 from arithmetic circuits 104, 112 and 116 are coupled to respective scaling circuits 121-123. The scaled output signals from the scaling circuits 121-123 are coupled to the summing circuit 130 which develops the recursion signal to be applied to the recursion circuitry 20".

Signals F1, F2 and F3 are multiplied by the factors α_1 , α_2 and α_3 respectively in scaling circuits 121-123. The recursion signal, RS, developed by summing circuit 130 is given by

$$RS = \alpha_1 F_1 + \alpha_2 F_2 + \alpha_3 F_3 \quad (8)$$

where $\alpha_1 + \alpha_2 + \alpha_3 = 1 \text{ or } 0. \quad (9)$

Typically, two of the three scale factors will be zero and the third will be one. However, there are instances when it may be desirable to force all three scale factors to zero, and instances where at least two of the signals F1-F3 are proportioned to form the recursion signal.

In FIGURE 8A, the scale factors α_1 - α_3 are generated as follows. The signals F1-F3 and signal W are applied to the differencing circuit 124 which produces three output signals corresponding to the absolute values of $(W-F_1)$, $(W-F_2)$ and $(W-F_3)$. These three signals are coupled to a second differencing circuit 126.

Differencing circuit 126 develops three output signals corresponding to the polarity of the difference between a predetermined value, TH, and each of the signals $|W-F_1|$, $|W-F_2|$ and $|W-F_3|$ applied to its input. The convention

used is that if the input signal exceeds the predetermined value TH, the polarity indication is a logic 1, otherwise it is a logic zero. The polarity or sign signals are coupled to the input terminals of a decoder 128 which produces the scale factors α_1 - α_3 .

Decoder 128 may be a read only memory (ROM) programmed with respective scale factors corresponding to all possible combinations of the polarity input signals. One exemplary scale factor-input signal correspondence is illustrated in the table of FIGURE 8B. The columns sgn F1, sgn F2 and sgn F3 represent the three polarity signals. The zeroes in these columns indicate that the difference between the respective signals W and Fi are acceptably small for the particular signal Fi to be coupled to the feedback input of circuit 20". If both signals F2 and F3 are acceptable, portions of both are utilized by programming α_1 , α_2 and α_3 to be 0, 1/4 and 3/4 respectively (rows 1 and 5 in FIGURE 8B). In all other instances, only one of the three signals F1-F3 is utilized except when all of the signals F1-F3 are unacceptable (bottom row). Note that if signal F1 and one of the other signals F2 and F3 are concurrently acceptable, i.e. sgn (Fi)=0, the other signals F2 and F3 are selected over signal F1.

Normally, recursive filtering tends to reduce the bandwidth of signals representing edges of moving objects in the reproduced scene and introduces phantom images. To reduce these undesirable features, the scaling/combining circuitry is arranged to be motion adaptive. The motion adaptive circuitry changes the scaling factors K for pixels containing moving edges so that a lesser percentage of delayed signal is combined with the current or incoming signal. This in turn tends to substantially reduce the noise reduction function of the system in the areas containing moving edges. Thus, the areas of the reproduced images adjacent to the edges of moving objects tend to be noisier than the non-moving parts of the reproduced scene.

The recursive filters described herein tend to reduce the number of occurrences that the motion adaptive scaling/combining means is activated to reduce the percentage of the delayed signal that is combined with incoming signal. This is so because the comparator chooses the delayed signal which is most like the incoming signal. The overall effect is that the reproduced images have fewer artifacts and less noise in areas of moving edges.

The circuitry illustrated has been selected to most lucidly describe the invention. It should be appreciated by those skilled in the art of circuitry design, however, that it may be necessary to interpose e.g. compensating delays at various points in the circuit, and that persons skilled in the art will readily be able to include such delays.

In the claims, the term "image period" is defined as the time interval of one field of video information or one frame of video information. A delay of "substantially one image period" is intended to include a range of delay intervals from an image period plus approximately one-half of one horizontal line period to an image period less approximately one-half of one horizontal line period for field recursive filter apparatus, and a range of delay intervals from an image period plus approximately one horizontal line period to an image period less approximately one horizontal line period for frame recursive filter apparatus. A sample period corresponds to one-quarter of one cycle of the color subcarrier frequency or integral cycles plus one-quarter cycle of the color subcarrier frequency.



CLAIMS:

1. A recursive filter for processing sampled data composite video signal, including a terminal for applying said composite video signal, scaling/combining means for combining incoming sampled data composite video signal from said terminal and delayed sampled data composite video signal in predetermined proportion, and means including delay means, coupled to an output port of said scaling/combining means for providing said delayed sampled data composite video signal, said signal providing means including means for providing a plurality of delayed signals each of which is delayed by substantially at least one image period with respect to said incoming sampled data composite video signal with each of said plurality of delayed signals containing a chrominance component substantially in phase with said incoming sampled data composite video signal, and means coupled to said signal providing means for arbitrating between said plurality of delayed signals and selectively coupling one of said plurality of delayed signals to said scaling/combining means.

2. The recursive filter set forth in Claim 1 wherein said means for providing said delayed signals includes means for providing samples representing picture points which are disposed about a picture point corresponding to a picture point currently represented by the incoming sampled data composite video signal; and means for combining ones of said samples for producing signals having a chrominance component in phase with the chrominance component of the incoming sampled data composite video signal.



3. The recursive filter set forth in Claim 1 wherein said plurality of signals includes signals derived from signals delayed by substantially one field interval and signals delayed by substantially one frame interval relative to said incoming composite video signal.

4. The recursive filter set forth in Claim 1 further including:

means, coupled to said terminal for applying composite video signal, for providing a plurality of composite video signals all of which represent picture points from the same field as the picture point represented by the composite video signal applied to said terminal, ones of which occur advanced in time with respect to composite video signal applied to said terminal and ones of which are delayed in time with respect to the composite video signal applied to said terminal;

means, coupled to said means for providing said plurality of composite video signals, for producing a combined signal having a chrominance component of like phase as a chrominance component of the composite video signal applied to said terminal;

means for coupling said combined signal to said means for selectively coupling and wherein said means for selectively coupling couples one of said plurality of delayed signals or said combined signal to said scaling/combining means.

5. The recursive filter set forth in Claim 1, including:

means, coupled to said means for providing a plurality of delayed signals, for producing at least two signals having a like chrominance phase as a chrominance



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component of composite video signal applied to said terminal, wherein at least one of said two signals is formed by combining ones of said plurality of delayed signals.

6. Recursive composite video signal filtering apparatus substantially in accordance with any of the alternatives hereinbefore described with reference to the accompanying drawings.
