"IMPROVEMENTS IN OR RELATING TO ELECTRONIC TIMEPIECES"

This invention relates to electronic timepieces and more specifically to electronic timepieces in which a reactance element, usually a capacitor, is connected to a piezo-electric (quartz) crystal oscillator through the intermediary of a switch in order that the time-keeping rate of the timepiece can be adjusted by opening and closing said switch to switch the reactance in and out of the oscillator circuit.

The invention is illustrated in and explained in connection with the accompanying drawings, in which:-

Figure 1 is a block diagram of one form of electronic timepiece embodying the invention;

Figure 2 is an explanatory figure illustrative of a known method of time keeping rate adjustment by reactance variation;

Figures 3(a) and (b) and Figure 4 illustrate typical temperature characteristics obtained with a quartz crystal;

Figure 5 is a circuit diagram of the embodiment of the invention illustrated in block diagram form in Figure 1;

Figure 6 is a timing chart showing signals occurring in the circuit of Figure 5; and

Figure 7 is a block diagram of another embodiment of this invention.

In the figures, wherever they occur, reference 1 is a quartz crystal oscillator; 2 is a reactance element (normally a capacitor incorporated in an integrated circuit (IC)); 3 is a switch (electronic); 4 is a frequency divider; 6 is a rate adjusting step width determining circuit; 7 is a rate adjusting amount determining circuit; and 8 is a controller circuit. These various items of circuitry will be understood from more detailed description to be given later herein.

Various provisions for adjusting the rate of a quartz timepiece are known. For example in one known type of arrangement a trimmer capacitor is included in the crystal oscillator circuit system so that the oscillation frequency can be varied (and the rate thus adjusted) by increasing or decreasing the reactance of the capacitor. In another known arrangement what is in effect a digital tuning method is employed; a variable ratio divider is provided at a stage following the crystal oscillator circuit and the divider ratio is adjusted digitally in order to adjust the rate of the timepiece.

In recent years there has arisen a demand for timepieces, and especially small timepieces such as wrist watches, which are of very high time-keeping precision and, despite this, are also very reliable and easy to adjust in rate. The two

known methods of rate adjustment just briefly described are insufficiently precise and reliable to enable this demand to be satisfied and, accordingly, a third method, illustrated by Figure 2 of the accompanying drawings has deen developed. Referring to Figure 2, a capacitor 2, provided for effecting frequency variation, is connected to a time-base quartz crystal oscillator 1 (X is the piezo-electric crystal therein) through an electronic switch (a transistor) 3, and the oscillation frequency is varied by opening and closing this switch by a control signal applied thereto. In this way the time-keeping rate is adjusted until the required precise accuracy of time-keeping is achieved. This method of rate adjustment, which will be found more fully described in U.S. Patents Nos. 3,568,093 and 4,473,303 has the advantage that the precise rate adjustment can be effected in a very short time. If this method is used in combination with the digital tuning method mentioned above, precise rate adjustment can be achieved over a relatively wide range of ambient temperature.

However, the arrangement illustrated by the accompanying Figure 2 has serious defects of its own. Because the capacitance of the capacitor 2 is small and the said capacitor 2 is, in practice, usually incorporated with the switch 3 in an integrated circuit (I.C.) and because, also, due to inevitable variations in manufacture, different individual capacitors 2 will, when manufactured, be of

different reactance values, the difference between the oscillation frequency when the capacitor 2 is connected to the oscillator 1 and the oscillation frequency when the said capacitor 2 is disconnected will differ from one timepiece to another. Accordingly, even if the timing at which the switch 3 is controlled is such as to give an equal adjustment rate in all the timepieces in a batch, the amount to be adjusted differs for different individual timepieces in the batch and this makes time-keeping rate adjustment troublesome and difficult. This is especially the case when rate adjustment is required to be effected in timepieces which have been distributed from a manufacturer to retailers and need to be rate adjusted because of the effect of ageing when in the hands of retailers. The retailer will, therefore, find it very difficult to effect precise rate adjustment before sale of the watches he has in stock from a manufacturer.

Unless a statement of the data for time-keeping rate adjustment is attached to or otherwise provided with each individual timepiece (and it is obviously expensive to the point of commercial impracticability to do this) the retailer will not know to what extent the rate of each individual timepiece is adjusted by the method of adjustment he generally uses and accordingly, if he is to achieve precise adjustment he has no option but to effect adjustment gradually, a little at a time, and, at each step of adjustment, check the

rate of the timepiece being adjusted against that of a rate measuring device. This makes rate adjustment a slow and troublesome matter taking a great deal of time.

The foregoing will be further explained with reference to Figures 3(a) and (b).

Figure 3 shows temperature characteristics of the rate (ordinates) against temperature (t) (abscissae) of an oscillator including a quartz crystal having binary frequency-temperature characteristics. Figures 3(a) and 3(b) respectively show the temperature characteristics for a case when the capacitance of the capacitor 2 (Figure 2) is relatively small and the case when it is relatively large. (As already explained such differences in capacitance inevitably arise between individual capacitors due to unavoidable small variationsin normal mass production manufacture). Figures 3(a) and 3(b) are drawn for quartz crystals of the same characteristic. fo (t) shows the characteristic when the switch 3 is open; f_1 (t) and f_2 (t) show the characteristic when the switch 3 is closed; and Δf_1 and Δf_2 show the frequency duration between the frequency when the switch 3 is open and the frequency when said switch is closed. Δf is generally substantially constant over the whole temperature range. Now consider the peak points of the temperature curves and assume that rate adjustment is to be effected by dividing

Δf into four adjusting steps. As will be seen the adjusting amount of one step will be different for the two individual timepieces with characteristics as shown in Figures 3(a) and 3(b), the adjusting amount of one step in Figure 3(b) being twice that achieved by the same step in Figure 3(a),

Figure 3 thus clearly shows how it is that manufacturing differences of capacitance between individual capacitors 2 cause the adjusting amount of one step of rate adjustment to differ between individual timepieces, thus preventing a person engaged in rate adjustment from knowing how many steps are required, in any individual timepiece, to achieve precisely accurate time-keeping. This is a very serious practical defect. The present invention seeks to avoid this defect and to provide rate adjustment in which, despite differences in the capacitances of different individual capacitors intended to be of the same value, the amount of adjustment achieved by an adjusting step does not materially differ from one individual timepiece of a batch to another and in which rate adjustment can be achieved.

According to this invention in one aspect an electronic timepiece comprises frequency dividing means for producing a reference signal determining the resolution of rate adjustment; rate adjusting step width determining means for determining the rate adjusting width achieved by one step of

adjustment; rate adjusting amount determining means for determining the rate adjusting amount; and control means for controlling the time ratio of connection of a frequency adjusting reactance element in a time standard piezo-electric oscillator of the timepiece.

According to this invention in another aspect an electronic timepiece includes a time-standard piezo-electric crystal oscillator the frequency of which is variable to effect time-keeping rate adjustment by switch means switching in and out of the oscillator circuit; frequency dividing means for dividing the oscillator output frequency to produce time standard signals for time-keeping operation of the timepiece and time standard signals for determining the resolution of rate adjustment; rate adjustment step width determining means for determining the rate adjustment step width (amount of adjustment per step) required to accord with the determined resolution; rate adjustment amount determining means for determining the required rate adjusting amount in accordance with the rate adjustment step width; and control means controlling the operation of the switching means under the control of time standard signals and output signals from said rate adjustment amount determining means, the whole arrangement being such that, irrespective of the actual value within a relatively wide range of possible values of the reactance switched in and out, the amount of rate

adjustment per step of adjustment remains substantially constant at a known predetermined selected value.

In carrying out this invention, Δf is properly divided by the resolution determined by the divider means; the rate adjusting step width determining means determines the rate adjusting width of one step to be always constant by combining some of the divisions of Δf, while the rate adjusting amount determining means determines the timing for the switching of the switch 3 with respect to every single step determined as above. Accordingly, with rate adjustment effected in this manner, the rate adjusting width of one step is maintained substantially constant regardless of the capacitance of the capacitor 2 and rate adjustment is made precise, easy and quick to achieve.

Figure 1 is a block diagram of one embodiment of this invention.

In Figure 1, there is a time standard quartz oscillator 1, the oscillation frequency of which can be varied by opening and closing an electronic switch 3 connected to the oscillator through the intermediary of a capacitor 2. 4 is a frequency divider which divides the output of the quartz crystal vibrator 1 and produces a standard time signal Fo for driving the rest of the watch circuitry and mechanism (represented simply by the block 5; it may take any well known form). F_1 and F_2 are frequencies taken from the divider and used for determining the resolution and the synchronization

respectively of rate adjustment. The rate adjusting step width determining circuit is represented by the block 6 and produces a signal $F_3(\alpha)$ representing the rate adjusting amount (i.e. rate adjusting width) produced by one step. As will be better understood later, the circuit 6 uses the signals F_1 and F_2 to produce a co-efficient α of adjustment per step of adjustment, the total adjustment width being determined by the application of signals to the selecting signal input terminals L1 to Ln. The rate adjusting amount determining circuit 7 produces a signal F4(P) representative of the total rate adjusting amount to be achieved, using the rate adjusting step width of one step as determined by the circuit 6, the standard signal F1 and the value (P) defining the total adjusting amount determined by the selecting signal input terminals Ln+1 to LN of circuitry. 8 is a control circuit producing a timing signal F5 for controlling opening and closing of the electronic switch 3 and utilises the signal F1 for determining synchronization and the signal F4(P) representing the total rate adjusting amount, and accordingly effecting rate adjustment by varying the oscillation frequency of the quartz crystal vibrator 1.

Figure 4 will assist in an understanding of the way in which the improved performance of the timepiece of Figure 1 is obtained.

Figure 4, like Figure 3, illsutrates the temperature

characteristic of a typical quartz crystal vibrator. In Figure 4, d is the resolution as determined by the reference signals F1 and F2 and the frequency deviation Δf. F1 is the signal for determining the adjusting frequency and F2 is the signal for determining the minimum unit time for switching the capacitor 2. We may write, for d, the equation

$$d = \Delta f, \frac{F_2^{-1}}{F_1^{-1}}$$

where F1 and F2 are the above-mentioned frequencies, $F_1^{-1}=1/F$ and $F_2^{-1} = 1/F_2$. S is the rate adjusting width of one step and is equal to αd. The rate adjusting amount determining circuit 6 performs the calculation $S=\alpha d$. The value of d will vary with fluctuation of Δf but S is caused to remain the same and not differ from one individual watch to another by adjusting the value of the coefficient α.

Since, owing to manufacturing variations between individual capacitors 2, the value of Δ_5 cannot be predetermined but will differ arbitrarily from watch to watch of the same line of manufacture, it is necessary, in the interests of achieving high time-keeping accuracy by precise rate adjustment, to choose the resolution d sufficiently small to enable the requirement for the rate adjusting width S to be achieved by adjusting the value of γ. Thus, if in mass production manufacture Δf is measured for a number of watches of a line and, in the light of the information thus obtained, the value of d is

suitably chosen to allow any desired value of rate adjustment likely to arise in adjusting the step width determining circuit 6 of the practice to be achieved, the rate adjusting width S of one step of adjustment will in effect be the same for all the individual watches despite differences of the value of capacitance of the capacitor 2 from one watch to another. As a result, the retailer will have no difficulty in effecting accurate rate adjustment of individual watches quickly and easily and can easily know how many steps of adjustment are necessary to adjust any individual timepiece.

Assuming that L in Figure 4 is the adjusting amount required in any particular case and P is the number of steps satisfying the equation $L = PS$, the number P is set into the rate adjusting amount determining circuit 7 which performs the calculation according to the predetermined vlaue of P to determine the total adjusting amount required. Accordingly, by informing retailers of the predetermined value of P they can easily and speedily complete rate adjustment.

The control circuit 8 in Figure 1 produces the actual rate adjusting signal F5 from the timing signal F1 received from divider 4 and F4(P) as determined by the calculation made by the rate adjusting amount determining circuit 7.

Figure 5 shows in some circuit detail the watch illustrated in block form by Figure 1 and Figure 6 is a timing chart shown occurring in Figure 5.

In Figure 5 the parts 1 to 5 inclusive correspond respectively with the similarly referenced parts in Figure 1 and blocks 6, 7 and 8 correspond respectively with the similarly referenced blocks in Figure 1. The blocks 9 are stages of a binary counter with reset terminals R and $\overline{R}$ and clock input terminals cL and Q output terminals and 10 is a coincidence detector circuit. LI to L5 are the rate adjusting step width determining terminals and L6 to L9 are the rate adjusting amount determining terminals. The wave forms in Figure 6 occur at points with corresponding references in Figure 5.

In Figure 5, the binary counter 9, the coincidence detector circuit 10 and the rate ajdusting step width and the rate adjusting amount determining terminals Ln together constitute a variable division ratio divider circuit, the ratio of which is determined in dependence upon which of the L terminals receives an input signal.

In the circuit of Figure 5, the resolution d is given by the equation:-

$$d = \Delta f. \frac{\frac{1}{\emptyset 256}}{\frac{1}{\emptyset\ 0.5}}$$

and accordingly, the frequency deviation Δf is divided into 512 parts. When Δf=0.205 sec/day, d=0.0004 sec/day. If the rate adjusting step width S of one step for a rate adjustment of the desired precision is 0.008 sec/day, α=20 (one twentieth of 0.008=0.0004), d is expressed as

$\frac{1}{\emptyset 256}$ in α = 2 sec (that is, the adjusting amount $\underline{d}$ is obtained if the switch 3 is closed for a period of $\frac{1}{\emptyset 256}$ sec in 2 sec). So, given that the signal representing the rate adjusting width S is F3(α), we may write:-

$$\frac{1}{F_{13}(20)} = 20 \cdot \frac{1}{\emptyset 256}$$

Converting this into frequency, we obtain:-

$$F3(20) = \frac{1}{20} \cdot \emptyset 256,$$

and thus F3(20) is obtained by dividing Ø256 by 20.

If α = 20 is set by binary codes in the rate adjusting step width determining circuit 6, the circuit 6 acts as a vicenary (twientieth) counter, thereby presenting a desired value of F3(20). Therefore, even if the frequency deviation Δf differs from one watch to another due to differences between the capacitances of different capacitors 2 and consequently α varies, by determining α, a desired value of F3(α) can be obtained.

If α is not an integer, decimal fractions can be discarded or α raised to the next integer above the decimal point. However, if error caused by such rounding off or rounding up is too large in a particular case to be ignored, having regard to the precision required in

that case, the resolution d can be raised until the error becomes tolerable (to increase the difference between F1 and F2) and the "bit" number of the rate adjusting step width determining circuit 6 increased in correspondence with the increased value of the resolution d.

As will now be appreciated, by previously determining α by calculation and setting it in the rate adjusting step width determining circuit 6 during manufacture, the rate adjusting amount can be determined in common for all specimens of a line of manufactured timepieces.

Take as a concrete example the case mentioned above in which S = 0.008 sec/day. If the necessary rate adjusting amount L is 0.056 sec/day, the number P of adjusting steps required is 7 (derived from L=P.S). Accordingly, by setting P(=7) in the terminals L6 to L9 of the rate adjusting amount determining circuit 7, from $F4(7) = \frac{1}{7} F3(20)$, the desired adjusting amount F4(P) can be obtained in the same way as in the case of the rate adjusting step width determining circuit.

The control circuit 8 produces the signal F5 which represents the ratio of F4(P) and F1 and which controls the electronic switch 3, so that the desired rate adjustment is obtained.

Figure 6 shows the timing of the above signals and will, it is thought, be self explanatory from the references thereon.

The invention is not limited to the embodiment so far described, and many modifications are possible without departing from the scope of the invention. For example the circuits 6 and 7 may utilise down-counting counters.

If the delay introduced by the control circuit 8 is large enough to warrant it, means may be provided for dealing with it. Figure 7 is a block diagram, similar to Figure 1, of an embodiment in which this is done. In Figure 7, a microprocessor (not shown) is employed.

Referring to Figure 7, the quartz crystal oscillator 1, which supplies time standard signals to the divider 4', has its oscillation frequency adjusted by opening and closing the electronic switch 3 which is connected to the oscillator through the capacitor 2. Divider means 4' divides the output from the quartz oscillator 1 to produce the time standard signal F_o for the rest of the watch (represented by block 5') and a signal F6 which is applied to the control circuit 8' and is one of the signals determining the resolution of rate adjustment. The divider 4' may be constructed of random logic circuits or be so constructed as to perform division in accordance with a predetermined program. The apparatus in block 5' may comprise means for performing as well as a basic timepiece function, a timer function, a stop watch function and, indeed, any other function, e.g. that of an alarm, known in electronic

timepiece practice, utilising the frequency F_o for the purpose or purposes. From a suitable point in the known circuitry in block 5' is taken a signal F7 determining the resolution and the effecting synchronization of rate adjustment. The apparatus in block 5' may include a stage of frequency in division (following the stages in block 4') or part of the time-keeping circuitry may be in block 4'. The signal F7 may accordingly be taken from block 4' or block 5' in accordance with the particular design and construction employed. The rate adjusting step width determining circuit 6' calculates the adjustable rate amount effected by one step of rate adjustment from the resolution determined by the signals F6 and F7 and the value α determining the adjusting width. The α input is applied externally to 6' as indicated in conventional manner. The rate adjusting amount determining circuit 7' calculates the total adjusting amount from the rate adjusting step width calculated by the rate adjusting step width determining circuit 6' and the value P, determining the total amount of adjustment, is applied externally to 7' as conventionally indicated. The control circuit 8' produces a timing signal F8 for opening and closing the switch 3 in accordance with the total rate adjusting amount as calculated by the rate adjusting amount determining circuit 7' and the signals F6 and F7. In this way the oscillation

frequency of the quartz crystal oscillator 1 is varied to effect rate adjustment. The portion of the circuitry enclosed by the broken line B represents the portion of the apparatus which is processed by the software of the microprocessor (not shown) supplying the inputs α and P. The characteristics shown in Figure 4 and already described apply also to the embodiment of Figure 7.

In the embodiment of Figure 7 the resolution $\underline{d}$ is as given by:-

$$d = \Delta f \cdot \frac{F6}{F7}$$

F7 is accordingly a signal determining the cycle of the timing for opening the switch 3 and F6 is a signal determining the minimum unit time for opening and closing the switch 3. The rate adjusting step width S is expressed by $S = \alpha \cdot d$ and this calculation is performed by the rate adjusting step width determining circuit 6' in accordance with a predetermined program. As will now be appreciated, although $\underline{d}$ varies with variation of Δf, it is possible to make S constant by adjusting the coefficient α. Therefore, if in the course of manufacturing a line of watches, $\underline{d}$ is suitably chosen after measurements of Δf, the value of α corresponding with the desired value of S is calculated with respect to an individual timepiece (α may, for example, be 4 in this embodiment) and the calculated value of α is set into the rate adjusting step width determining

means circuit 6'. This adjusting amount effected by one step of rate adjustment will be, practically speaking, the same for all specimens of the same manufacturing line of watches

It will be seen to follow, from the description already given of Figure 7, that there are various possible ways of making S constant, by changing the coefficient α in $S = \alpha d$ for it will be at once appreciated that if any of the values F6, F7 and α is changed the same effects are enjoyed.

Once the ajdusting width of one step is determined, it is easy to determine how many steps are necessary to adjust the rate of any individual timepiece. If L in Figure 4 is the rate adjusting amount, it is easy to effect a total required amount of rate adjustment by externally applying to 7' an input P which satisfies the equation $L = PS$.

The control circuit 8' produces the signal F8 which keeps switch 3 open for a period $\alpha PF6$ seconds every F7 seconds, when the total adjusting amount calculated by the rate adjusting amount determining circuit 7' is set into it. The control circuit 8' may, for example, be a preset down counting counter.

As already mentioned before, if α is set by the timepiece manufacturer and the value of P is given to timepiece retailers, precise rate adjustment can be effected speedily and without difficulty by the average timepiece retailer before he sells an individual watch in a line of manufactured watches.

To recapitulate, even if there are manufacturing differences between the capacitances of individual capacitors 2, the rate adjusting step width calculating means (6 or 6') will determine the adjusting amount per step the same for all watches of a line; the retailer can then set the number of steps in accordance with the desired total adjusting amount; the rate adjusting amount determining circuit (7 or 7') and the controller circuit (8 or 8') will then automatically produce the signal (F3 or F8) for adjusting the rate by controlling the opening and closing of the switch 3; and thus precise rate adjustment is quickly and easily performed. All the retailer has to do is to determine and set the adjusting step number P while taking into account the rate adjusting width of one step (as previously determined by the manufacturer and of which he has been informed), and the required total adjusting amount will be obtained regardless of manufacturing differences between different watches in a line of manufactured watches. Moreover the minimum adjusting amount can be made very small (because the minimum resoltuion is determined only by the ratio of F1 to F2 in Figure 1 or of F6 to F7 in Figure 7). So if this invention is used in combination with a conventional digital method of changing the division ratio of the divider, the method of setting the rate adjusting amount will appear to the outside observer to differ from the conventional digital tuning

method only in that the setting "bit" number is increased. And finally, the invention enables rate adjustment of a timepiece to be effected easily and simply to an extreme degree of precision unattainable by the general logic tuning methods commonly employed hitherto. The invention is thus very advantageous commercially, not least because of the facility for after-sales service it provides for timepiece retailers.

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C L A I M S

1. An electronic timepiece comprising frequency dividing means for producing a reference signal determining the resolution of rate adjustment; rate adjusting step width determining means for determining the rate adjusting width achieved by one step of adjustment; rate adjusting amount determining means for determining the rate adjusting amount; and control means for controlling the time ratio of connection of a frequency adjusting reactance element in a time standard piezo-electric oscillator of the timepiece.

2. An electronic timepiece including a time-standard piezo-electric crystal oscillator the frequency of which is variable to effect time-keeping rate adjustment by switch means switching reactance in and out of the oscillator circuit; frequency dividing means for dividing the oscillator output frequency to produce time standard signals for determining the resolution of rate adjustment; rate adjustment step width determining means for determining the rate adjustment step width (amount of adjustment step) required to accord with the determined resolution; rate adjustment amount determining

* C L M S *

means for determining the required rate adjusting amount in accordance with the rate adjustment step width; and control means controlling the operation of the switching means under the control of time standard signals and output signals from said rate adjustment amount determining means, the whole arrangement being such that, irrespective of the actual value within a relatively wide range of possible values of the reactance switched in and out, the amount of rate adjustment per step of adjustment remains substantially constant at a known predetermined selected value.

3. A timepiece as claimed in claim 1 or 2 wherein a synchronising frequency (F_1) is applied to the rate adjustment step width determining means, the rate amount determining means and to the control means; said rate adjustment step width determining means has a further input consisting of a frequency difference which depends on the actual value of the capacitance switched in and out and further input terminals for receiving signals for determining the total adjustment width and provides output signals to said rate adjustment amount determining means; the last-mentioned means supplies its output (F_4P) to the control means and has further input terminals for receiving signals for determining the number of steps of adjustment required; and the control means is constituted by an electronic switch controlled thereby and effecting the switching.

* C L M S *

4. A timepiece as claimed in claim 1 or 2 wherein a frequency (Fo) is applied from the frequency dividing means to the rate adjustment step with determining means and to the rate adjustment amount determining means; a further input frequency (F_7) is applied as an input to the rate adjustment step with determining means and to the control means, the former of these two means receiving a control input (α) from a micro-processor and providing an output to the rate adjustment amount determining means which receives a control input (P) from said micro-processor; and the control means also receives the output from said rate adjustment amount determining means, a frequency from the frequency dividing means and provides an output (F_8) controlling an electron switch switching the reactance in and out.

5. Electronic timepieces having rate adjustment means operating substantially as herein described with reference to Figures 1, 4, 5, 6 and 7 of the accompanying drawings.

6. An electronic timepiece substantially as herein described with reference to Figure 1 of the accompanying drawings.

7. An electronic timepiece substantially as herein described with reference to Figure 7 of the accompanying drawings.

8. An electronic timepiece as claimed in claim 6 and having rate adjusting circuitry substantially as herein described with reference to Figure 5 of the accompanying drawings.

9. An electronic timepiece as claimed in any of the preceding claims and including also known means for digitally varying the division ratio of the frequency dividing means.

10. In an electronic timepiece including a quartz crystal oscillator operating as a time standard and a capacitor for changing the frequency delivered from said quartz crystal oscillator, said capacitor being connected to said oscillator through intermediary of a switching means, and the closing and opening of said switching means effecting the pace adjustment of said electronic timepiece, an improvement comprising:

a divider means for dividing the output of said quartz crystal oscillator and producing the standard signals determining the resolution of the pace adjustment;

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a pace adjusting step width determining means for determining the necessary pace adjusting width of one step according to said resolution;

a pace adjusting amount determining means for determining the required pace adjusting amount according to said pace adjusting step width;

a controller circuit for controlling the ratio of the closing and opening of said switching means according to said standard signals and the output of said pace adjusting amount determining means; and the pace adjustment being realized based upon the output of said controller circuit.