

DATA READING METHOD AND APPARATUS

TECHNICAL FIELD

[0001] This application relates to the storage field, and in particular, to a data reading method and apparatus.

BACKGROUND

[0002] At present, each floating-gate transistor used for storage on a solid state drive (English: Solid State Drive, SSD for short) can store two or three bits. The bits stored in each floating-gate transistor are separately distributed on different pages (English: page). Therefore, pages in each block are classified into two or three different types according to storage locations in floating-gate transistors.

[0003] Using multi-level cell storage (English: Multi Level Cell, MLC for short) as an example, two bits of a floating-gate transistor of the multi-level cell storage are respectively referred to as a least significant bit (English: Least Significant Bit, LSB for short) and a most significant bit (English: Most Significant Bit, MSB for short). Therefore, in each block, pages on which different bits in floating-gate transistors are separately located are classified into two types: an LSB page (for storing the LSB of the floating-gate transistor; the LSB page may also be referred to as a lower page and in this application, the LSB page is used uniformly) and an MSB page (for storing the MSB of the floating-gate transistor; the MSB page may also be referred to as an upper page and in this application, the MSB page is used uniformly). On a basis that data of corresponding bits of the LSB page and the MSB page is stored in a same floating-gate transistor, the LSB page and the MSB page belong to one group of shared pages (English: shared pages). Specifically, Table 1 describes shared pages in a block of an MLC of a vendor.

Table 1

LSB page	MSB page	LSB page	MSB page
0	2	...	...
1	4	241	244
3	6	243	246

5	8	245	248
7	10	247	250
9	12	249	252
11	14	251	254
...	...	253	255

[0004] When data is being written, it is required that LSBs be written before MSBs. Therefore, data can be written into a corresponding MSB page only after an entire LSB page is full. However, writing data into the MSB page causes interference to data that has been written into the LSB page before. Using the foregoing MLC of the vendor as an example, Table 2 describes interference data that is obtained during data writing according to an experiment.

Table 2

Page	Page 0	Page 1	Page 2	Page 3	Page 4	Page 5	Page 6	Page 7	Page 8
Page 0	0	0	<u>125</u>	<u>105</u>	5	3	4	6	3
Page 1		2	1	1	50	35	8	9	6
Page 2			0	0	0	0	0	0	0
Page 3				0	0	0	<u>296</u>	<u>193</u>	25
Page 4					17	15	14	15	16
Page 5						0	0	0	<u>270</u>
Page 6							0	0	0
Page 7								1	0
Page 8									0

[0005] The foregoing Table 2 describes interference on vertical pages when data is written into horizontal pages. It can be known from the foregoing Table 2 that, when data is being written into an MSB page, a relatively severe error correcting code (English: Error Correcting Code, ECC for short) error or uncorrectable ECC error (English: Uncorrectable ECC Error, UNC for short) may occur on a shared LSB page of the MSB page and on a shared LSB page of an adjacent MSB page. As shown in Table 2, underlined data has relatively severe errors.

[0006] Likewise, for a storage device whose floating-gate transistor stores more bits, for example, a storage device whose floating-gate transistor stores three bits, which means that a group of shared pages includes an LSB page, a middle significant bit (English: middle significant bit, CSB for short) page, and an MSB page, writing into an upper page also causes write

maximum page number difference m between an MSB page and an LSB page in all groups of shared pages in the non-volatile storage space, where m is a natural number; and allocating cache space with a size of at least $n \cdot p + m$ pages for the preset cache area, where p represents a quantity of shared pages of an MSB page in the non-volatile storage space, and n is a natural number and is at least 1.

[0012] With reference to the second possible implementation manner of the first aspect, in a third possible implementation manner of the first aspect, the method further includes: if the write target address belongs to an MSB page in the non-volatile storage space, determining whether the MSB page in which the write target address is located is the last MSB page in a block; if the MSB page in which the write target address is located is not the last MSB page in the block, obtaining an address of a shared page of the n^{th} MSB page as counted forward from the MSB page in which the write target address is located, and using the obtained address as a data release address; or if the MSB page in which the write target address is located is the last MSB page in the block, obtaining addresses of shared pages of the last $n+1$ MSB pages in the block, and using the obtained addresses as the data release addresses; and releasing data that is in the preset cache area and that a cache address having the first mapping relationship with the data release address points to, and deleting the data release address from the first mapping relationship.

[0013] With reference to the first aspect or any one of the first to third possible implementation manners of the first aspect, in a fourth possible implementation manner of the first aspect, the method further includes: during power-off, saving data that is in the preset cache area in the non-volatile storage space, and establishing a second mapping relationship between the cache address and a save address that is in the non-volatile storage space; and during power-on, caching, at the cache address in the preset cache area according to the second mapping relationship, the data that the save address in the non-volatile storage space points to.

[0014] With reference to the first aspect or the first to third possible implementation manners of the first aspect, in a fifth possible implementation manner of the first aspect, the preset cache area is located in a double data rate synchronous dynamic random access memory DDR or a static random access memory SRAM.

[0015] With reference to the first aspect or the first to third possible implementation manners of the first aspect, in a sixth possible implementation manner of the first aspect, the non-volatile storage space is storage space of a solid state drive SSD.

[0016] A second aspect of this application provides a data reading apparatus. The apparatus includes a first determining module, a first reading module, and a second reading module. The first determining module is configured to: when receiving a read instruction that includes a read target

address, determine whether a preset cache area has cached data that the read target address points to, and send a first determining result to the first and second reading modules. The first reading module is configured to: when the preset cache area has cached the data that the read target address points to, find a cache address corresponding to the read target address according to a first mapping relationship, and read, from the preset cache area, data that the cache address points to, where the first mapping relationship is used to record a correspondence between the target address and the cache address. The second reading module is configured to: when the preset cache area has not cached the data that the read target address points to, read, from non-volatile storage space, the data that the read target address points to.

[0017] With reference to the second aspect, in a first possible implementation manner of the second aspect, the apparatus further includes a second determining module, a first writing module, and a second writing module. The second determining module is configured to: when receiving a write instruction, determine whether a write target address in the write instruction belongs to a most significant bit page MSB page in the non-volatile storage space, and send a second determining result to the first and second writing modules, where the write instruction includes to be written data and the write target address. The first writing module is configured to: when it is determined that the write target address does not belong to an MSB page in the non-volatile storage space, store, in the preset cache area and the non-volatile storage space that is corresponding to the write target address, the to be written data, and establish the first mapping relationship between the cache address and the target address. The second writing module is configured to: when it is determined that the write target address belongs to an MSB page in the non-volatile storage space, store, in the non-volatile storage space corresponding to the write target address, the to be written data.

[0018] With reference to the first possible implementation manner of the second aspect, in a second possible implementation manner of the second aspect, the apparatus further includes a third obtaining module and an allocating module. The third obtaining module is configured to obtain a maximum page number difference m between an MSB page and an LSB page in all groups of shared pages in the non-volatile storage space, and send m to the allocating module, where m is a natural number. The allocating module is configured to allocate cache space with a size of at least $n \cdot p + m$ pages for the preset cache area, where p represents a quantity of shared pages of an MSB page in the non-volatile storage space, and n is a natural number and is at least 1.

[0019] With reference to the second possible implementation manner of the second aspect, in a third possible implementation manner of the second aspect, the apparatus further includes a third determining module, a first obtaining module, a second obtaining module, and a releasing module. The third determining module is configured to: when the write target address belongs to an MSB

page in the non-volatile storage space, determine whether the MSB page in which the write target address is located is the last MSB page in a block, and send a third determining result to the first and second obtaining modules. The first obtaining module is configured to: when the MSB page in which the write target address is located is not the last MSB page in the block, obtain an address of a shared page of the n^{th} MSB page as counted forward from the MSB page in which the write target address is located, use the obtained address as a data release address, and send the data release address to the releasing module. The second obtaining module is configured to: when the MSB page in which the write target address is located is the last MSB page in the block, obtain addresses of shared pages of the last $n+1$ MSB pages in the block, use the obtained addresses as the data release addresses, and send the data release addresses to the releasing module. The releasing module is configured to release data that is in the preset cache area and that a cache address having the first mapping relationship with the data release address points to, and delete the data release address from the first mapping relationship.

[0020] With reference to the second aspect or the first to third possible implementation manners of the second aspect, in a fourth possible implementation manner of the second aspect, the apparatus further includes a saving module and a caching module. The saving module is configured to: during power-off, save data that is in the preset cache area in the non-volatile storage space, establish a second mapping relationship between the cache address and a save address that is in the non-volatile storage space, and send the second mapping relationship to the caching module. The caching module is configured to: during power-on, cache, at the cache address in the preset cache area according to the second mapping relationship, the data that the save address in the non-volatile storage space points to.

[0021] With reference to the second aspect or the first to third possible implementation manners of the second aspect, in a fifth possible implementation manner of the second aspect, the preset cache area is located in a double data rate synchronous dynamic random access memory DDR or a static random access memory SRAM.

[0022] With reference to the second aspect or the first to third possible implementation manners of the second aspect, in a sixth possible implementation manner of the second aspect, the non-volatile storage space is storage space of a solid state drive SSD.

[0023] In the foregoing solutions, a manner in which cached data is preferentially read is used. When a preset cache area has cached data that a read target address points to, the data is preferentially read from the preset cache area. Because data in the cache area is not subject to write interference as in non-volatile storage space, read errors caused by write interference are reduced, and reliability of a storage device is improved.

bits, the pages of the non-volatile storage space of the storage device further include a CSB page.

[0047] The controller of the storage device receives, from an interface such as a SATA/SAS/PCIe interface, a write instruction sent by a host. The write instruction includes to be written data and a write target address, so as to instruct the controller to store, in the non-volatile storage space that the write target address points to, the to be written data. After receiving the write instruction, the controller first determines whether the write target address belongs to an MSB page in the non-volatile storage space. If the write target address does not belong to an MSB page in the non-volatile storage space, the controller executes step 202. If the write target address belongs to an MSB page in the non-volatile storage space, the controller executes step 203.

[0048] 202. The controller of the storage device stores, in the preset cache area and the non-volatile storage space that is corresponding to the write target address, the to be written data, and establishes a first mapping relationship between a cache address and the write target address.

[0049] As described in the background, when data is being written into an MSB page in non-volatile storage space of a storage device, write interference is caused to a shared page of the MSB page, such as a corresponding LSB page or CSB page, and a data read error may occur as a result. Therefore, when the controller determines that the write target address does not belong to an MSB page, it means that the to be written data may be subject to write interference when data is being written into an MSB page subsequently. Therefore, the controller stores, in the non-volatile storage space that the write target address points to, the to be written data, and caches the data into the preset cache area as a backup. The preset cache area may be a double data rate synchronous dynamic random access memory (English: double data rate synchronous dynamic random access memory, DDR SDRAM for short) in the storage device. For example, a conventional SSD is inherently provided therein with a DDR, and data passes the DDR no matter in data writing or data reading. Based on this storage manner, the preset cache area may be preferentially configured on the DDR, that is, some cache space is provided on the DDR as the preset cache area. Certainly, the preset cache area may alternatively be a memory other than the non-volatile storage space, for example, a static random access memory (English: Static Random-Access Memory, SRAM for short).

[0050] After the foregoing writing is complete, the controller obtains a cache address at which the to be written data is cached in the preset cache area, and establishes a first mapping relationship between the cache address and the write target address, so that the data in the preset cache area corresponds to the data in the non-volatile storage space. The first mapping relationship may be saved in a tabular form in the non-volatile storage space of the storage device or in the preset cache area.

[0051] 203. The controller of the storage device stores, in the non-volatile storage space

an LSB page in the groups of shared pages of the non-volatile storage space of the storage device. It means that the preset cache area requires cache space of at least m pages, to ensure that a shared page of an MSB page (such as an LSB page or a CSB page corresponding to the MSB page) can be cached in the preset cache area before the MSB page is fully written, so as to avoid a read error due to write interference of the MSB page. In addition, the dynamic release rule of this application is that, when data is being written into an MSB page, it is ensured that shared pages of at least n MSB pages (such as LSB pages or CSB pages corresponding to the MSB pages) as counted forward from the MSB pages can be cached in the preset cache area. According to experimental data, when n is at least 1, it can be essentially ensured that data currently subject to relatively severe write interference can all be cached.

[0060] According to the foregoing principle for specifying the cache space size and the foregoing rule for setting groups of shared pages of the non-volatile storage space of the storage device, to ensure that data currently subject to relatively severe write interference can all be cached, the controller of the storage device allocates, for the preset cache area, cache space of at least $m+n*p$ pages, for example, allocates cache space of $m+n*p$ pages. p represents a quantity of shared pages of an MSB page in the non-volatile storage space of the storage device. For example, one group of shared pages of an MLC-type storage device includes an MSB page and an LSB page. Therefore, a quantity of shared pages of the MSB page in non-volatile storage space of the storage device is 1, that is, the LSB page. One group of shared pages of a TLC-type storage device includes an MSB page, a CSB page, and an LSB page. Therefore, a quantity of shared pages of the MSB page in non-volatile storage space of the storage device is 2, including the CSB page and the LSB page.

[0061] 303. When receiving a write instruction, the controller of the storage device determines whether a write target address in the write instruction belongs to an MSB page in the non-volatile storage space, where the write instruction includes to be written data and the write target address.

[0062] After receiving the write instruction, the controller first determines whether the write target address belongs to an MSB page in the non-volatile storage space of the storage device. If the write target address does not belong to an MSB page in the non-volatile storage space, the controller executes step 304. If the write target address belongs to an MSB page in the non-volatile storage space, the controller executes step 305.

[0063] 304. The controller of the storage device stores, in the preset cache area and the non-volatile storage space that is corresponding to the write target address, the to be written data, and establishes a first mapping relationship between a cache address and the target address.

[0064] 305. The controller of the storage device stores, in the non-volatile storage space

corresponding to the write target address, the to be written data, and determines whether an MSB page in which the write target address is located is the last MSB page in a block.

[0065] If the write target address belongs to an MSB page in the non-volatile storage space, the controller of the storage device stores, only in the non-volatile storage space that the write target address points to, the to be written data, and determines whether the MSB page in which the write target address is located is the last MSB page in the block. For example, the last MSB page in the block shown in Table 1 is page 255. If it is determined that the write target address does not belong to page 255, the controller executes step 306. If it is determined that the write target address belongs to page 255, the controller executes step 307.

[0066] 306. The controller of the storage device obtains an address of a shared page of the n^{th} MSB page as counted forward from the MSB page in which the write target address is located, and uses the obtained address as a data release address.

[0067] In this implementation manner, a dynamic cache release manner is used. A specific rule is that, when data is being written into an MSB page, it is ensured that shared pages of at least n MSB pages (such as LSB pages or CSB pages corresponding to the MSB pages) can be cached in a preset cache area. Using the MLC-type storage device shown in Table 2 in the background as an example, it can be known from Table 2 that an LSB page is subject to relatively severe write interference in a process between writing an MSB page corresponding to the LSB page and starting writing a next MSB page. It can be ensured that data currently subject to relatively severe write interference can all be cached, only when a minimum value of n is 1. However, to further reduce write interference, n is preferentially at least 2, that is, an LSB page corresponding to an MSB page is not deleted before writing of data into at least two MSB pages next to the MSB page is complete.

[0068] Specifically, still using the storage device described in Table 1 in the background as an example, it is assumed that a current write target address belongs to page 6, which is an MSB page, and does not belong to the last MSB page. As counted forward from page 6, the first MSB page is page 4, and the second MSB page is page 2. If n is 1, it is considered that no write interference will be caused to a shared page of page 4, that is, page 1, after data is written into page 6. Therefore, the controller obtains an address of page 1 and uses the address of page 1 as a data release address, so as to release cache space that is in the preset cache area and that is corresponding to page 1. According to the foregoing dynamic cache release rule, when data is written into page 2, data in the cache area is not released; when data is written into page 4, page 0 in the cache area is released; when data is written into page 6, page 1 in the cache area is released; when data is written into page 8, page 3 in the cache area is released; and so on. In this way, correct data can be read from the cache before write interference indicated by the underlined data in Table 2 is eliminated.

[0069] It is the same for a storage device whose floating-gate transistor stores more than two bits. That is, addresses of shared pages (if the floating-gate transistor stores three bits, a corresponding LSB page and a corresponding CSB page are included) of the n^{th} MSB page as counted forward from the MSB page in which the write target address is located are obtained and used as data release addresses.

[0070] 307. The controller of the storage device obtains addresses of shared pages of the last $n+1$ MSB pages in the block, and uses the obtained addresses as the data release addresses.

[0071] If the MSB page in which the write target address is located is the last MSB page in the block, it means that write interference of all pages in the block is eliminated, and therefore all data cache space of the block can be released. According to the cache release rule of the foregoing step 306, when data is being written into the last MSB page, data of shared pages of the last $n+1$ MSB pages in the block remains cached in the preset cache area, where n is a natural number and is at least 1. Therefore, the controller obtains the addresses of the shared pages (which are LSB pages if the floating-gate transistor stores two bits, or include LSB pages and CSB pages if the floating-gate transistor stores three bits) of the last $n+1$ MSB pages in the block, and uses the obtained addresses as the data release addresses.

[0072] 308. The controller of the storage device releases data that is in the preset cache area and that a cache address having the first mapping relationship with the data release address points to, and deletes the data release address from the first mapping relationship.

[0073] The controller of the storage device obtains, according to the first mapping relationship, the cache address having the first mapping relationship with the data release address, and releases the data at the cache address. In this way, cache space can be dynamically released while ensuring that data currently subject to severe write interference remains cached. Because the cache space is already released, the data release address and the cache address in the first mapping relationship are deleted.

[0074] 309. When receiving a read instruction that includes a read target address, the controller of the storage device determines whether the preset cache area has cached data that the read target address points to. If the preset cache area has cached the data that the read target address points to, the controller executes step 310. If the preset cache area has not cached the data that the read target address points to, the controller executes step 311.

[0075] 310. The controller of the storage device finds a cache address corresponding to the read target address according to a first mapping relationship, and reads, from the preset cache area, data that the cache address points to.

[0076] 311. The controller of the storage device reads, from the non-volatile storage space, the

data that the read target address points to.

[0077] In this implementation manner, data for which a read error may occur due to write interference of an MSB page is cached for backup. In addition, during reading of this part of data, the data is preferentially read from a cache. This avoids the occurrence of an error in reading the data due to that the data is currently subject to write interference, thereby greatly reducing read errors caused by write interference. Moreover, in this implementation manner, because when data is being written into an MSB page of a storage device, write interference is caused only to a shared page of the MSB page and to a shared page of an adjacent MSB page before the MSB page, a manner of dynamically releasing a cache is used, to reduce required cache space. In addition, in this application, cache space is allocated according to a maximum page number difference m of shared page groups of a storage device, so as to enable compatibility with storage devices of different vendors.

[0078] Referring to FIG. 4, FIG. 4 is a partial flowchart of yet another implementation manner of a data reading method according to this application. The method in this implementation manner includes the steps in the foregoing implementation manner and further includes the following steps.

[0079] 401. During power-off, the controller of the storage device saves data that is in the preset cache area in the non-volatile storage space, and establishes a second mapping relationship between the cache address and a save address that is in the non-volatile storage space.

[0080] After the storage device is powered off, the data in the preset cache area is lost. To ensure that the data in the non-volatile storage space can still be correctly read after next power-on, during power-off, the controller saves the data that is in the preset cache area in the non-volatile storage space, and establishes the second mapping relationship between the cache address that is in the preset cache area and the save address that is in the non-volatile storage space, so that the data previously cached in the preset cache area can correspond to the data saved in the non-volatile storage space.

[0081] 402. During power-on, the controller of the storage device caches, at the cache address in the preset cache area according to the second mapping relationship, the data that the save address in the non-volatile storage space points to.

[0082] When powered on again, the controller of the storage device obtains the save address that is in the non-volatile storage space and that is in the second mapping relationship, and correspondingly caches the data at the save address at the cache address that has the second mapping relationship with the save address, so as to cache again, according to the original cache address, the data that is cached in the preset cache area before power-off. In this way, when data that is in the non-volatile storage space and that has been cached needs to be read, corresponding cached

page, a CSB page, and an LSB page. Therefore, a quantity of shared pages of the MSB page in non-volatile storage space of the storage device is 2, including the CSB page and the LSB page.

[0108] The third determining module 630 is configured to: when the write target address belongs to an MSB page in the non-volatile storage space, determine whether the MSB page in which the write target address is located is the last MSB page in a block, and send a third determining result to the first obtaining module 640 and the second obtaining module 650.

[0109] For example, when the second determining module 540 determines that the write target address belongs to an MSB page in the non-volatile storage space, the third determining module 630 determines whether the MSB page in which the write target address is located is the last MSB page in the block.

[0110] The first obtaining module 640 is configured to: when the MSB page in which the write target address is located is not the last MSB page in the block, obtain an address of a shared page of the n^{th} MSB page as counted forward from the MSB page in which the write target address is located, use the obtained address as a data release address, and send the data release address to the releasing module 660.

[0111] In this implementation manner, a dynamic cache release manner is used. A specific rule is that, when data is being written into an MSB page, it is ensured that shared pages of at least n MSB pages (such as LSB pages or CSB pages corresponding to the MSB pages) can be cached in a preset cache area. Using the MLC-type storage device shown in Table 2 in the background as an example, it can be known from Table 2 that an LSB page is subject to relatively severe write interference in a process between writing an MSB page corresponding to the LSB page and starting writing a next MSB page. It can be ensured that data currently subject to relatively severe write interference can all be cached, only when a minimum value of n is 1. However, to further reduce read interference, n is preferentially at least 2. That is, an LSB page corresponding to an MSB page is not deleted before writing of data into at least two MSB pages next to the MSB page is complete.

[0112] Specifically, still using the storage device described in Table 1 in the background as an example, it is assumed that a current write target address belongs to page 6, which is an MSB page, and does not belong to the last MSB page. As counted forward from page 6, the first MSB page is page 4, and the second MSB page is page 2. If n is 1, it is considered that no write interference will be caused to a shared page of page 4, that is, page 1, after data is written into page 6. Therefore, the first obtaining module 640 uses an address of page 1 as a data release address, so as to release cache space that is in the preset cache area 570 and that is corresponding to page 1.

[0113] It is the same for a storage device whose floating-gate transistor stores more than two bits. That is, addresses of shared pages (if the floating-gate transistor stores three bits, a

non-volatile storage device.

[0120] The caching module 680 is configured to: during power-on, cache, at the cache address in the preset cache area 570 according to the second mapping relationship, the data that the save address in the non-volatile storage space points to.

5 **[0121]** When powered on again, the caching module 680 obtains the save address that is in the non-volatile storage space and that is in the second mapping relationship, and correspondingly caches the data at the save address at the cache address that has the second mapping relationship with the save address, so as to cache again, according to the original cache address, the data that is cached in the preset cache area before power-off. In this way, when data that is in the non-volatile
10 storage space and that has been cached needs to be read, corresponding cached data can be read according to the first mapping relationship that is previously established, and thereby correct data reading is implemented.

[0122] It may be understood that, the data reading apparatus in this application is not limited to including all the modules in this implementation manner. In a different implementation manner, in
15 addition to the modules shown in FIG. 5, the data reading apparatus may further include only the third obtaining module and the allocating module, or further include only the third determining module, the first obtaining module, the second obtaining module, and the releasing module, or further include only the saving module and the caching module, or further include modules of two of the three alternatives.

20 **[0123]** Referring to FIG. 7, FIG. 7 is a schematic structural diagram of an implementation manner of a controller according to this application. The controller 700 in this implementation manner includes a receiver 701, a processor 702, a memory 703, and a bus 704. The controller 700 is connected to a preset cache area 710 and non-volatile storage space 720.

[0124] The receiver 701 is configured to receive a write instruction and a read instruction.

25 **[0125]** The processor 702 is configured to:
when receiving a read instruction that includes a read target address, determine whether the preset cache area 710 has cached data that the read target address points to; and
when the preset cache area has cached the data that the read target address points to, find a cache address corresponding to the read target address according to a first mapping relationship, and read, from the preset cache area 710, data that the cache address points to, where the first
30 mapping relationship is used to record a correspondence between the target address and the cache address; or when the preset cache area has not cached the data that the read target address points to, read, from the non-volatile storage space 720, the data that the read target address points to.

[0126] Optionally, the processor 702 may be further configured to:

when receiving a write instruction, determine whether a write target address in the write instruction belongs to a most significant bit page MSB page in the non-volatile storage space 720, where the write instruction includes to be written data and the write target address; and

when it is determined that the write target address does not belong to an MSB page in the non-volatile storage space, store, in the preset cache area 710 and the non-volatile storage space 720 that is corresponding to the write target address, the to be written data, and establish a first mapping relationship between a cache address and the target address; or when it is determined that the write target address belongs to an MSB page in the non-volatile storage space, store, in the non-volatile storage space 720 corresponding to the write target address, the to be written data.

10 **[0127]** Optionally, the processor 702 is further configured to:

when the write target address belongs to an MSB page in the non-volatile storage space 720, determine whether the MSB page in which the write target address is located is the last MSB page in a block;

when the MSB page in which the write target address is located is not the last MSB page in the block, obtain an address of a shared page of the n^{th} MSB page as counted forward from the MSB page in which the write target address is located, and use the obtained address as a data release address, where n is a natural number and is at least 1; or when the MSB page in which the write target address is located is the last MSB page in the block, obtain addresses of shared pages of the last $n+1$ MSB pages in the block, and use the obtained addresses as the data release addresses, where n is a natural number and is at least 1; and

release data that is in the preset cache area 710 and that a cache address having the first mapping relationship with the data release address points to, and delete the data release address from the first mapping relationship.

[0128] Optionally, the processor 702 is further configured to:

25 obtain a maximum page number difference m between an MSB page and an LSB page in all groups of shared pages in the non-volatile storage space 720, where m is a natural number; and

allocate cache space with a size of at least $n \cdot p + m$ pages for the preset cache area 710, where p represents a quantity of shared pages of an MSB page in the non-volatile storage space 720, and n is a natural number and is at least 1.

30 **[0129]** Optionally, the processor 702 is further configured to:

during power-off, save data that is in the preset cache area 710 in the non-volatile storage space 720, and establish a second mapping relationship between the cache address and a save address that is in the non-volatile storage space 720; and

during power-on, cache, at the cache address in the preset cache area 710 according to

the second mapping relationship, the data that the save address in the non-volatile storage space 720 points to.

[0130] The memory 703 may include a read-only memory and a random access memory, and provide instructions and data for the processor 702. A part of the memory 703 may further include a non-volatile random access memory (NVRAM). In another implementation manner, the memory 703 may alternatively be located in a same storage medium with the non-volatile storage space 720.

[0131] The memory 703 stores the following elements, executable modules or data structures, a subset thereof, or an extension set thereof:

operating instructions: including various operating instructions used to implement various operations; and

an operating system: including various system programs, which are used to implement various basic services and process hardware-based tasks.

[0132] In an embodiment of the present invention, the processor 702 executes the foregoing operations by calling the operating instructions stored in the memory 703 (the operating instructions may be stored in the operating system).

[0133] The processor 702 may also be referred to as a CPU (Central Processing Unit, central processing unit). In a specific application, components of the controller are coupled together by using the bus 704. The bus 704 includes a data bus, and in addition, may further include a power bus, a control bus, a state signal bus, and the like. However, for clarity of description, various buses are marked as the bus 704 in the figure.

[0134] The method disclosed in the foregoing embodiments of the present invention may be applied to the processor 702, or implemented by the processor 702. The processor 702 may be an integrated circuit chip and has a signal processing capability. In an implementation process, the steps of the foregoing methods may be completed by using a hardware integrated logic circuit of the processor 702 or software instructions. The processor 702 may be a general-purpose processor, a digital signal processor (DSP), an application-specific integrated circuit (ASIC), a field programmable gate array (FPGA) or another programmable logical device, a discrete gate or a transistor logic device, or a discrete hardware component. The methods, steps, and logical block diagrams disclosed in the embodiments of the present invention can be implemented or executed.

The general-purpose processor may be a microprocessor, or the processor may be any conventional processor or the like. The steps of the methods disclosed in the embodiments of the present invention may be directly executed by a hardware decoding processor, or executed by a combination of hardware in a decoding processor and software modules. The software modules may

CLAIMS

1. A data reading method, comprising:

determining whether a preset cache area has cached data that a read target address points to when receiving a read instruction that comprises the read target address; and

5 finding a cache address corresponding to the read target address according to a first mapping relationship if the preset cache area has cached the data that the read target address points to, and reading, from the preset cache area, data that the cache address points to, wherein the first mapping relationship is used to record a correspondence between the read target address and the cache address; or
10 reading, from non-volatile storage space, the data that the read target address points to if the preset cache area has not cached the data that the read target address points to.

2. The method according to claim 1, further comprising:

when receiving a write instruction, determining whether a write target address in the write instruction belongs to a most significant bit page MSB page in the non-volatile storage space, wherein the write instruction comprises to be written data and the write target address; and

15 if the write target address does not belong to an MSB page in the non-volatile storage space, storing, in the preset cache area and the non-volatile storage space that is corresponding to the write target address, the to be written data, and establishing the first mapping relationship between the cache address and the write target address; or if the write target address belongs to an MSB page in the non-volatile storage space, storing, in the non-volatile storage space corresponding to the write
20 target address, the to be written data.

3. The method according to claim 2, further comprising:

obtaining a maximum page number difference m between an MSB page and an LSB page in all groups of shared pages in the non-volatile storage space, wherein m is a natural number; and

25 allocating cache space with a size of at least $n \cdot p + m$ pages for the preset cache area, wherein p represents a quantity of shared pages of an MSB page in the non-volatile storage space, and n is a natural number and is at least 1.

4. The method according to claim 3, further comprising:

30 if the write target address belongs to an MSB page in the non-volatile storage space, determining whether the MSB page in which the write target address is located is the last MSB page in a block;

if the MSB page in which the write target address is located is not the last MSB page in the block, obtaining an address of a shared page of the n^{th} MSB page as counted forward from the MSB

page in which the write target address is located, and using the obtained address as a data release address; or if the MSB page in which the write target address is located is the last MSB page in the block, obtaining addresses of shared pages of the last $n+1$ MSB pages in the block, and using the obtained addresses as a data release addresses; and

5 releasing data that is in the preset cache area and a cache address having the first mapping relationship with the data release address points to, and deleting the data release address from the first mapping relationship.

5. The method according to any one of claims 1 to 4, further comprising:

10 during power-off, saving data that is in the preset cache area in the non-volatile storage space, and establishing a second mapping relationship between the cache address and a save address that is in the non-volatile storage space; and

 during power-on, caching, at the cache address in the preset cache area according to the second mapping relationship, the data that the save address in the non-volatile storage space points to.

15 6. The method according to any one of claims 1 to 4, wherein the preset cache area is located in a double data rate synchronous dynamic random access memory, DDR SDRAM or a static random access memory SRAM.

 7. The method according to any one of claims 1 to 4, wherein the non-volatile storage space is storage space of a solid state drive SSD.

20 8. A data reading apparatus, comprising a first determining module, a first reading module, and a second reading module, wherein

 the first determining module is configured to: when receiving a read instruction that comprises a read target address, determine whether a preset cache area has cached data that the read target address points to, and send a first determining result to the first and second reading modules;

25 the first reading module is configured to: when the preset cache area has cached the data that the read target address points to, find a cache address corresponding to the read target address according to a first mapping relationship, and read, from the preset cache area, data that the cache address points to, wherein the first mapping relationship is used to record a correspondence between the target address and the cache address; and

30 the second reading module is configured to: when the preset cache area has not cached the data that the read target address points to, read, from a non-volatile storage space, the data that the read target address points to.

 9. The apparatus according to claim 8, further comprising a second determining module, a first writing module, and a second writing module, wherein

 the second determining module is configured to: when receiving a write instruction, determine

whether a write target address in the write instruction belongs to a most significant bit page MSB page in the non-volatile storage space, and send a second determining result to the first and second writing modules, wherein the write instruction comprises to be written data and the write target address;

5 the first writing module is configured to: when it is determined that the write target address does not belong to an MSB page in the non-volatile storage space, store, in the preset cache area and the non-volatile storage space that is corresponding to the write target address, the to be written data, and establish the first mapping relationship between the cache address and the write target address; and

10 the second writing module is configured to: when it is determined that the write target address belongs to an MSB page in the non-volatile storage space, store, in the non-volatile storage space corresponding to the write target address, the to be written data.

10. The apparatus according to claim 9, further comprising a third obtaining module and an allocating module, wherein

15 the third obtaining module is configured to obtain a maximum page number difference m between an MSB page and an LSB page in all groups of shared pages in the non-volatile storage space, and send m to the allocating module, wherein m is a natural number; and

20 the allocating module is configured to allocate cache space with a size of at least $n \times p + m$ pages for the preset cache area, wherein p represents a quantity of shared pages of an MSB page in the non-volatile storage space, and n is a natural number and is at least 1.

11. The apparatus according to claim 10, further comprising a third determining module, a first obtaining module, a second obtaining module, and a releasing module, wherein

25 the third determining module is configured to: when the write target address belongs to an MSB page in the non-volatile storage space, determine whether the MSB page in which the write target address is located is the last MSB page in a block, and send a third determining result to the first and second obtaining modules;

30 the first obtaining module is configured to: when the MSB page in which the write target address is located is not the last MSB page in the block, obtain an address of a shared page of the n^{th} MSB page as counted forward from the MSB page in which the write target address is located, use the obtained address as a data release address, and send the data release address to the releasing module;

 the second obtaining module is configured to: when the MSB page in which the write target address is located is the last MSB page in the block, obtain addresses of shared pages of the last $n+1$ MSB pages in the block, use the obtained addresses as the data release addresses, and send the data