

Trellis Code for Extended Partial Response Maximum Likelihood
(EPRML) Channel

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

The present invention relates to encoding for disk drives and, particularly, to an improved trellis code for an extended partial response with maximum likelihood (EPRML) channel.

DESCRIPTION OF THE RELATED ART

In order to achieve higher recording densities, designers of magnetic recording channels have switched from analog peak detection techniques to sampled data detection techniques. In sampled data detection systems, the readback signal is filtered and sampled at a channel rate of $1/T$, where T is the duration of a channel symbol. One such technique is referred to as extended partial response maximum likelihood (EPRML). The discrete time transfer function of an extended partial response channel is $(1+D-D^2-D^3)$, where D represents a unit time delay operator with unit-time T . Thus, the noiseless output of the extended partial response channel is equal to the input signal minus a version of the input signal delayed in time by $2T$, minus a version of the input signal delayed in time by $3T$ and plus a version of the input signal forward in time by T . In an EPRML system the output of the noisy partial response channel is sampled at the channel rate and detected using a maximum likelihood Viterbi detector.

Modulation codes are used to generate inputs to EPRML channels to increase detectability of the recorded bit sequences. With such codes, it is desirable to decrease the maximum number of consecutive zeroes and to maximize the minimum number of transitions per code word. Further, it is desirable to minimize the error propagation due to EPRML minimum distance channel errors.

Additionally, in order to achieve higher recording densities, it is desirable to have as efficient a code as possible. Generally, code efficiency is expressed in terms of a rate,

which is the ratio of the number of input bits to be encoded to the number of output bits in the resulting code word. It is desirable to have the rate approach unity.

SUMMARY OF THE INVENTION

A first trellis code according to the present invention is a rate 24/26 trellis code with three (3) bytes error propagation due to EPRML minimum distance channel errors, a minimum of six (6) transitions per code word and a maximum of twelve (12) consecutive zeroes. A second trellis code according to the present invention is a rate 48/51 trellis code, derived from the first trellis code. The second trellis code has four (4) bytes error propagation due to EPRML minimum distance channel errors, a minimum of twelve (12) transitions per code word and a maximum of twelve (12) consecutive zeroes. A third trellis code according to the present invention is a rate 48/51 trellis code with four (4) bytes error propagation due to EPRML minimum distance channel errors, a minimum of fourteen (14) transitions per code word and a maximum of eleven (11) consecutive zeroes.

BRIEF DESCRIPTION OF THE DRAWINGS

A better understanding of the invention is obtained when the following detailed description is considered in conjunction with the following drawings in which:

FIG. 1 is a diagram of an EPRML channel according to an embodiment of the invention;

FIG. 2A is a block diagram of an exemplary encoder according to an embodiment of the invention;

FIG. 2B is a block diagram of an exemplary decoder according to an embodiment of the invention;

FIGS. 3, 4A, 4B, and 5-8 characterize an exemplary trellis code according to the embodiment of FIGS. 2A and 2B;

FIG. 9A is a block diagram of an exemplary encoder according to an embodiment of the invention;

FIG. 9B is a block diagram of an exemplary decoder according to an embodiment of the invention;

FIG. 10A is a block diagram of an exemplary encoder according to an embodiment of the invention;

FIG. 10B is a block diagram of an exemplary decoder according to an embodiment of the invention;

FIGS. 11A, 11B, 12A, 12B and 13-14 characterize an exemplary trellis code according to another embodiment of the invention;

FIG. 15A is a block diagram of an exemplary encoder according to an embodiment of the invention; and

FIG. 15B is a block diagram of an exemplary decoder according to an embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

Turning now to the drawings and with particular attention to FIG. 1, a block diagram illustrating an EPRML channel according to an embodiment of the invention is shown. The channel 10 includes an encoder 12 according to the present invention, a precoder 14, an EPR channel 16, a Viterbi detector 18, a postcoder 19, and a decoder 20. The encoder 12 produces one or more novel trellis codes according to the present invention, as will be explained in greater detail below.

A first trellis code according to the present invention is a rate 24/26 trellis code with three (3) bytes error propagation due to EPRML minimum distance channel errors, a minimum of six (6) transitions per code word and a maximum of twelve (12) consecutive zeroes. A second trellis code according to the present invention is a rate 48/51 trellis code, derived from the first trellis code. The second trellis code has four (4) bytes error propagation due to EPRML minimum distance channel errors, a minimum of twelve (12) transitions per code word and a maximum of twelve (12) consecutive zeroes. A third trellis code according to the present invention is a rate 48/51 trellis code with four (4) bytes error propagation due to EPRML minimum distance channel errors, a minimum of fourteen (14) transitions per code word and a maximum of eleven (11) consecutive zeroes.

As shown in FIG. 1, an input signal on a line 22 is transmitted to an input of an encoder 12. The encoder 12 produces an encoded output signal from the input signal, as

will be explained in greater detail below. The output of the encoder 12 is coupled to the line 24 to provide the coded sequence to the precoder 14.

The precoder 14 has an input and an output and generates a precoded sequence based on the coded sequence. In particular, according to an embodiment of the present invention, the precoder 14 is defined by the transfer function $(1/1 \oplus D \oplus D^2 \oplus D^3)$. The precoder 14 may be a finite state machine with input x , output y and state s , where at time n the following holds:

initial state	$s_{\text{initial}} = (\text{state}_1 \text{ state}_2 \text{ state}_3)$, where state_k , $k=1,2$, and 3 , is the output of the pre-coder at time $n-k$,
output	$y = x + \text{state}_1 + \text{state}_2 + \text{state}_3 \pmod{2}$, and
final state	$s_{\text{final}} = (y \text{ state}_1 \text{ state}_2)$.

The precoder 14 will be described further with regard to the particular embodiments. The output of the precoder 14 is coupled to the line 26 to provide the precoded sequence to the EPR channel 16. An output of the precoder 14 is also provided back to the encoder 12, as will be described in greater detail below.

A detector 18 receives the output of the EPR channel 16 along line 28. The detector 18 may be a Viterbi detector. The detector 18 provides the detected output along a line 30 to a postcoder 19, which essentially performs the inverse of the precoder 14. The output of the postcoder 19 is provided to the decoder 20. The decoder 20 performs the inverse of the encoder 12 and has several embodiments, each corresponding to an embodiment of the trellis code, as will be described below.

As noted above, a first embodiment of the encoder implements a rate 24/26 trellis code with three (3) bytes error propagation due to EPRML minimum distance channel errors, a minimum of six (6) transitions per code word and a maximum of twelve (12) consecutive zeroes. A block diagram of an encoder 12A according to this embodiment is shown in FIG. 2A. In particular, as shown, the encoder 12A is characterized by a first map F and a second map f , as will be explained in greater detail below. Two maps $M1$ and $M2$ further characterize the map F , as will be explained in greater detail below. A decoder according to this embodiment is shown in FIG. 2B. The decoder 20A is characterized by a Map FF , which is further characterized by Maps $MM1$ and $MM2$, as will be explained in greater detail below.

The encoder 12A according to this embodiment may be implemented as a finite state machine that receives 24-bit data, $(a_1 a_2 \dots a_{12})(a_2 a_2 \dots a_{12})$, and outputs a 26-bit code-word, $(b_1 b_2 \dots b_{12}) e_1 (b_2 b_2 \dots b_{12}) e_2$. It is noted that a_1 is the first bit received and b_1 is the first bit transmitted.

As noted above, the code-word is passed through a $(1/(1 \oplus D \oplus D^2 \oplus D^3))$ pre-coder. For this embodiment, the output of the pre-coder 14A has an even number of ones every 26 bits that span the image of a code-word. Specifically, if $(x_1 x_2 \dots x_{26}) = (b_1 b_2 \dots b_{12}) e_1 (b_2 b_2 \dots b_{12}) e_2$ is input to the pre-coder having initial state $s_{\text{initial}} = (state_1 state_2 state_3)$, then $y_1 + y_2 + \dots + y_{26} = 0 \pmod{2}$, where y_k is the output of the pre-coder corresponding to the input x_k .

As noted above, the encoder 12A can be characterized by two maps F and f , where

$$F: (a_1 a_2 \dots a_{12})(a_2 a_2 \dots a_{12}) \implies (b_1 b_2 \dots b_{12}) e_1 (b_2 b_2 \dots b_{12}),$$

and

$$f: (a_1 a_2 \dots a_{12})(a_2 a_2 \dots a_{12}) \times s_{\text{initial}} \implies e_2.$$

Also as noted above, the Map F may be described by two maps $M1$ and $M2$. The Map $M1$ maps 12 bits, $a = (a_1 \dots a_{12})$, to 11 bits, $(b_1 \dots b_{11})$. Next, several sets are defined which help to partition the domain of map $M1$:

(Let
 $'$ to denote Complement
 $\wedge$ to denote AND
 $\vee$ to denote OR
 $\oplus$ to denote EXCLUSIVE OR)

Let:

$C1 = \{ (a_1 \dots a_{12}): a_2 = a_3, a_4 = a_5, a_6 = a_7 \}$ (has 2^9 points)
 $C2 = \{ (a_1 \dots a_{12}): a_1 = a_2, a_3 = a_4, a_5 = a_6, a_7 = a_8 \}$ (has 2^8 points)
 $C3 = \{ (a_1 \dots a_{12}): a_2 = a_3 = a_4 = a_5 = a_6 \}$ (has 2^8 points)
 $C4 = \{ (a_1 \dots a_{12}): a_1 + a_2 + \dots + a_{12} \leq 1 \}$ (has $12+1=13$ points)

Let:

$C = C1 \cup C2 \cup C3 \cup C4$
 $B1 = C1 \cap C4'$
 $B2 = C2 \cap C1' \cap C4'$
 $B3 = C3 \cap C1' \cap C2' \cap C4'$
 $B4 = C4$

$$B = B1 \cup B2 \cup B3 \cup B4$$

$$G = B'$$

LEMMA 1 $B=C$.

LEMMA 2 B_i 's are pair-wise disjoint.

Let:

$$V1 = \{a2=a4, a6=a8\}$$

$$V2 = \{a1=1, a2=1, a4=a6\}$$

$$V3 = \{1 = a2 = a4 = a6\}$$

$$R1 = V1$$

$$R2 = V2 \cap V1'$$

$$R3 = V3 \cap V2' \cap V1'$$

The mapping for the Map M1 is shown in FIG. 3. In particular, the second to the left-most column defines the sets (i.e., the subset of M1) to which the bits $a = (a1 \dots a12)$ belong (i.e., the sets define the partitioning of the map). The top row defines the eleven bits $b = (b1 \dots b11)$ into which the twelve bits $a = (a1 \dots a12)$ are to be mapped. The remainder of the table defines the particular mapping. For example, if the twelve bits $a = (a1 \dots a12)$ belong to the set defined by G above, then the eleven bits $(b1 \dots b11) = (a1 \dots a11)$. Similarly, if the twelve bits $a = (a1 \dots a12)$ belong to the set defined by $B2$ above, then the bits are mapped into $b = (b1 \dots b11) = (0, 1, 0, a2, a4, a6, a8, a9, a10, a11, a12)$.

The map M2 maps 12 bits, $a=(a1 \dots a12)$, to 10 bits, $(v1 \dots v10)$. Several sets are defined which help to partition the domain of map M2.

Let:

$E1 = \{ (a1 \dots a12): a4=a5, a6=a7, a8=a9, a10=a11 \}$	(has 2^8 points)
$E2 = \{ (a1 \dots a12): a3=a4, a5=a6, a7=a8, a9=a10 \}$	(has 2^8 points)
$E3 = \{ (a1 \dots a12): a4=a5 = a6 = a7 = a8=a9=a10 \}$	(has 2^6 points)
$E4 = \{ (a1 \dots a12): a1+a2+\dots+a12 \leq 2 \}$	(has $66+12+1=79$ points)
$E5 = \{ (a1 \dots a12): a6+a7+a8+a9+a10+a11+a12=0 \}$	

Let:

$$E = E1 \cup E2 \cup E3 \cup E4$$

$$D1 = E1 \cap E4'$$

$$D2 = E2 \cap E1' \cap E4'$$

$$D3 = E3 \cap E1' \cap E2' \cap E4'$$

$$D4 = E4$$

$$\begin{aligned}
D5 &= E5 \cap E1' \cap E2' \cap E3' \cap E4' \\
D &= D1 \cup D2 \cup D3 \cup D4 \cup D5 \\
GG &= D'
\end{aligned}$$

LEMMA 1 $E=D$.

LEMMA 2 D_i 's are pair-wise disjoint.

Let:

$$\begin{aligned}
T1 &= \{a1=1 \ a2=1 \quad a3=a5 \ a7=a9\} \\
T2 &= \{a2=a3 \quad a5=a7 \ a9=a11\} \\
T3 &= \{a1=a3 \quad a7=a11\} \\
T4 &= \{a1=0 \ a2=a3=a5=a7=a9=1 \ a11=0\}
\end{aligned}$$

The actual mapping of the Map M2 is shown in FIG. 4A and FIG. 4B. For example, if the set $a = (a1 \dots a12)$ belongs to the set GG, then the 10-bit set $v = (v1 \dots v10)$ takes on the values $(a3, a4, a5, a6, a7, a8, a9, a10, a11, a12)$.

To complete the encoder characterization it is necessary to define the maps F and f. Let's recall that

$$F: (a1 \ a2 \dots a12)(a21 \ a22 \dots a212) \implies (b1 \ b2 \dots b12) \ e1 \ (b21 \ b22 \dots b212),$$

and

$$f: (a1 \ a2 \dots a12)(a21 \ a22 \dots a212) \times s_{\text{initial}} \implies e2.$$

The table of FIG. 7 completes the description of the Map F. For example, if A1 is in the set G and A2 is in the set GG, then $b11 \dots b111$ is $M1(A1)$; $b112$ is $a112$; $e1$ is 1; $b21$ is $a21$; $b22$ is $a22$; and $b23b24 \dots b212$ is $M2(A2)$.

The following equation describes the Map f:

$$e2 = b29 + b25 + b21 + b110 + b16 + b12 + \text{state}_1 + \text{state}_2,$$

$$\text{where } s_{\text{initial}} = (\text{state}_1 \ \text{state}_2 \ \text{state}_3).$$

Thus, the current code-word is passed through the pre-coder 14A and the final state of the pre-coder is the initial state for the computation of $e2$ of the next code-word.

The decoder 20A according to this embodiment is a block map, which inverts the encoder. The decoder 20A receives 26 bits, $(b1 \ b2 \dots b12) \ e1 \ (b21 \ b22 \dots b212) \ e2$, and it outputs a 24 bit data, $(a1 \ a2 \dots a12)(a21 \ a22 \dots a212)$. As noted above, the decoder can be characterized by a map FF, where

$$FF: (b1 \ b2 \dots b12) \ e1 \ (b21 \ b22 \dots b212) \ e2 \implies (a1 \ a2 \dots a12)(a21 \ a22 \dots a212)$$

$a_22...a_212$).

The Map MM1 is defined in FIG. 5 and maps eleven bits ($b_1...b_{11}$) to twelve bits ($a_1...a_{12}$). For example, if $b_2=1$ and $b_3=1$, then $(a_1...a_{12}) = (b_1, b_4, b_4, b_5, b_5, b_6, b_6, b_7, b_8, b_9, b_{10}, b_{11})$.

The map MM2 maps 10 bits ($v_1...v_{10}$) to twelve bits ($a_1...a_{12}$). The map MM2 is shown in FIG. 6. For example, if $v_2=0$ and $v_3=1$, then $(a_1...a_{12}) = (v_1, v_4, v_5, v_6, v_6, v_7, v_7, v_8, v_8, v_9, v_9, v_{10})$.

The table of FIG. 8 completes the characterization of the map FF. For example, if $e_1=1$, then $(a_11 a_12...a_110) = (b_11b_12...b_110)$, $a_111 = b_111$, $a_112 = b_112$, $a_21 = b_21$, $a_22 = b_22$, and $(a_23a_24...a_212) = (b_23b_24...b_212)$.

A rate 48/51 trellis code according to a second embodiment of the invention may be generated from the 24/26 trellis code described above. In particular, the trellis code according to this embodiment has four (4) bytes error propagation due to EPRML minimum distance channel errors, a minimum of twelve (12) transitions per code word and a maximum of twelve (12) consecutive zeroes. FIG. 9A illustrates a block diagram of an encoder 12B according to this embodiment. The encoder 12B according to this embodiment includes a pair of Maps FA and FB, which are characterized similarly to the Map F described above. In addition, a Map fa is provided, as will be explained in greater detail below. A decoder 20B according to this embodiment is shown in FIG. 9B. As will be explained in greater detail below, the decoder 20B includes a pair of maps FFA and FFB, which are generally similar to the Map FF described above.

The encoder 12B according to this embodiment is characterized as follows: $(a_11 a_12...a_112)(a_21 a_22...a_212)(a_31 a_32...a_312)(a_41 a_42...a_412) == >$

$(b_11 b_12...b_112) e_1 (b_21 b_22...b_212) (b_31 b_32...b_312) e_2 (b_41 b_42...b_412) e_3$,

where

$(b_11 b_12...b_112) e_1 (b_21 b_22...b_212) = FA ((a_11 a_12...a_112)(a_21 a_22...a_212))$,

$(b_31 b_32...b_312) e_2 (b_41 b_42...b_412) = FB ((a_31 a_32...a_312)(a_41 a_42...a_412))$, where the

Maps FA and FB are as described above with reference to the Map F.

The Map fa is described by the following equation: $e_3 = b_{49} + b_{45} + b_{41} + b_{310} + b_{36} + b_{32} + b_{210} + b_{26} + b_{22} + b_{111} + b_{17} + b_{13} + \text{state}_1$

Encoding for the first 25 code-word bits may begin after 24 data bits are received. Thus, it is not necessary to receive all 48 data bits to begin coding.

The decoder 20B according to this embodiment is characterized as follows: $(b_1 \ 1 \ b_1 2 \dots b_1 12) \ e_1 \ (b_2 \ 1 \ b_2 2 \dots b_2 12) \ (b_3 \ 1 \ b_3 2 \dots b_3 12) \ e_2 \ (b_4 \ 1 \ b_4 2 \dots b_4 12) \ e_3 \implies (a_1 \ 1 \ a_1 2 \dots a_1 12) (a_2 \ 1 \ a_2 2 \dots a_2 12) \ (a_3 \ 1 \ a_3 2 \dots a_3 12) (a_4 \ 1 \ a_4 2 \dots a_4 12)$,

where

$$(a_1 \ 1 \ a_1 2 \dots a_1 12) (a_2 \ 1 \ a_2 2 \dots a_2 12) = \text{FFA} ((b_1 \ 1 \ b_1 2 \dots b_1 12) \ e_1 \ (b_2 \ 1 \ b_2 2 \dots b_2 12)),$$

$$(a_3 \ 1 \ a_3 2 \dots a_3 12) (a_4 \ 1 \ a_4 2 \dots a_4 12) = \text{FFB} ((b_3 \ 1 \ b_3 2 \dots b_3 12) \ e_2 \ (b_4 \ 1 \ b_4 2 \dots b_4 12)),$$

where the Maps FFA and FFB are as described above with reference to the Map FF (with e_3 used for parity purposes in the Viterbi decoder).

Decoding for the first 24 data bits may begin after 25 code-word bits are received. Thus, it is not necessary to receive all 51 code word bits to begin decoding.

Finally, a 48/51 trellis code according to another embodiment of the invention is described. According to this embodiment, a rate 48/51 trellis code is provided, with four (4) bytes error propagation due to EPRML minimum distance channel errors, a minimum of fourteen (14) transitions per code word and a maximum of eleven (11) consecutive zeroes.

The code, TC, encoder is characterized as follows:

$$(a_1 \ 1 \ a_1 2 \dots a_1 12) (a_2 \ 1 \ a_2 2 \dots a_2 12) \ (a_3 \ 1 \ a_3 2 \dots a_3 12) (a_4 \ 1 \ a_4 2 \dots a_4 12) \implies$$

$$(b_1 \ 1 \ b_1 2 \dots b_1 12) \ e_1 \ (b_2 \ 1 \ b_2 2 \dots b_2 12) \ (b_3 \ 1 \ b_3 2 \dots b_3 12) \ e_2 \ (b_4 \ 1 \ b_4 2 \dots b_4 12) \ e_3,$$

It is noted that $a_1 \ 1$ is the first bit received and $b_1 \ 1$ is the first bit transmitted. The pre-coder 14 according to this embodiment has an even number of ones (1) every 51 bits that span the image of a code-word. Specifically, if

$$(x_1 \ x_2 \ \dots \ x_{51}) = (b_1 \ 1 \ b_1 2 \dots b_1 12) \ e_1 \ (b_2 \ 1 \ b_2 2 \dots b_2 12) \ (b_3 \ 1 \ b_3 2 \dots b_3 12) \ e_2 \ (b_4 \ 1 \ b_4 2 \dots b_4 12) \ e_3$$

is input to the pre-coder 14 having initial state $s_{\text{initial}} = (\text{state}_1 \ \text{state}_2 \ \text{state}_3)$, then

$y_1 + y_2 + \dots + y_{51} = 0 \pmod{2}$, where y_k is the output of the pre-coder corresponding to the input x_k .

First, we define a rate 24/25 code C, as shown in FIG. 10A and FIG. 10B. The encoder for the Code C includes an encoder 12C characterized by a Map F1, which is further characterized by a Map M3, as will be explained in greater detail below. The Code C decoder 20C (FIG. 10B), in turn, may be characterized by a Map FF1, which is further characterized by a Map MM3, as will also be explained in greater detail below.

The code C encoder 12C may be embodied as a finite state machine that receives 24-bit data, $(a_1 a_2 \dots a_{12})(a_2 a_2 \dots a_{12})$, and outputs a 25-bit code-word, $(b_1 b_2 \dots b_{12}) e_1 (b_2 b_2 \dots b_{12})$.

As noted above, the encoder 12C can be characterized by a map F1, where $F1: (a_1 a_2 \dots a_{12})(a_2 a_2 \dots a_{12}) \implies (b_1 b_2 \dots b_{12}) e_1 (b_2 b_2 \dots b_{12})$.

The decoder 20C can be characterized by a map FF1, where $FF1: (b_1 b_2 \dots b_{12}) e_1 (b_2 b_2 \dots b_{12}) \implies (a_1 a_2 \dots a_{12})(a_2 a_2 \dots a_{12})$.

A map M3 is used to specify the map F1. The map M3 maps 12 bits, $a=(a_1 \dots a_{12})$, to 10 bits, $(b_1 \dots b_{10})$. Next we define several sets which help to partition the domain of map M3.

(Let ' to denote Complement
 $\wedge$ to denote AND
 $\vee$ to denote OR
 $\oplus$ to denote EXCLUSIVE OR)

Let:
 $C1 = \{ (a_1 \dots a_{12}): a_2=a_3, a_4=a_5, a_6=a_7, a_8=a_9 \}$ (has 2^8 points)
 $C2 = \{ (a_1 \dots a_{12}): a_3=a_4, a_5=a_6, a_7=a_8, a_9=a_{10} \}$ (has 2^8 points)
 $C3 = \{ (a_1 \dots a_{12}): a_3 = a_4 = a_5 = a_6 = a_7 = a_8 = a_9 \}$ (has 2^6 points)
 $C4 = \{ (a_1 \dots a_{12}): a_1+a_2+\dots+a_{12} \leq 2 \}$ (has $66+12+1=79$ points)
 $C5 = \{ (a_1 \dots a_{12}): a_1+a_2+\dots+a_6 = 0 \} \cap C1' \cap C2' \cap C3' \cap C4'$

Let
 $C = C1 \cup C2 \cup C3 \cup C4$
 $B1 = C1 \cap C4'$
 $B2 = C2 \cap C1' \cap C4'$
 $B3 = C3 \cap C1' \cap C2' \cap C4'$
 $B4 = C4$
 $B5 = C5$
 $B = B1 \cup B2 \cup B3 \cup B4 \cup B5$
 $G = B'$

LEMMA 1 $B=C$.

LEMMA 2 B_i 's are pair-wise disjoint.

Then, the Map M3 maps 12 bits into 10 bits as shown in the table of FIGS. 11A and 11B. Then, the table of FIG. 13 completes the characterization of the Map F1.

The Code C decoder 20C is a block map, which inverts the encoder. The decoder receives 25 bits, $(b_1 b_2 \dots b_{12}) e_1 (b_2 b_2 \dots b_{12})$, and it outputs a 24 bit data, $(a_1 a_2 \dots a_{12})(a_2 a_2 \dots a_{12})$. The decoder can be characterized by a map FF1, where $FF1: (b_1 b_2 \dots b_{12}) e_1 (b_2 b_2 \dots b_{12}) \Rightarrow (a_1 a_2 \dots a_{12})(a_2 a_2 \dots a_{12})$. A map MM3 is used to characterize the map FF1. The map MM is shown in FIGS. 12A and 12B. Finally, the table of FIG. 13 completes the characterization of the map FF1 from the map MM2.

The rate 24/25 code, C, described above is used to generate a trellis code, TC, having a rate 48/51. Block diagrams of a Code TC encoder and decoder are shown in FIG. 15A and FIG. 15B, respectively. In particular, the Code TC encoder 12D includes a pair of Maps F1A and F1B, similar to the Map F1 described above. In addition, a Map f2 is provided, which will be explained in greater detail below. Similarly, the decoder 20D is characterized by a pair of Maps FF1A and FF1B, similar to the Map FF1 described above.

The Code TC encoder is characterized as follows:

$$(b_1 b_2 \dots b_{12}) e_1 (b_2 b_2 \dots b_{12}) = F1A ((a_1 a_2 \dots a_{12})(a_2 a_2 \dots a_{12})),$$

$$(b_3 b_3 \dots b_{12}) e_2 (b_4 b_4 \dots b_{12}) = F1B ((a_3 a_3 \dots a_{12})(a_4 a_4 \dots a_{12})), \text{ and}$$

where the maps F1A and F1B are as the Map F1 described above, and

$$e_3 = b_4 + b_5 + b_4 + b_3 + b_3 + b_2 + b_2 + b_1 + b_1 + b_1 + \text{state}_1, \text{ mod } 2$$

It is noted that it is not necessary to receive all forty-eight (48) data bits to start encoding. As soon as twenty-four (24) data bits are received, the first twenty-five (25) code-word bits may be encoded.

The Code TC decoder is characterized as follows:

$$(b_1 b_2 \dots b_{12}) e_1 (b_2 b_2 \dots b_{12}) (b_3 b_3 \dots b_{12}) e_2 (b_4 b_4 \dots b_{12}) e_3 \Rightarrow$$

$$(a_1 a_2 \dots a_{12})(a_2 a_2 \dots a_{12}) (a_3 a_3 \dots a_{12})(a_4 a_4 \dots a_{12}),$$

where

$$(a_1 a_2 \dots a_{12})(a_2 a_2 \dots a_{12}) = FF1A ((b_1 b_2 \dots b_{12}) e_1 (b_2 b_2 \dots b_{12})),$$

$$(a_3 a_3 \dots a_{12})(a_4 a_4 \dots a_{12}) = FF1B ((b_3 b_3 \dots b_{12}) e_2 (b_4 b_4 \dots b_{12})),$$

where the maps FF1A and FF1B are as the map FF1 described above (and with e_3 used for parity purposes in the Viterbi decoder).

It is noted that it is not necessary to receive all fifty-one (51) bits to start decoding. After twenty-five (25) code-word bits are received, the first twenty-four (24) data bits may be decoded.

CLAIMS

WHAT IS CLAIMED IS:

1. An extended partial response maximum likelihood (EPRML) channel, comprising:
an encoder coupled to receive an input signal and implementing a rate 24/26 trellis code having three (3) bytes error propagation due to EPRML minimum distance channel errors;
a precoder coupled to receive a coded signal from said encoder, perform a precoding operation on said coded signal;
an extended partial response (EPR) channel coupled to receive an output from said precoder;
a detector for detecting an output of said EPR channel; and
a decoder coupled to receive an output of said detector for inverting said encoder.
2. An EPRML channel according to Claim 1, wherein said encoder has a minimum of six (6) transitions per code word.
3. An EPRML channel according to Claim 1, wherein said encoder has a maximum of twelve (12) consecutive zeroes.
4. An EPRML channel according to Claim 1, wherein said encoder implements a rate 48/51 trellis code having four (4) bytes error propagation due to EPRML minimum distance channel errors using a concatenation of said rate 24/26 trellis code.
5. An EPRML channel according to Claim 4, wherein said encoder has a minimum of twelve (12) transitions per code word.
6. An EPRML channel according to Claim 4, wherein said encoder has a maximum of twelve (12) consecutive zeroes.



7. An extended partial response maximum likelihood (EPRML) channel, comprising:
 - an encoder coupled to receive an input signal and implementing a rate 48/51 trellis code having four (4) bytes error propagation due to EPRML minimum distance channel errors;
 - a precoder coupled to receive a coded signal from said encoder, perform a precoding operation on said coded signal;
 - an extended partial response (EPR) channel coupled to receive an output from said precoder;
 - a detector for detecting an output of said EPR channel; and
 - a decoder coupled to receive an output of said detector for inverting said encoder.
8. An EPRML channel according to Claim 7, wherein said encoder has a minimum of fourteen (14) transitions per code word.
9. An EPRML channel according to Claim 7, wherein said encoder has a maximum of eleven (11) consecutive zeroes.
10. An extended partial response maximum likelihood (EPRML) channel, comprising:
 - an encoder coupled to receive an input signal and implementing a trellis code including a partitioning into at least first and second maps;
 - a precoder coupled to receive a coded signal from said encoder, perform a precoding operation on said coded signal;
 - an extended partial response (EPR) channel coupled to receive an output from said precoder;
 - a detector for detecting an output of said EPR channel; and
 - a decoder coupled to receive an output of said detector for inverting said encoder.

