

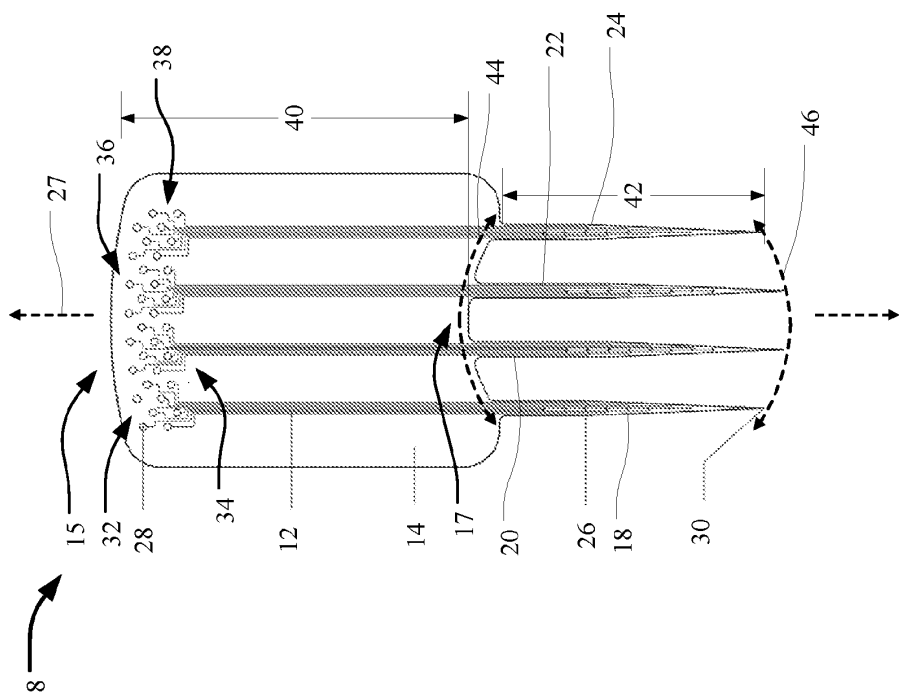


FIG. 1A

2/15

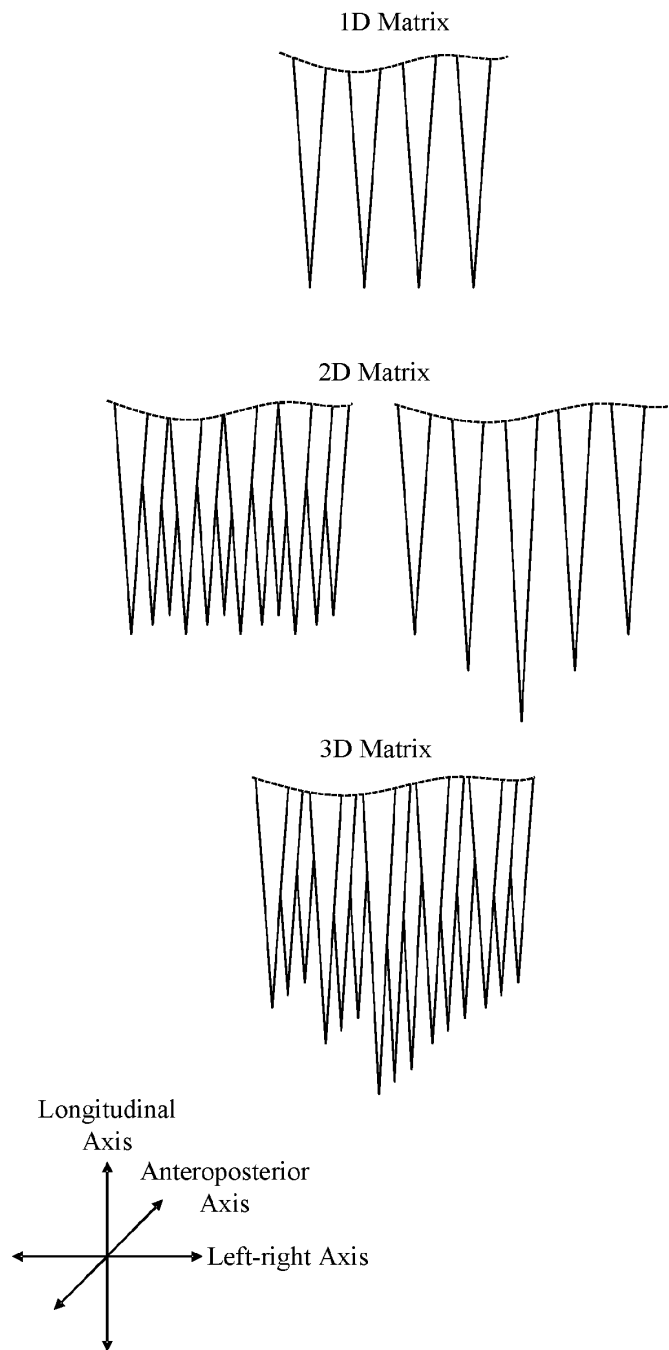


FIG. 1B

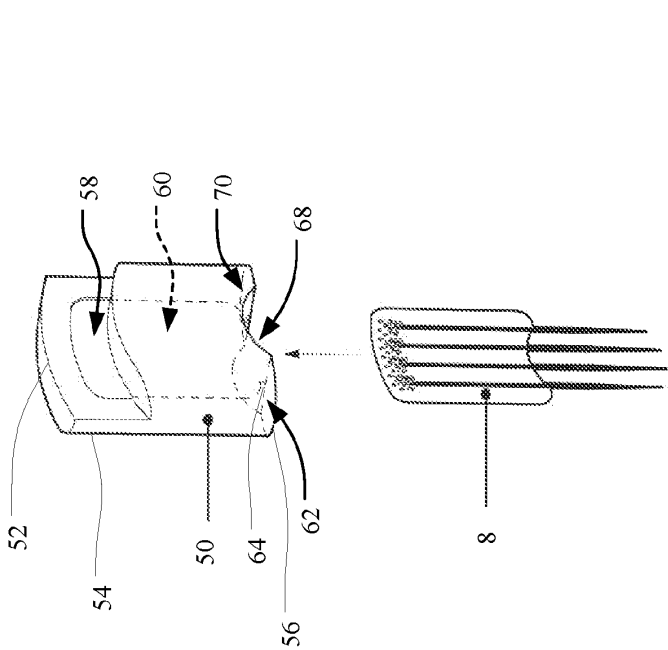


FIG. 2

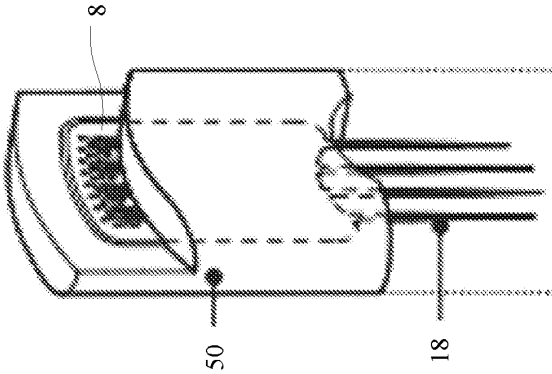


FIG. 3

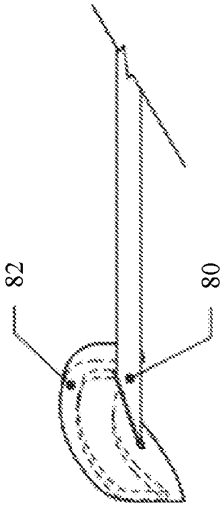


FIG. 4

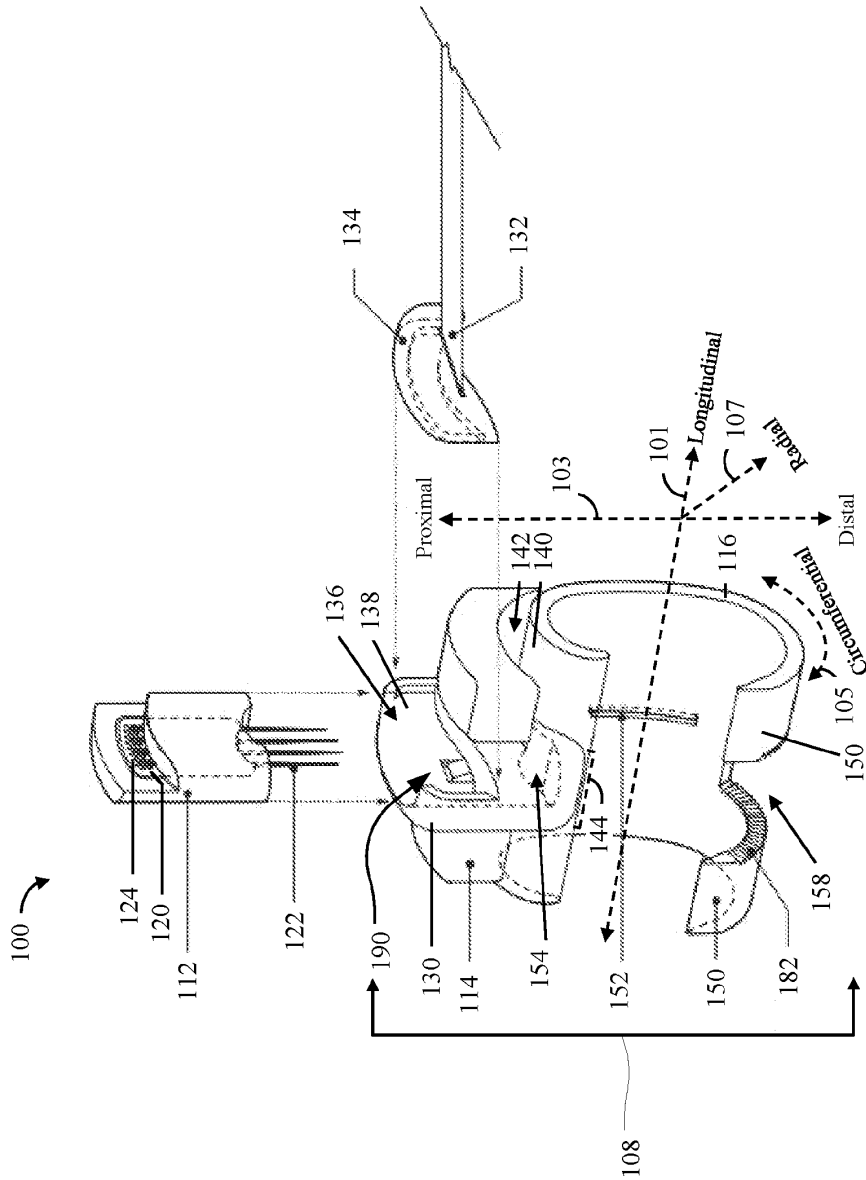


FIG. 5

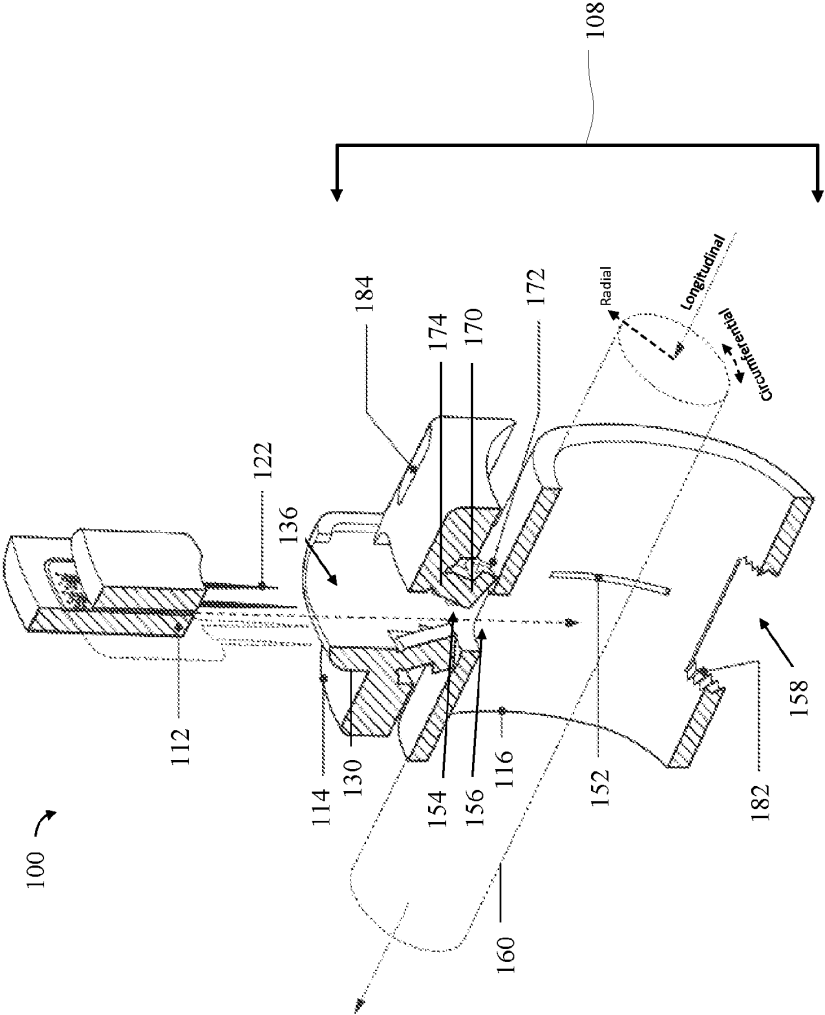


FIG. 6

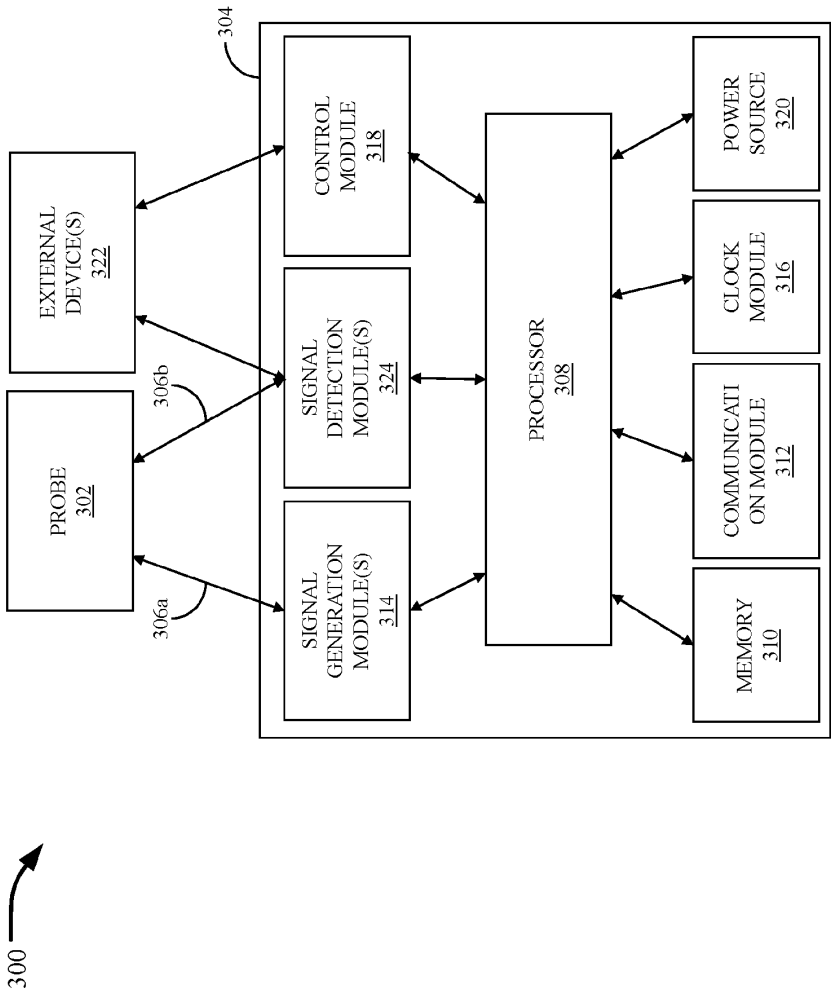


FIG. 7

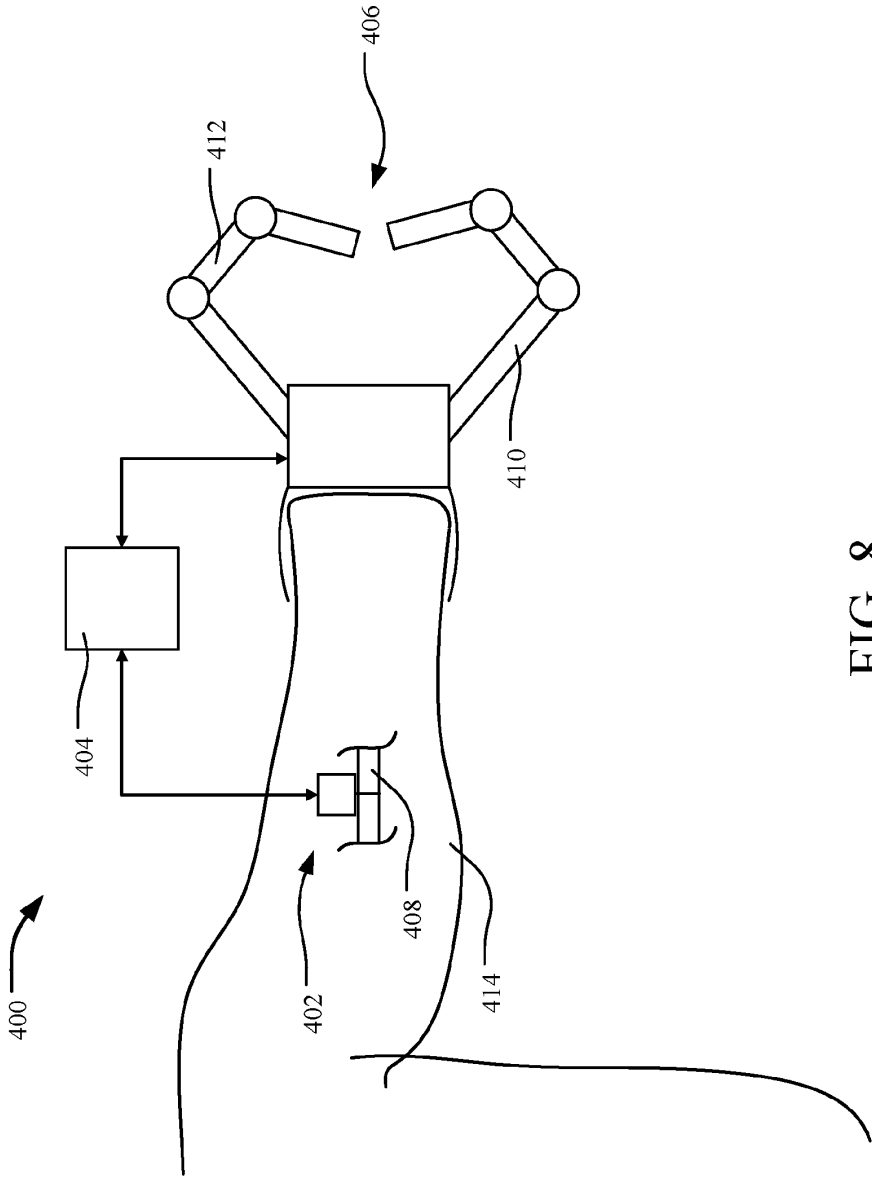


FIG. 8

10/15

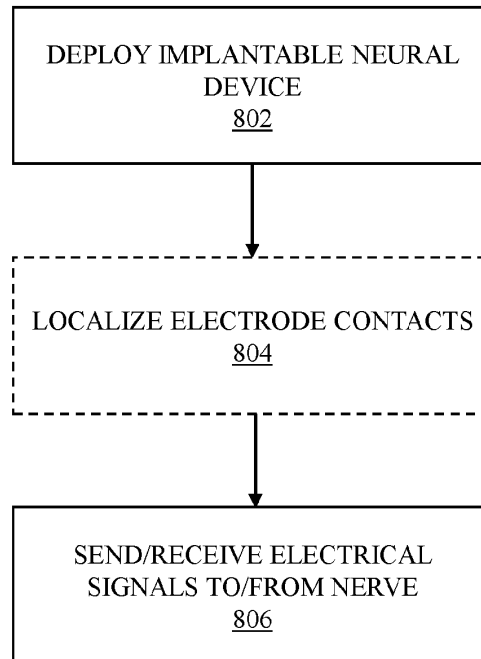
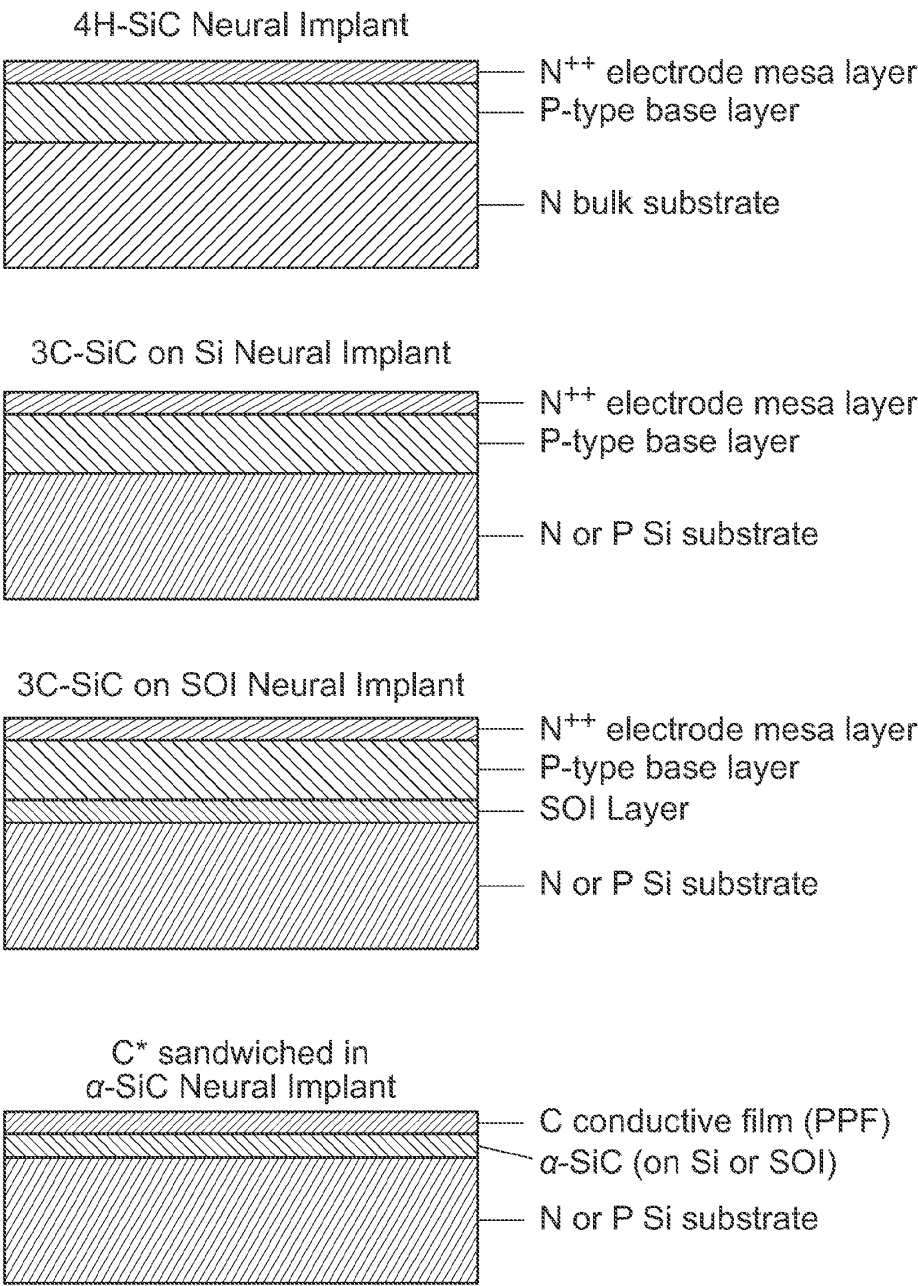
800 

FIG. 9

SiC Neural Interface Options
Layers needed to make device



C* layer can be replaced with heavily doped polycrystalline SiC

FIG. 10

SiC Neural Interface Options
Etch definition of conductive mesa

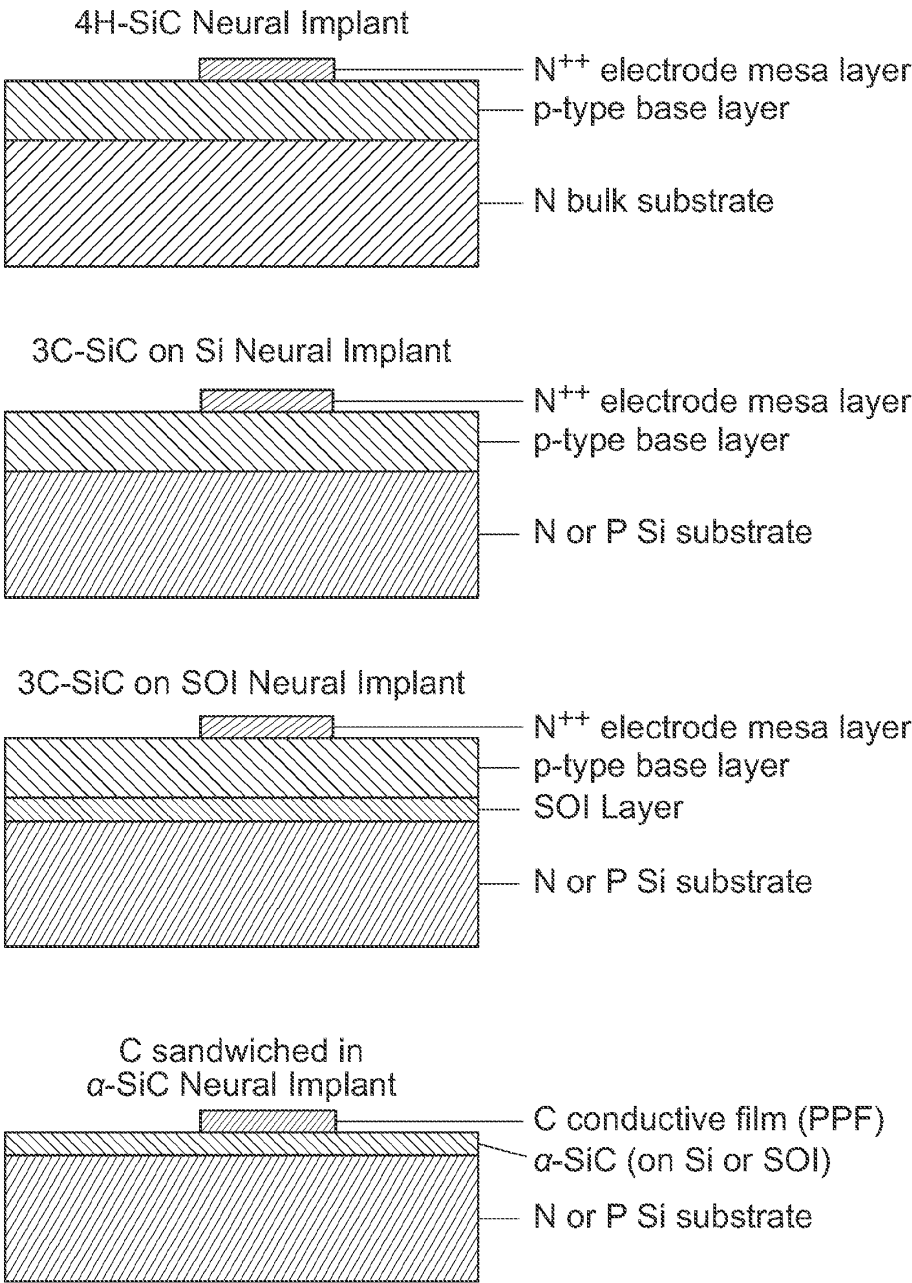


FIG. 11

SiC Neural Interface Options
 α -SiC insulator coating and device thinning

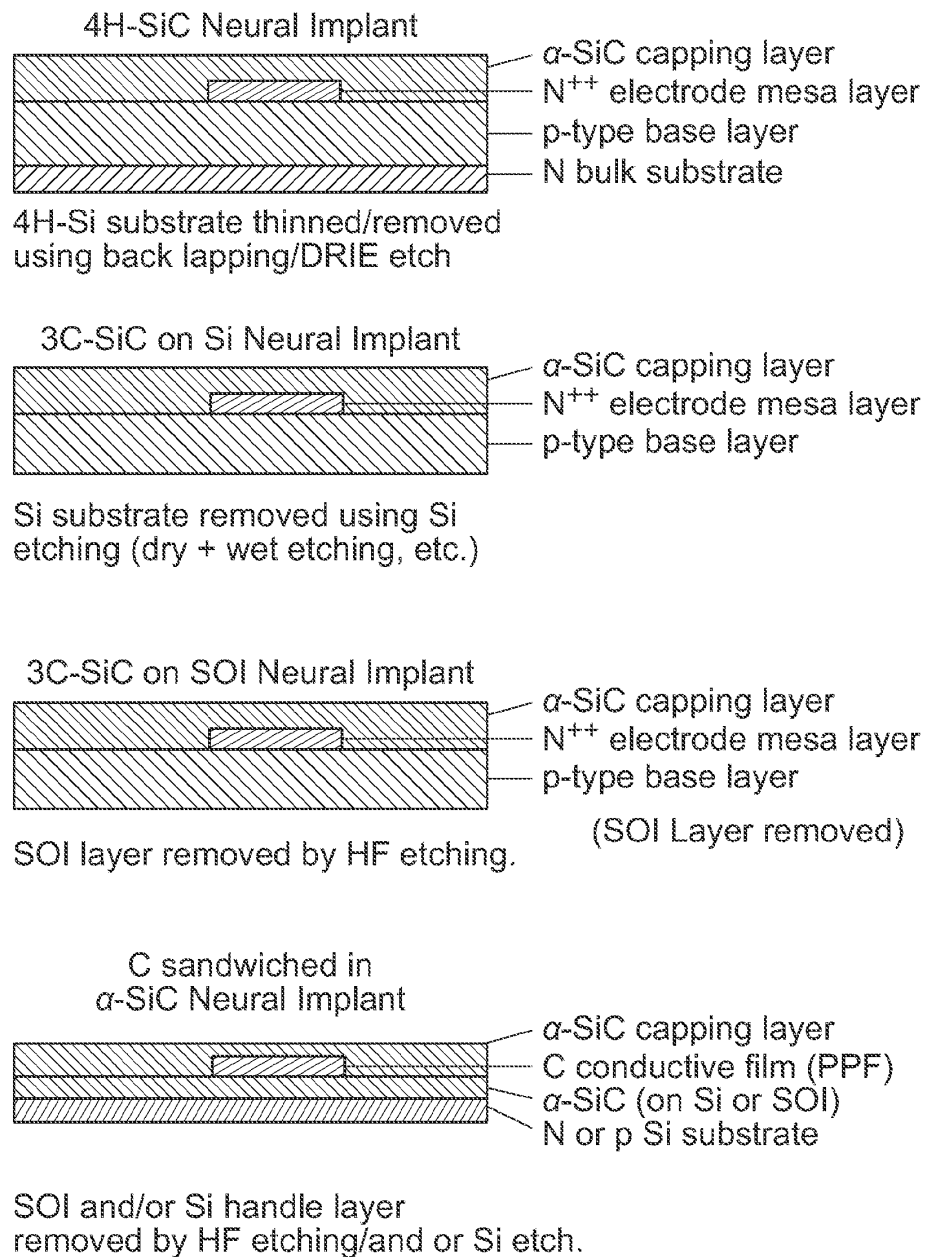
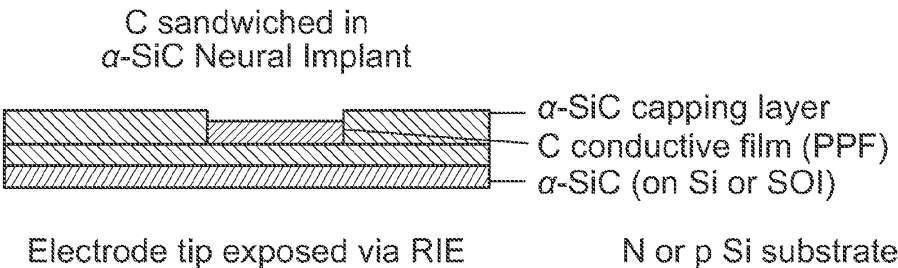
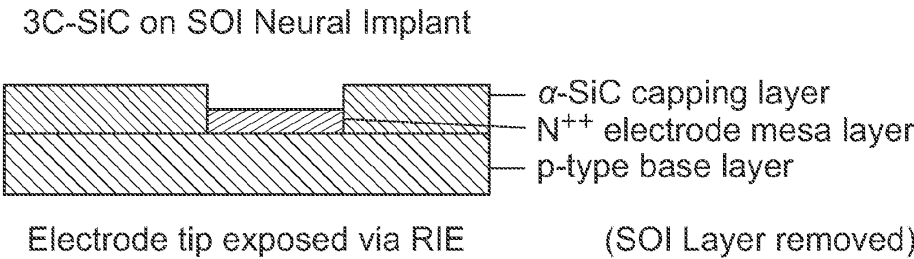
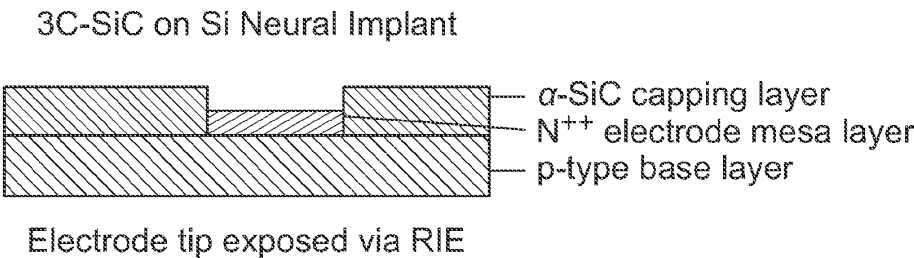
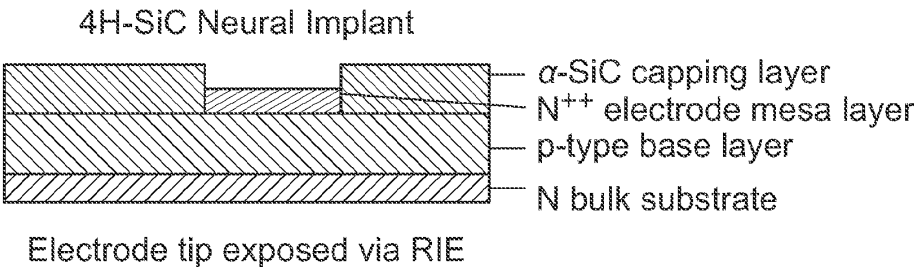


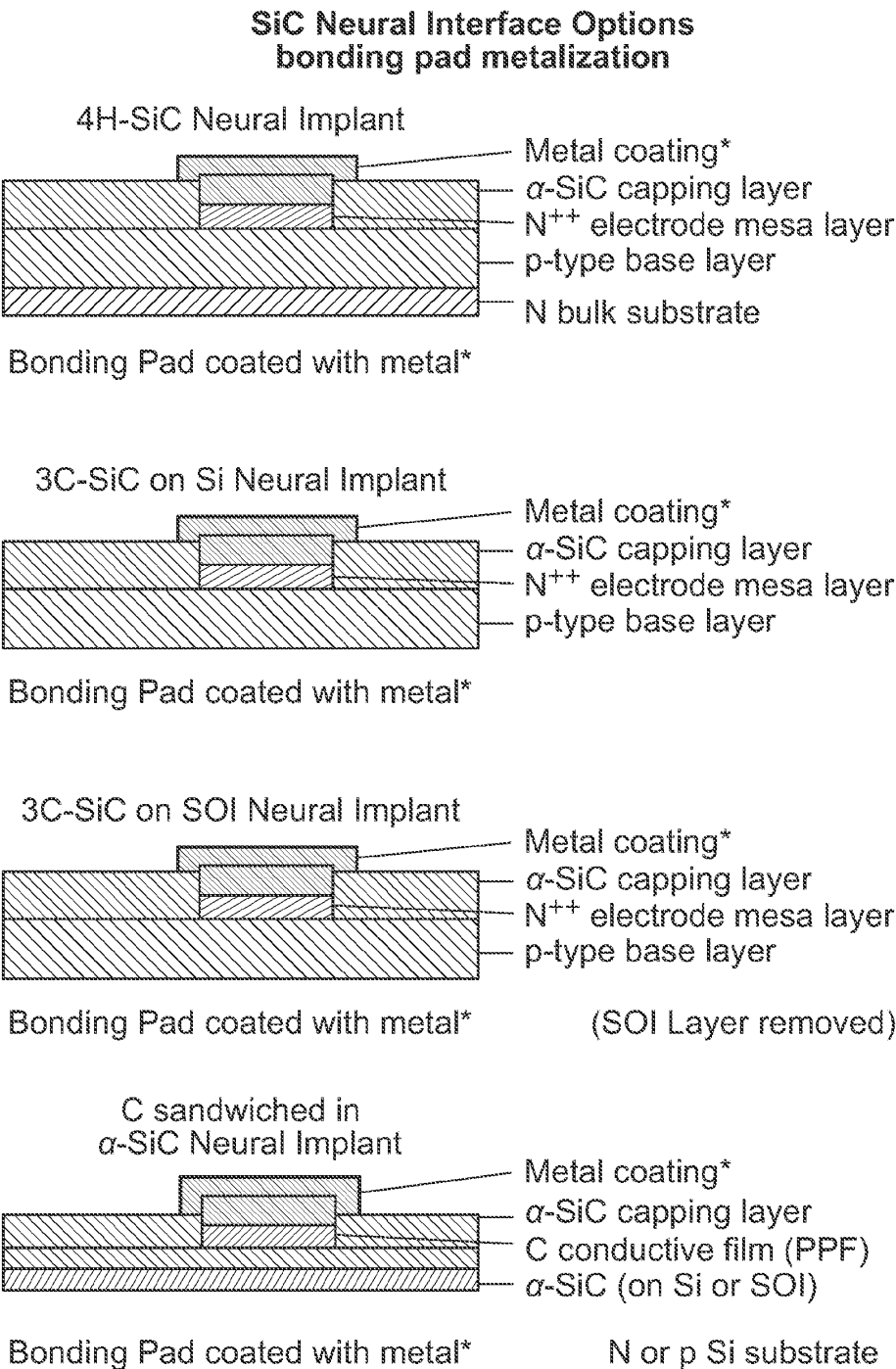
FIG. 12

SiC Neural Interface Options
Insulator window etch*: bonding pads and recording tip**



* RIE (reactive ion etching) step done before wafer thinning
** Bonding pads not shown here, only recording tip window

FIG. 13



* Typically Ti/Au or similar layers. Ti layer facilitates metal adhesion to SiC while Au is the conducting layer to facilitate packaging

FIG. 14