WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a first stack structure and a second stack structure on a semiconductor substrate;

a first vertical structure having a sidewall in contact with the first stack structure, the first vertical structure including a first memory layer and a first channel pattern;

a second vertical structure having a sidewall in contact with the second stack structure, the second vertical structure including a second memory layer and a second channel pattern;

a first bit line contact structure on the first vertical structure; and

a first bit line overlapping with the first bit line contact structure,

wherein each of the first stack structure and the second stack structure includes conductive layers stacked on the semiconductor substrate to be spaced vertically apart from each other,

wherein the first bit line contact structure has a shape which is widened toward the first bit line, and

wherein the first bit line contact structure is a portion of the first channel pattern which protrudes the first stack structure.

2. The semiconductor memory device of claim 1, wherein the first stack structure includes first conductive layers of the conductive layers stacked on the semiconductor substrate to be spaced vertically apart from each other, and

the second stack structure includes second conductive layers of the conductive layers stacked on the semiconductor substrate to be spaced vertically apart from each other, and

wherein the first conductive layers and the second conductive layers are disposed at the same level.

3. The semiconductor memory device of claim 1, further comprising an isolation insulating layer disposed between the first stack structure and the second stack structure.

4. The semiconductor memory device of claim 1, further comprising:

a first isolation structure disposed between the first memory layer and the second memory layer; and

a second isolation structure disposed between the first channel pattern and the second channel pattern.

5. The semiconductor memory device of claim 1, wherein the first bit line contact structure extends from the first channel pattern to protrude beyond the first stack structure.

6. The semiconductor memory device of claim 1, further comprising an upper contact disposed between the first bit line contact structure and the first bit line.

7. The semiconductor memory device of claim 1, wherein the first stack structure includes a first cell stack structure and a first select stack structure, and

the second stack structure includes a second cell stack structure and a second select stack structure, and

wherein the semiconductor memory device further comprises an isolation structure disposed between the first select stack structure and the second select stack structure.

8. The semiconductor memory device of claim 7, further comprising a dummy vertical structure penetrating the first stack structure or the second stack structure.

9. A semiconductor memory device comprising:

a first stack structure and a second stack structure on a semiconductor substrate;

a first vertical structure having a sidewall in contact with the first stack structure, the first vertical structure including a first memory layer and a first channel pattern;

a second vertical structure having a sidewall in contact with the first stack structure, the second vertical structure including a second memory layer and a second channel pattern;

a third vertical structure having a sidewall in contact with the

second stack structure, the third vertical structure including a third memory layer and a third channel pattern;

a fourth vertical structure having a sidewall in contact with the second stack structure, the fourth vertical structure including a fourth memory layer and a fourth channel pattern;

a first bit line contact structure on the first vertical structure; and

a first bit line overlapping with the first bit line contact structure,

wherein each of the first stack structure and the second stack structure includes conductive layers stacked on the semiconductor substrate to be spaced vertically apart from each other,

wherein the first bit line contact structure has a shape which is widened toward the first bit line, and

wherein the first bit line contact structure is a portion of the first channel pattern which protrudes the first stack structure.

10. The semiconductor memory device of claim 9, further comprising an isolation insulating layer disposed between the first stack structure and the second stack structure.

11. The semiconductor memory device of claim 9, further comprising:

a first isolation structure disposed between the first memory layer and the second memory layer; and

a second isolation structure disposed between the first channel

pattern and the second channel pattern.

12. The semiconductor memory device of claim 9, further comprising an upper contact disposed between the first bit line contact structure and the first bit line.

13. The semiconductor memory device of claim 9, wherein the first bit line contact structure extends from the first channel pattern to protrude beyond the first stack structure.

14. A semiconductor memory device comprising:

a first stack structure and a second stack structure on a semiconductor substrate;

a first vertical structure having a sidewall in contact with the first stack structure, the first vertical structure including a first memory layer and a first channel pattern extending vertically away from the semiconductor substrate;

a second vertical structure having a sidewall in contact with the second stack structure, the second vertical structure including a second memory layer and a second channel pattern extending vertically away from the semiconductor substrate;

a bit line contact structure on the first vertical structure; and

a bit line overlapping with the bit line contact structure,

wherein the first channel pattern is isolated into first separate

channel patterns by vertically extending isolation layers disposed against the sidewall of the first vertical structure,

wherein the second channel pattern is isolated into second separate channel patterns by vertically extending isolation layers disposed against the sidewall of the second vertical structure,

wherein the bit line contact structure contacts one of the first separate channel patterns, and

wherein the first bit line contact structure is a portion of the first channel pattern which protrudes the first stack structure.

15. The semiconductor memory device of claim 14, wherein the first memory layer is disposed on the sidewall of the first vertical structure and extends vertically away from the semiconductor substrate.

16. The semiconductor memory device of claim 15, wherein the first channel pattern and the first memory layer have a cylindrical shape penetrating the first stack structure.

17. The semiconductor memory device of claim 14, wherein each of the first stack structure and the second stack structure includes conductive layers stacked on the semiconductor substrate to be spaced vertically from each other.

18. The semiconductor memory device of claim 14, wherein the

bit line contact structure has a shape which is widened toward the bit line.