

ABSTRACT

A non-volatile semiconductor memory device is proposed whereby voltage can be more flexibly set in accumulating electric charges into a selected memory cell transistor in comparison with a conventional device. In a non-volatile semiconductor memory device (1), when a selected memory cell transistor (115) is caused to accumulate electric charges, high voltage as writing prevention voltage is applied from a PMOS transistor (9b) while low voltage as writing voltage is applied from an NMOS transistor (15a). Thus, a role of applying voltage to either the selected memory cell transistor (115) or a non-selected memory cell transistor (116) is shared by the PMOS transistor (9b) and the NMOS transistor (15a). Therefore, the gate voltage and the source voltage of the PMOS transistor (9b) and those of the NMOS transistor (15a) can be separately adjusted, and gate-to-substrate voltage thereof can be finally set to be, for instance, 4[V] or etc.