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(21) International Application Number: PCT/US96/19658 (22) International Filing Date: 11 December 1996 (11.12.96) (30) Priority Data: 08/575,663 19 December 1995 (19.12.95) US (71) Applicant (for all designated States except US): INTEL CORPORATION [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95052 (US). (72) Inventors; and (75) Inventors/Applicants (for US only): GILLESPIE, Byron [US/US]; 3730 E. Rockwood Drive, Phoenix, AZ 85024 (US). GARBUS, Elliot [US/US]; 2700 N. Hayden Road #3106, Scottsdale, AZ 85257 (US). FUTRAL, William [US/US]; 17715 N.E. Elk Run Drive, Portland, OR 97229 (US). (74) Agents: TAYLOR, Edwin, H. et al.; Blakely, Sokoloff, Taylor & Zafman L.L.P., 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025 (US).		(81) Designated States: AL, AM, AT, AT (Utility model), AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, CZ (Utility model), DE, DE (Utility model), DK, DK (Utility model), EE, EE (Utility model), ES, FI, FI (Utility model), GB, GE, HU, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SK (Utility model), TJ, TM, TR, TT, UA, UG, US, UZ, VN, ARIPO patent (KE, LS, MW, SD, SZ, UG), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG). Published <i>With international search report.</i>
(54) Title: METHOD AND APPARATUS FOR DYNAMIC APPENDING OF DIRECT MEMORY ACCESS CHAIN DESCRIPTORS		
(57) Abstract Computer system (100) having host processor (102), DMA unit (104), host memory (106) and external memory (108) wherein DMA unit (104) controls transference of data between host memory (106) and external memory (108) based upon data transference parameters specified in chain descriptors created by host processor (102) and stored as data structures within host memory (106). Dynamic appending of chain descriptors is achieved by employing resume bit stored within register (10) of DMA unit (104). Host processor (102), upon creating new group of chain descriptors to be appended to previous group, updates link value within last chain descriptor for the previous group to point to the first chain descriptor of the new group and also sets the resume bit. DMA unit (104) reads chain descriptor parameters, including link values, they perform data transfer operation specified by the chain descriptor parameters. Upon completion of the transfer operation, DMA unit (104) examines the resume bit, and, if set, DMA unit (104) rereads the link value for the current chain descriptor.		