SEMICONDUCTOR DEVICE HAVING AN INTERCONNECT STRUCTURE WITH TSV USING ENCAPSULANT FOR STRUCTURAL SUPPORT

Field of the Invention

The present invention relates in general to semiconductor devices and, more particularly, to a semiconductor device and method of forming an interconnect structure with a through silicon via using an encapsulant for structural support.

Background of the Invention

Semiconductor devices are commonly found in modern electronic products. Semiconductor devices vary in the number and density of electrical components. Discrete semiconductor devices generally contain one type of electrical component, e.g., light emitting diode (LED), small signal transistor, resistor, capacitor, inductor, and power metal oxide semiconductor field effect transistor (MOSFET). Integrated semiconductor devices typically contain hundreds to millions of electrical components. Examples of integrated semiconductor devices include microcontrollers, microprocessors, charged-coupled devices (CCDs), solar cells, and digital micro-mirror devices (DMDs).

Semiconductor devices perform a wide range of functions such as high-speed calculations, transmitting and receiving electromagnetic signals, controlling electronic devices, transforming sunlight to electricity, and creating visual projections for television displays. Semiconductor devices are found in the fields of entertainment, communications, power conversion, networks, computers, and consumer products. Semiconductor devices are also found in military applications, aviation, automotive, industrial controllers, and office equipment.

Semiconductor devices exploit the electrical properties of semiconductor materials. The atomic structure of semiconductor material allows its electrical conductivity to be manipulated by the application of an electric field or through the process of doping. Doping introduces impurities into the semiconductor material to manipulate and control the conductivity of the semiconductor device.

A semiconductor device contains active and passive electrical structures. Active structures, including bipolar and field effect transistors, control the flow of electrical current. By varying levels of doping and application of an electric field or base current, the transistor either promotes or restricts the flow of electrical current. Passive structures, including resistors, capacitors, and inductors, create a relationship between voltage and current necessary to perform a variety of electrical functions. The passive and active structures are electrically connected to form circuits, which enable the semiconductor device to perform high-speed calculations and other useful functions.

Semiconductor devices are generally manufactured using two complex manufacturing processes, i.e., front-end

manufacturing, and back-end manufacturing, each involving potentially hundreds of steps. Front-end manufacturing involves the formation of a plurality of die on the surface of a semiconductor wafer. Each die is typically identical and contains circuits formed by electrically connecting active and passive components. Back-end manufacturing involves singulating individual die from the finished wafer and packaging the die to provide structural support and environmental isolation.

One goal of semiconductor manufacturing is to produce smaller semiconductor devices. Smaller devices typically consume less power, have higher performance, and can be produced more efficiently. In addition, smaller semiconductor devices have a smaller footprint, which is desirable for smaller end products. A smaller die size may be achieved by improvements in the front-end process resulting in die with smaller, higher density active and passive components. Back-end processes may result in semiconductor device packages with a smaller footprint by improvements in electrical interconnection and packaging materials.

The electrical interconnection between the semiconductor package containing semiconductor devices on multiple levels (3-D device integration) and an external printed circuit board (PCB) or substrate is typically accomplished with wire bonds, through hole vias (THV), or through silicon vias (TSV). Wire bonds require additional package area to form the bend in the leads. To make electrical interconnect using THVs or TSVs, a temporary carrier is bonded to the package substrate for structural support while forming the THVs and TSVs. For thin wafers, e.g., less than 250 micrometers (μm), excessive handling can lead to breakage and slippage. The temporary carrier adds manufacturing costs. The bonding material for the

temporary carrier limits processing temperatures to about 200°C.

Summary of the Invention

In one embodiment, the present invention is a semiconductor device comprising a substrate and via extending through the substrate. A first insulating layer is disposed on sidewalls of the via. An electrically conductive material is disposed in the via over the first insulating layer to form a conductive TSV. A first interconnect structure is disposed over a first side of the substrate. A semiconductor die or a component is mounted to the first interconnect structure. An encapsulant is disposed over the first interconnect structure and semiconductor die or component. A second interconnect structure is disposed over the second side of the substrate. The second interconnect structure is electrically connected to the TSV.

In another embodiment, the present invention is a semiconductor device comprising a substrate and a via disposed through the substrate. An electrically conductive material is disposed in the via to form a conductive via. A first interconnect structure is disposed over a first side of the substrate. A semiconductor die or a component is mounted to the first interconnect structure. An encapsulant is deposited over the first interconnect structure and semiconductor die or component. A second interconnect structure is disposed over the second side of the substrate. The second interconnect structure is electrically connected to the conductive via.

In still another embodiment, the present invention is a semiconductor device comprising a substrate and a conductive via disposed through the substrate. A first interconnect

structure is disposed over a first side of the substrate. A semiconductor die or component is mounted to the first interconnect structure. An encapsulant is disposed over the first interconnect structure and the semiconductor die or component.

In yet another embodiment, the present invention is a semiconductor device comprising a substrate and a conductive via disposed through the substrate. A first interconnect structure is disposed over a first side of the substrate. A semiconductor component is mounted to the first interconnect structure. An encapsulant is disposed over the first interconnect structure and the semiconductor component.

Brief Description of the Drawings

FIG. 1 illustrates a PCB with different types of packages mounted to its surface;

FIGs. 2a-2c illustrate further detail of the representative semiconductor packages mounted to the PCB;

FIGs. 3a-3h illustrate a method of forming an interconnect structure with TSV for 3-D devices using an encapsulant for structural support; and

FIGs. 4a-4d illustrate a method of forming an interconnect structure with TSV and backside RDL for 3-D devices using an encapsulant for structural support.

Detailed Description of the Drawings

The present invention is described in one or more embodiments in the following description with reference to the figures, in which like numerals represent the same or similar

elements. While the invention is described in terms of the best mode for achieving the invention's objectives, it will be appreciated by those skilled in the art that it is intended to cover alternatives, modifications, and equivalents as may be included within the spirit and scope of the invention as defined by the appended claims and their equivalents as supported by the following disclosure and drawings.

Semiconductor devices are generally manufactured using two complex manufacturing processes: front-end manufacturing and back-end manufacturing. Front-end manufacturing involves the formation of a plurality of die on the surface of a semiconductor wafer. Each die on the wafer contains active and passive electrical components, which are electrically connected to form functional electrical circuits. Active electrical components, such as transistors and diodes, have the ability to control the flow of electrical current. Passive electrical components, such as capacitors, inductors, resistors, and transformers, create a relationship between voltage and current necessary to perform electrical circuit functions.

Passive and active components are formed over the surface of the semiconductor wafer by a series of process steps including doping, deposition, photolithography, etching, and planarization. Doping introduces impurities into the semiconductor material by techniques such as ion implantation or thermal diffusion. The doping process modifies the electrical conductivity of semiconductor material in active devices, transforming the semiconductor material into an insulator, conductor, or dynamically changing the semiconductor material conductivity in response to an electric field or base current. Transistors contain regions of varying types and degrees of doping arranged as necessary to enable the transistor to promote

or restrict the flow of electrical current upon the application of the electric field or base current.

Active and passive components are formed by layers of materials with different electrical properties. The layers can be formed by a variety of deposition techniques determined in part by the type of material being deposited. For example, thin film deposition may involve chemical vapor deposition (CVD), physical vapor deposition (PVD), electrolytic plating, and electroless plating processes. Each layer is generally patterned to form portions of active components, passive components, or electrical connections between components.

The layers can be patterned using photolithography, which involves the deposition of light sensitive material, e.g., photoresist, over the layer to be patterned. A pattern is transferred from a photomask to the photoresist using light. The portion of the photoresist pattern subjected to light is removed using a solvent, exposing portions of the underlying layer to be patterned. The remainder of the photoresist is removed, leaving behind a patterned layer. Alternatively, some types of materials are patterned by directly depositing the material into the areas or voids formed by a previous deposition/etch process using techniques such as electroless and electrolytic plating.

Depositing a thin film of material over an existing pattern can exaggerate the underlying pattern and create a non-uniformly flat surface. A uniformly flat surface is required to produce smaller and more densely packed active and passive components. Planarization can be used to remove material from the surface of the wafer and produce a uniformly flat surface. Planarization involves polishing the surface of the wafer with a polishing pad. An abrasive material and corrosive chemical are

added to the surface of the wafer during polishing. The combined mechanical action of the abrasive and corrosive action of the chemical removes any irregular topography, resulting in a uniformly flat surface.

Back-end manufacturing refers to cutting or singulating the finished wafer into the individual die and then packaging the die for structural support and environmental isolation. To singulate the die, the wafer is scored and broken along non-functional regions of the wafer called saw streets or scribes. The wafer is singulated using a laser cutting tool or saw blade. After singulation, the individual die are mounted to a package substrate that includes pins or contact pads for interconnection with other system components. Contact pads formed over the semiconductor die are then connected to contact pads within the package. The electrical connections can be made with solder bumps, stud bumps, conductive paste, or wirebonds. An encapsulant or other molding material is deposited over the package to provide physical support and electrical isolation. The finished package is then inserted into an electrical system and the functionality of the semiconductor device is made available to the other system components.

FIG. 1 illustrates electronic device 50 having a chip carrier substrate or PCB 52 with a plurality of semiconductor packages mounted on its surface. Electronic device 50 may have one type of semiconductor package, or multiple types of semiconductor packages, depending on the application. The different types of semiconductor packages are shown in FIG. 1 for purposes of illustration.

Electronic device 50 may be a stand-alone system that uses the semiconductor packages to perform one or more electrical functions. Alternatively, electronic device 50 may

be a subcomponent of a larger system. For example, electronic device 50 may be a graphics card, network interface card, or other signal processing card that can be inserted into a computer. The semiconductor package can include microprocessors, memories, application specific integrated circuits (ASICs), logic circuits, analog circuits, RF circuits, discrete devices, or other semiconductor die or electrical components.

In FIG. 1, PCB 52 provides a general substrate for structural support and electrical interconnect of the semiconductor packages mounted on the PCB. Conductive signal traces 54 are formed over a surface or within layers of PCB 52 using evaporation, electrolytic plating, electroless plating, screen printing, or other suitable metal deposition process. Signal traces 54 provide for electrical communication between each of the semiconductor packages, mounted components, and other external system components. Traces 54 also provide power and ground connections to each of the semiconductor packages.

In some embodiments, a semiconductor device has two packaging levels. First level packaging is a technique for mechanically and electrically attaching the semiconductor die to an intermediate carrier. Second level packaging involves mechanically and electrically attaching the intermediate carrier to the PCB. In other embodiments, a semiconductor device may only have the first level packaging where the die is mechanically and electrically mounted directly to the PCB.

For the purpose of illustration, several types of first level packaging, including wire bond package 56 and flip chip 58, are shown on PCB 52. Additionally, several types of second level packaging, including ball grid array (BGA) 60, bump chip carrier (BCC) 62, dual in-line package (DIP) 64, land grid

array (LGA) 66, multi-chip module (MCM) 68, quad flat non-leaded package (QFN) 70, and quad flat package 72, are shown mounted on PCB 52. Depending upon the system requirements, any combination of semiconductor packages, configured with any combination of first and second level packaging styles, as well as other electronic components, can be connected to PCB 52. In some embodiments, electronic device 50 includes a single attached semiconductor package, while other embodiments call for multiple interconnected packages. By combining one or more semiconductor packages over a single substrate, manufacturers can incorporate pre-made components into electronic devices and systems. Because the semiconductor packages include sophisticated functionality, electronic devices can be manufactured using cheaper components and a streamlined manufacturing process. The resulting devices are less likely to fail and less expensive to manufacture resulting in a lower cost for consumers.

FIGs. 2a-2c show exemplary semiconductor packages. FIG. 2a illustrates further detail of DIP 64 mounted on PCB 52. Semiconductor die 74 includes an active region containing analog or digital circuits implemented as active devices, passive devices, conductive layers, and dielectric layers formed within the die and are electrically interconnected according to the electrical design of the die. For example, the circuit may include one or more transistors, diodes, inductors, capacitors, resistors, and other circuit elements formed within the active region of semiconductor die 74. Contact pads 76 are one or more layers of conductive material, such as aluminum (Al), copper (Cu), tin (Sn), nickel (Ni), gold (Au), or silver (Ag), and are electrically connected to the circuit elements formed within semiconductor die 74. During assembly of DIP 64, semiconductor die 74 is mounted to an intermediate carrier 78 using a gold-

silicon eutectic layer or adhesive material such as thermal epoxy. The package body includes an insulative packaging material such as polymer or ceramic. Conductor leads 80 and wire bonds 82 provide electrical interconnect between semiconductor die 74 and PCB 52. Encapsulant 84 is deposited over the package for environmental protection by preventing moisture and particles from entering the package and contaminating die 74 or wire bonds 82.

FIG. 2b illustrates further detail of BCC 62 mounted on PCB 52. Semiconductor die 88 is mounted over carrier 90 using an underfill or epoxy-resin adhesive material 92. Wire bonds 94 provide first level packing interconnect between contact pads 96 and 98. Molding compound or encapsulant 100 is deposited over semiconductor die 88 and wire bonds 94 to provide physical support and electrical isolation for the device. Contact pads 102 are formed over a surface of PCB 52 using a suitable metal deposition such electrolytic plating or electroless plating to prevent oxidation. Contact pads 102 are electrically connected to one or more conductive signal traces 54 in PCB 52. Bumps 104 are formed between contact pads 98 of BCC 62 and contact pads 102 of PCB 52.

In FIG. 2c, semiconductor die 58 is mounted face down to intermediate carrier 106 with a flip chip style first level packaging. Active region 108 of semiconductor die 58 contains analog or digital circuits implemented as active devices, passive devices, conductive layers, and dielectric layers formed according to the electrical design of the die. For example, the circuit may include one or more transistors, diodes, inductors, capacitors, resistors, and other circuit elements within active region 108. Semiconductor die 58 is electrically and mechanically connected to carrier 106 through bumps 110.

BGA 60 is electrically and mechanically connected to PCB 52 with a BGA style second level packaging using bumps 112. Semiconductor die 58 is electrically connected to conductive signal traces 54 in PCB 52 through bumps 110, signal lines 114, and bumps 112. A molding compound or encapsulant 116 is deposited over semiconductor die 58 and carrier 106 to provide physical support and electrical isolation for the device. The flip chip semiconductor device provides a short electrical conduction path from the active devices on semiconductor die 58 to conduction tracks on PCB 52 in order to reduce signal propagation distance, lower capacitance, and improve overall circuit performance. In another embodiment, the semiconductor die 58 can be mechanically and electrically connected directly to PCB 52 using flip chip style first level packaging without intermediate carrier 106.

FIGs. 3a-3h illustrate a process of forming an interconnect structure with a conductive via for 3-D devices using an encapsulant for structural support. In FIG. 3a, a semiconductor wafer 118 contains a substrate made with a base material such as silicon, polymer, polymer composite, metal, ceramic, glass, glass epoxy, beryllium oxide, or other suitable low-cost, rigid material for structural support. Alternatively, the substrate can be a semiconductor base material such as germanium, gallium arsenide, indium phosphide, or silicon carbide. A plurality of semiconductor die can be formed on the substrate using semiconductor manufacturing processes such as described above. Each semiconductor die includes an active region 120 containing analog or digital circuits implemented as active devices, passive devices, conductive layers, and dielectric layers formed within the die and electrically interconnected according to the electrical design and function

of the die. For example, the circuit may include one or more transistors, diodes, and other circuit elements formed within active surface 120 to implement baseband analog circuits or digital circuits, such as digital signal processor (DSP), ASIC, memory, or other signal processing circuit. The semiconductor die may also contain integrated passive devices (IPD), such as inductors, capacitors, and resistors, for radio frequency (RF) signal processing.

The IPDs contained within semiconductor wafer 118 provide the electrical characteristics needed for high frequency applications, such as resonators, high-pass filters, low-pass filters, band-pass filters, symmetric Hi-Q resonant transformers, matching networks, and tuning capacitors. The IPDs can be used as front-end wireless RF components, which can be positioned between the antenna and transceiver. The inductor can be a hi-Q balun, transformer, or coil, operating up to 100 Gigahertz. In some applications, multiple baluns are formed on a same substrate, allowing multi-band operation. For example, two or more baluns are used in a quad-band for mobile phones or other global system for mobile (GSM) communications, each balun dedicated for a frequency band of operation of the quad-band device. A typical RF system requires multiple IPDs and other high frequency circuits in one or more semiconductor packages to perform the necessary electrical functions.

A plurality of vias is formed in semiconductor wafer 118 using laser drilling or etching process, such as deep reactive ion etching (DRIE). An insulating layer 121 is formed to line the sidewalls and bottom of the vias. The insulating layer 121 can be one or more layers of silicon dioxide (SiO2), silicon nitride (Si3N4), silicon oxynitride (SiON), tantalum pentoxide (Ta2O5), aluminum oxide (Al2O3), polyimide,

benzocyclobutene (BCB), polybenzoxazoles (PBO), or other suitable dielectric material. The insulating layer 121 is formed using PVD, CVD, or thermal oxidation.

An electrically conductive material 122 is deposited in the vias over insulating layer 121 using PVD, CVD, sputtering, electrolytic plating, electroless plating process, or other suitable metal deposition process. Conductive material 122 can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, W, poly-silicon, or other suitable electrically conductive material. Conductive material 122 in the vias functions as conductive TSV.

In FIG. 3b, an electrically conductive layer 124 is formed over TSVs 122 and semiconductor wafer 118 using PVD, CVD, sputtering, electrolytic plating, electroless plating process, or other suitable metal deposition process. Conductive layer 124 can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. The individual portions of conductive layer 124 can be electrically common or electrically isolated depending on the function of the semiconductor device.

An insulating or passivation layer 126 is formed on conductive layer 124 and active surface 120 of semiconductor wafer 118. The insulating layer 126 can be one or more layers of SiO_2, Si_3N_4, SiON, Ta_2O_5, Al_2O_3, or other material having similar insulating properties. The insulating layer 126 is formed using PVD, CVD, printing, spin coating, spray coating, sintering, or thermal oxidation. A portion of insulating layer 126 is removed by an etching process to expose conductive layer 124.

An electrically conductive layer 128 is formed over conductive layer 124 and insulating layer 126 using PVD, CVD,

sputtering, electrolytic plating, electroless plating process, or other suitable metal deposition process. Conductive layer 128 can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. The individual portions of conductive layer 128 can be electrically common or electrically isolated depending on the function of the semiconductor device.

An insulating or passivation layer 130 is formed on conductive layer 128 and insulating layer 126. The insulating layer 130 can be one or more layers of SiO_2, Si_3N_4, SiON, Ta_2O_5, Al_2O_3, or other material having similar insulating properties. The insulating layer 130 is formed using PVD, CVD, printing, spin coating, spray coating, sintering, or thermal oxidation. A portion of insulating layer 130 is removed by plasma or chemical etching process to expose conductive layer 128.

Conductive pillars or posts 132 are formed over conductive layer 128. Conductive pillars 132 can be Cu, Al, W, Au, solder, or other suitable electrically conductive material. In one embodiment, the conductive pillars 132 can be Cu and formed by a plating process. A thick layer of photoresist is deposited over insulating layer 130 and conductive layer 128. The photoresist can be a liquid or a dry film with a thickness of 15 to 130 μm. Two layers of photoresist may be applied to achieve the desired thickness. In one embodiment, conductive pillars have a height of 2-120 μm. The photoresist is patterned using photolithography. Cu is deposited in the patterned areas of the photoresist using electrolytic plating. The photoresist is stripped away leaving behind individual conductive pillars 132. In another embodiment, solder balls or stud bumps can be formed over conductive layer 128.

An insulating or passivation layer 134 is formed

around conductive pillars 132. The insulating layer 134 can be one or more layers of SiO2, Si3N4, SiON, Ta2O5, Al2O3, or other material having similar insulating properties. The insulating layer 134 is formed using PVD, CVD, printing, spin coating, spray coating, sintering, or thermal oxidation. A portion of insulating layer 134 is removed by an etching process to expose conductive pillar 132.

In FIG. 3c, an electrically conductive layer 136 is formed over conductive pillars 132 using PVD, CVD, sputtering, electrolytic plating, electroless plating process, or other suitable metal deposition process. Conductive layer 136 can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. Conductive layer 136 is an under bump metallization (UBM) in electrical contact with conductive pillar 132. UBM 136 can be a multi-metal stack with adhesion layer, barrier layer, and seed or wetting layer. The adhesion layer is formed over conductive pillar 132 and can be Ti, titanium nitride (TiN), titanium tungsten (TiW), Al, or chromium (Cr). The barrier layer is formed over the adhesion layer and can be made of Ni, nickel vanadium (NiV), platinum (Pt), palladium (Pd), TiW, or chromium copper (CrCu). The barrier layer inhibits the diffusion of Cu into the active area of the die. The seed layer can be Cu, Ni, NiV, Au, or Al. The seed layer is formed over the barrier layer and acts as an intermediate conductive layer between conductive pillar 132 and subsequent bumps or other interconnect structure. UBM 136 provides a low resistive interconnect to conductive pillar 132, as well as a barrier to solder diffusion and seed layer for solder wettability.

An electrically conductive material is deposited over UBM 136 using an evaporation, electrolytic plating, electroless

plating, ball drop, or screen printing process. The conductive material can be Al, Sn, Ni, Au, Ag, Pb, Bi, Cu, solder, and combinations thereof, with an optional flux material. For example, the conductive material can be eutectic Sn/Pb, high-lead solder, or lead-free solder. The conductive material is bonded to UBM 136 using a suitable attachment or bonding process. In one embodiment, the conductive material is reflowed by heating the material above its melting point to form spherical balls or bumps 138. In some applications, bumps 138 are reflowed a second time to improve electrical contact to UBM 136. The bumps can also be compression bonded to UBM 136. Bumps 138 represent one type of interconnect structure that can be formed over UBM 136. The interconnect structure can also use bond wires, conductive paste, stud bump, micro bump, or other electrical interconnect.

Semiconductor die 140 each have contact pads 142 metallurgically and electrically connected to bumps 138. Each semiconductor die 140 includes a substrate with an active region containing analog or digital circuits implemented as active devices, passive devices, conductive layers, and dielectric layers formed within the die and electrically interconnected according to the electrical design and function of the die. The semiconductor die may also contain IPD for RF signal processing. A passive device or component 144 is structurally and electrically connected to UBM 136 using bonds 146. Semiconductor die 140 and passive device 144, in combination with the IPD formed in active region 120, provide a 3-D semiconductor structure.

The semiconductor device is encapsulated to protect the device and provide robust structural support during formation of additional interconnect structures. FIG. 3d shows

an encapsulant or molding compound 150 deposited over the structure described in FIG. 3c using a paste printing, compressive molding, transfer molding, liquid encapsulant molding, or other suitable applicator. Encapsulant 150 can be epoxy resin, epoxy acrylate, polymer, or polymer composite material. Encapsulant 150 is non-conductive and environmentally protects the semiconductor device from external elements and contaminants.

In FIG. 3e, semiconductor wafer 118 is inverted and back surface 152 is reduced in thickness by mechanical grinding, CMP, wet etching, dry etching, plasma etching, or another thinning process. Since semiconductor wafer 118 is covered with encapsulant 150, the structure is sufficiently robust to reduce substrate thickness to less than 300 μm. In one embodiment, the thickness of the substrate is reduced to 10-50 μm. A temporary carrier or tape is not needed because encapsulant 150 provides the support to maintain the structural integrity of the device, even with the reduced substrate thickness.

In FIG. 3f, an insulating or passivation layer 154 is formed over back surface 152 and TSVs 122. The insulating layer 154 can be one or more layers of SiO_2, Si_3N_4, SiON, Ta_2O_5, Al_2O_3, or other material having similar insulating properties. The insulating layer 154 is formed using PVD, CVD, printing, spin coating, spray coating, sintering, or thermal oxidation. A portion of insulating layer 154 is removed by an etching process to expose TSVs 122.

An electrically conductive layer 156 is formed over TSVs 122 and insulating layer 154 using PVD, CVD, sputtering, electrolytic plating, electroless plating process, or other suitable metal deposition process. Conductive layer 156 can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable

electrically conductive material. Conductive layer 156 is a UBM in electrical contact with TSVs 122.

In FIG. 3g, an electrically conductive material is deposited over UBM 156 using an evaporation, electrolytic plating, electroless plating, ball drop, or screen printing process. The conductive material can be Al, Sn, Ni, Au, Ag, Pb, Bi, Cu, solder, and combinations thereof, with an optional flux material. For example, the conductive material can be eutectic Sn/Pb, high-lead solder, or lead-free solder. The conductive material is bonded to UBM 156 using a suitable attachment or bonding process. In one embodiment, the conductive material is reflowed by heating the material above its melting point to form spherical balls or bumps 158. In some applications, bumps 158 are reflowed a second time to improve electrical contact to UBM 156. The bumps can also be compression bonded to UBM 156. Bumps 158 represent one type of interconnect structure that can be formed over UBM 156. The interconnect structure can also use bond wires, conductive paste, stud bump, micro bump, or other electrical interconnect.

In FIG. 3h, semiconductor wafer 118 is inverted again and singulated into semiconductor devices 160, which are metallurgically and electrically connected to contact pads 166 on PCB 168 using bumps 158. Semiconductor die 140 and passive device 144, as well as passive and active devices in active region 120, electrically connect to PCB 168 through bumps 138 and 158, UBMs 136 and 156, TSV 122, conductive pillars 132, bonds 146, and conductive layers 124 and 128.

The encapsulation process makes the substrate or wafer structurally robust during formation of additional interconnect structures. The encapsulant permits backside grinding to substantially reduce its thickness. The electrical connection

to PCB 168 is made on the backside of the wafer with TSVs 122 thus reducing the silicon area and package size and increasing device performance. The encapsulant eliminates the need for bonding & de-bonding to a temporary carrier, lowers manufacturing cost, reduces breakage and slip, simplifies handling, and enables higher processing temperatures. The electrical connection to the PCB on the backside of the substrate reduces silicon area and corresponding package size and thickness.

Another embodiment of forming an interconnect structure for 3-D devices using the process flow of FIGs. 3a-3d. At this point, TSVs 122, conductive layers 124 and 128, UBM 136, conductive pillars 132, bumps 138, semiconductor die 140, passive device 144, bonds 146, and insulating layers 126, 130, and 134 have been formed on semiconductor wafer 118. Encapsulant 150 is deposited over the structure 122-146 for structural support during formation of additional interconnect structures.

In FIG. 4a, semiconductor wafer 118 is inverted and back surface 152 is reduced in thickness by mechanical grinding, CMP, wet etching, dry etching, plasma etching, or another thinning process. Since semiconductor wafer 118 is covered with encapsulant 150, the structure is sufficiently robust to reduce substrate thickness to less than 300 μm. In one embodiment, the thickness of the substrate is reduced to 10-50 μm. A temporary carrier or tape is not needed because encapsulant 150 provides the support to maintain the structural integrity of the device, even with the reduced substrate thickness.

An insulating or passivation layer 170 is formed over back surface 152 and TSVs 122. The insulating layer 170 can be one or more layers of SiO_2, Si_3N_4, SiON, Ta_2O_5, Al_2O_3, or other

material having similar insulating properties. The insulating layer 170 is formed using PVD, CVD, printing, spin coating, spray coating, sintering, or thermal oxidation. A portion of insulating layer 170 is removed by an etching process to expose TSVs 122.

An electrically conductive layer 172 is formed over TSVs 122 and insulating layer 170 using PVD, CVD, sputtering, electrolytic plating, electroless plating process, or other suitable metal deposition process. Conductive layer 172 can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. Conductive layer 172 is a redistribution layer (RDL) in electrical contact with TSVs 122. RDL 172 extends electrical connectivity of TSVs 122.

In FIG. 4b, an insulating or passivation layer 174 is formed over insulating layer 170 and RDLs 172. The insulating layer 174 can be one or more layers of SiO2, Si3N4, SiON, Ta2O5, Al2O3, or other material having similar insulating properties. The insulating layer 174 is formed using PVD, CVD, printing, spin coating, spray coating, sintering, or thermal oxidation. A portion of insulating layer 174 is removed by an etching process to expose RDLs 172.

An electrically conductive layer 176 is formed over RDLs 172 and insulating layer 174 using PVD, CVD, sputtering, electrolytic plating, electroless plating process, or other suitable metal deposition process. Conductive layer 176 can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. Conductive layer 176 is a UBM in electrical contact with RDLs 172.

In FIG. 4c, an electrically conductive material is deposited over UBM 176 using an evaporation, electrolytic plating, electroless plating, ball drop, or screen printing

process. The conductive material can be Al, Sn, Ni, Au, Ag, Pb, Bi, Cu, solder, and combinations thereof, with an optional flux material. For example, the conductive material can be eutectic Sn/Pb, high-lead solder, or lead-free solder. The conductive material is bonded to UBM 176 using a suitable attachment or bonding process. In one embodiment, the conductive material is reflowed by heating the material above its melting point to form spherical balls or bumps 178. In some applications, bumps 178 are reflowed a second time to improve electrical contact to UBM 176. The bumps can also be compression bonded to UBM 176. Bumps 178 represent one type of interconnect structure that can be formed over UBM 176. The interconnect structure can also use bond wires, conductive paste, stud bump, micro bump, or other electrical interconnect.

In FIG. 4d, semiconductor wafer 118 is inverted again and singulated into semiconductor devices 180, which are metallurgically and electrically connected to contact pads 186 on PCB 188 using bumps 178. Semiconductor die 140 and passive device 144, as well as passive and active devices in active region 120, electrically connect to PCB 188 through bumps 138 and 158, RDL 172, TSV 122, UBMs 136 and 156, conductive pillars 132, bonds 146, and conductive layers 124 and 128.

The encapsulation process makes the substrate or wafer structurally robust during formation of additional interconnect structures. The encapsulant permits backside grinding to substantially reduce its thickness. The electrical connection to PCB 188 is made on the backside of the wafer with TSVs 122 thus reducing the silicon area and package size and increasing device performance. The encapsulant eliminates the need for bonding & de-bonding to a temporary carrier, lowers manufacturing cost, reduces breakage and slip, simplifies

handling, and enables higher processing temperatures. The electrical connection to the PCB on the backside of the substrate reduces silicon area and corresponding package size and thickness.

While one or more embodiments of the present invention have been illustrated in detail, the skilled artisan will appreciate that modifications and adaptations to those embodiments may be made without departing from the scope of the present invention as set forth in the following claims.

Claims

What is claimed:

1. A semiconductor device, comprising:

a substrate;

a via extending through the substrate;

a first insulating layer disposed on sidewalls of the via;

an electrically conductive material disposed in the via over the first insulating layer to form a through silicon via (TSV);

a first interconnect structure disposed over a first surface of the substrate;

a semiconductor die or component mounted to the first interconnect structure;

an encapsulant disposed over the first interconnect structure and semiconductor die or component; and

a second interconnect structure disposed over a second surface of the substrate, the second interconnect structure being electrically connected to the TSV.

2. The semiconductor device of claim 1, wherein the first interconnect structure includes:

a first conductive layer disposed over the TSV;

a second insulating layer disposed over the first conductive layer and substrate;

a second conductive layer disposed over the first conductive layer; and

a third insulating layer disposed over the second conductive layer and second insulating layer.

3. The semiconductor device of claim 2, wherein the first interconnect structure further includes:

a conductive pillar disposed over the second conductive layer;

a fourth insulating layer disposed around the conductive pillar; and

a third conductive layer disposed over the conductive pillar, wherein the third conductive layer is electrically connected to the semiconductor die or component.

4. The semiconductor device of claim 1, further including a printed circuit board, the semiconductor device mounted to the printed circuit board through the second interconnect structure.

5. The semiconductor device of claim 1, wherein the second interconnect structure includes:

a second insulating layer disposed over the second surface of the substrate and TSV; and

a first conductive layer disposed over the TSV and in contact with the TSV through the second insulating layer.

6. The semiconductor device of claim 1, wherein the second interconnect structure includes:

a second insulating layer disposed over the second surface of the substrate and the TSV;

a first conductive layer disposed over the TSV to extend the conductivity of the TSV;

a third insulating layer disposed over the second insulating layer and the first conductive layer; and

a second conductive layer disposed over the first conductive layer.

7. A semiconductor device, comprising:

a substrate;

a conductive via disposed through the substrate;

a first interconnect structure disposed over a first surface of the substrate;

a semiconductor die or a component disposed over the first interconnect structure and the conductive via;

an encapsulant deposited over the first interconnect structure and semiconductor die or component; and

a second interconnect structure disposed over a second surface of the substrate and electrically connected to the conductive via.

8. The semiconductor device of claim 7, wherein the first interconnect structure includes:

a first conductive layer disposed over the conductive via;

a first insulating layer disposed over the first conductive layer and substrate;

a second conductive layer disposed over the first conductive layer;

a second insulating layer disposed over the second conductive layer and first insulating layer;

a conductive pillar disposed over the second conductive layer;

a third insulating layer disposed around the conductive pillar; and

a third conductive layer disposed over the conductive pillar and electrically connected to the semiconductor die or component.

9. The semiconductor device of claim 7, wherein the first interconnect structure includes a conductive bump.

10. The semiconductor device of claim 7, the second interconnect structure including:

a first insulating layer disposed over the second surface of the substrate and the conductive via; and

a first conductive layer disposed over the conductive via.

11. The semiconductor device of claim 7, wherein the second interconnect structure includes:

a first insulating layer disposed over the substrate;

a first conductive layer disposed over the conductive via to extend the conductivity of the conductive via;

a second insulating layer disposed over the first insulating layer and first conductive layer; and

a second conductive layer disposed over the first conductive layer.

12. The semiconductor device of claim 7, wherein a thickness of the substrate is less than 300 μm.

13. A semiconductor device, comprising:

a substrate;

a conductive via disposed through the substrate;

a first interconnect structure disposed over a first surface of the substrate;

a semiconductor die or a component disposed over the first interconnect structure; and

an encapsulant disposed over the first interconnect structure and the semiconductor die or component.

14. The semiconductor device of claim 13, further including a second interconnect structure disposed over a second surface of the substrate, the second interconnect structure electrically connected to the conductive via.

15. The semiconductor device of claim 13, wherein the first interconnect structure includes a bond wire.

16. The semiconductor device of claim 14, wherein the second interconnect structure includes:

a first insulating layer disposed over the second surface of the substrate; and

a first conductive layer disposed over the conductive via.

17. The semiconductor device of claim 14, wherein the second interconnect structure includes:

a first insulating layer disposed over the second surface of the substrate;

a first conductive layer disposed over the conductive via to extend the conductivity of the conductive via;

a second insulating layer disposed over the first insulating layer and the first conductive layer; and

a second conductive layer disposed over the first conductive layer.

18. The semiconductor device of claim 13, wherein the first interconnect structure includes:

a first conductive layer disposed over the conductive via;

a first insulating layer disposed over the first conductive layer and the substrate;

a second conductive layer disposed over the first insulating layer;

a second insulating layer disposed over the second conductive layer and the first insulating layer;

a conductive pillar disposed over the second conductive layer;

a third insulating layer disposed around the conductive pillar; and

a third conductive layer disposed over the conductive pillar, the semiconductor die or component electrically connected to the third conductive layer.

19. The semiconductor device of claim 13, wherein a thickness of the substrate is in a range of about 10 μm to about 50 μm.

20. A semiconductor device, comprising:

a substrate;

a conductive via disposed partially through the substrate;

a first interconnect structure disposed over a first surface of the substrate;

a semiconductor component disposed over the first interconnect structure; and

an encapsulant disposed over the first interconnect structure and the semiconductor component.

21. The semiconductor device of claim 20, wherein the first interconnect structure includes a conductive paste.

22. The semiconductor device of claim 20, wherein the first interconnect structure includes:

a first conductive layer over the conductive via;

a first insulating layer over the first conductive layer;

a second conductive layer over the first insulating layer; and

a second insulating layer over the second conductive layer and the first insulating layer.

23. The semiconductor device of claim 22, wherein the first interconnect structure further includes:

a conductive pillar over the second conductive layer;

a third insulating layer around the conductive pillar; and

a third conductive layer over the conductive pillar, the semiconductor component electrically connected to the third conductive layer.

24. The semiconductor device of claim 20, wherein a thickness of the substrate is in a range of 10 µm to 50 µm.

25. The semiconductor device of claim 20, wherein a thickness of the substrate is less than 300 µm.