CLAIMS

1. A computer implemented method for extending an effective number of General Purpose Registers (GPRs) available to instructions of a program in a computer having a first number of large GPRs, each instruction comprising an opcode and one or more GPR fields for specifying corresponding GPRs, each large GPR comprising a first portion and a second portion, said large GPRs comprising first small GPRs consisting of first portions and second small GPRs consisting of second portions, the method comprising:

responsive to the computer being in a small GPR mode; executing instructions of a first set of instructions, the first set of instructions for accessing said first small GPRs, the execution comprising generating memory addresses for accessing memory operands based on said first small GPRs or accessing first small GPR operands, wherein the first small GPRs consist of said first portions; and executing instructions of a second set of instructions, the second set of instructions for accessing said second small GPRs, the execution comprising generating memory addresses for accessing memory operands based on said second small GPRs or accessing second small GPR operands, wherein the second small GPRs consist of said second portions; and

responsive to the computer being in a large GPR mode, executing instructions of a third set of instructions, the execution comprising generating memory addresses for accessing memory operands based on said large GPRs or accessing large GPR operands comprising said first portions and said second portions.

2. The method according to Claim 1, the small GPR mode comprising being in one of a 24 bit addressing mode or a 31 bit addressing mode.

3. The method according to Claim 1 or Claim 2, wherein the first portion is 32 bits and the second portion is 32 bits.

4. The method according to any preceding claim, wherein the execution of the instruction of the second instruction set comprises performing a corresponding opcode defined function based on two operands, and storing the result, the corresponding opcode

defined function consisting of an ADD of two operands function or a COMPARE of two operands function.

5. The method according to any of claims 1 to 3, wherein the execution of the instruction of the second instruction set comprises performing a corresponding opcode defined function based on two operands, and storing the result, the corresponding opcode defined function consists of a LOAD of an operand from memory function or a STORE of an operand to memory function.

6. The method according to any of claims 1 to 3, wherein the execution of the instruction of the second instruction set comprises performing a corresponding opcode defined function based on two operands, and storing the result, the corresponding opcode defined function is a ROTATE THEN INSERT SELECTED BITS function comprising:

rotating a source operand by an instruction specified amount; and

inserting a selected portion of the rotated source operand in a selected portion of a target operand.

7. The method according to Claim 2, comprising supporting an Operating System operating in Large GPR mode wherein the Large GPRs are saved and restored during context switches for Applications running in Small GPR mode.

8. The method according to Claim 7, wherein the third set of instructions comprise the first set of instructions and the second set of instructions.

9. A computer program product for extending an effective number of General Purpose Registers (GPRs) available to instructions of a program in a computer having a first number of large GPRs, each instruction comprising an opcode and one or more GPR fields for specifying corresponding GPRs, each large GPR comprising a first portion and a second portion, said large GPRs comprising first small GPRs consisting of first portions and second small GPRs consisting of second portions, the computer program product comprising a tangible storage medium readable by a processing circuit and storing instructions which

when executed by the processing circuit perform the method according to any of claims 1 to 8.

10. A computer system for extending an effective number of General Purpose Registers (GPRs) available to instructions of a program in a computer having a first number of large GPRs, each instruction comprising an opcode and one or more GPR fields for specifying corresponding GPRs, each large GPR comprising a first portion and a second portion, said large GPRs comprising first small GPRs consisting of first portions and second small GPRs consisting of second portions, comprising:

a memory;

a processor in communication with the memory, the processor comprising an instruction fetching element for fetching instructions from memory and one or more execution elements for executing fetched instructions;

wherein the computer system is configured to perform the method according to any of claims 1 to 8.

CLAIMS

1. A computer implemented method for extending an effective number of General Purpose Registers (GPRs) available to instructions of a program in a computer having a first number of large GPRs, each instruction comprising an opcode and one or more GPR fields for specifying corresponding GPRs, each large GPR comprising a first portion and a second portion, said large GPRs comprising first small GPRs consisting of first portions and second small GPRs consisting of second portions, the computer having a small GPR mode and a large GPR mode, the small GPR mode using only operands of a first small GPRs as GPR based main store operand addresses, the large GPR mode using operands spanning both first small GPRs and second small GPRs as GPR based main store operands, the method comprising:

based on a program status word (PSW), determining whether the computer is in a small GPR mode or a large GPR mode, the small GPR mode permitting execution of programs written for a computer having a small GPR architecture, the small GPR architecture having memory addresses and register operands limited to the size of a small GPR;

based on a High-Word facility function of the computer being not enabled, preventing execution of a second set of instructions, the computer having a control field controlling whether the High-Word function is enabled or disabled;

responsive to the computer being in the small GPR mode, executing instructions of a first set of instructions, the first set of instructions for accessing said first small GPRs, the execution comprising generating memory addresses for accessing memory operands based on said first small GPRs or accessing first small GPR operands, wherein the first small GPRs consist of said first portions;

based on the High-Word facility function being enabled, executing instructions of the second set of instructions, the second set of instructions for accessing said second small GPRs, the execution comprising generating memory addresses for accessing memory operands based on said second small GPRs or accessing second small GPR operands, wherein the second small GPRs consist of said second portions; and

responsive to the computer being in the large GPR mode, executing instructions of a third set of instructions, the execution comprising generating memory addresses for accessing memory operands based on said large GPRs or accessing large GPR operands comprising said first portions and said second portions.

2. The method according to Claim 1, the small GPR mode comprising being in one of a 24 bit addressing mode or a 31 bit addressing mode.

3. The method according to Claim 1 or Claim 2, wherein the first portion is 32 bits and the second portion is 32 bits.

4. The method according to any preceding claim, wherein the execution of the instruction of the second instruction set comprises performing a corresponding opcode defined function based on two operands, and storing the result, the corresponding opcode defined function consisting of an ADD of two operands function or a COMPARE of two operands function.

5. The method according to any of claims 1 to 3, wherein the execution of the instruction of the second instruction set comprises performing a corresponding opcode defined function based on two operands, and storing the result, the corresponding opcode defined function consists of a LOAD of an operand from memory function or a STORE of an operand to memory function.

6. The method according to any of claims 1 to 3, wherein the execution of the instruction of the second instruction set comprises performing a corresponding opcode defined function based on two operands, and storing the result, the corresponding opcode defined function is a ROTATE THEN INSERT SELECTED BITS function comprising:

rotating a source operand by an instruction specified amount; and

inserting a selected portion of the rotated source operand in a selected portion of a target operand.

7. The method according to Claim 2, comprising supporting an Operating System operating in Large GPR mode wherein the Large GPRs are saved and restored during context switches for Applications running in Small GPR mode.

8. The method according to Claim 7, wherein the third set of instructions comprise the first set of instructions and the second set of instructions.

9. A computer program product for extending an effective number of General Purpose Registers (GPRs) available to instructions of a program in a computer having a first number of large GPRs, each instruction comprising an opcode and one or more GPR fields for specifying corresponding GPRs, each large GPR comprising a first portion and a second portion, said large GPRs comprising first small GPRs consisting of first portions and second small GPRs consisting of second portions, the computer program product comprising a tangible storage medium readable by a processing circuit and storing instructions which when executed by the processing circuit perform the method according to any of claims 1 to 8.

10. A computer system for extending an effective number of General Purpose Registers (GPRs) available to instructions of a program in a computer having a first number of large GPRs, each instruction comprising an opcode and one or more GPR fields for specifying corresponding GPRs, each large GPR comprising a first portion and a second portion, said large GPRs comprising first small GPRs consisting of first portions and second small GPRs consisting of second portions, comprising:

a memory;

a processor in communication with the memory, the processor comprising an instruction fetching element for fetching instructions from memory and one or more execution elements for executing fetched instructions;

wherein the computer system is configured to perform the method according to any of claims 1 to 8.