VERTICAL NROM

Cross Reference To Related Applications

This application is related to the following co-pending, commonly assigned U.S. patent applications: "Write Once Read Only Memory Employing Charge Trapping in Insulators," attorney docket no. 1303.052US1, U.S. serial number 10/177,077, "Write Once Read Only Memory Employing Floating Gates," attorney docket no. 1303.051US1, U.S. serial number 10/177,083, "Nanocrystal Write Once Read Only Memory for Archival Storage," attorney docket no. 1303.054US1, U.S. serial number 10/177,214, "Write Once Read Only Memory with Large Work Function Floating Gates," attorney docket no. 1303.055US1, U.S. serial number 10/177,213, "Ferroelectric Write Once Read Only Memory for Archival Storage," attorney docket no. 1303.058US1, U.S. serial number 10/177,082, and "Multistate NROM Having a Storage Density Much Greater than 1 Bit per $1F^2$," attorney docket no. 1303.053US1, U.S. serial number 10/177,211, which are filed on even date herewith and each of which disclosure is herein incorporated by reference.

Field of the Invention

The present invention relates generally to semiconductor integrated circuits and, more particularly, to vertical NROM having a storage density of one bit for each 1.0 lithographic feature squared ($1F^2$) unit area.

Background of the Invention

Many electronic products need various amounts of memory to store information, e.g. data. One common type of high speed, low cost memory includes dynamic random access memory (DRAM) comprised of individual DRAM cells arranged in arrays. DRAM cells include an access transistor, e.g a metal oxide semiconducting field effect transistor (MOSFET), coupled to a capacitor cell. With successive generations of DRAM chips, an emphasis continues to be placed on increasing array density and maximizing chip real estate while minimizing the cost of manufacture. It is further desirable to increase array density with little or no modification of the DRAM optimized process flow.

A requirement exists for memory devices which need only be programmed a limited number of times, as for instance to function as an electronic film in a camera. If the memory arrays have a very high density then they can store a large number of very high resolution images in a digital camera. If the memory is inexpensive then it can for instance replace the light sensitive films which are used to store images in conventional cameras.

Thus, there is a need for improved DRAM technology compatible high density memory cells. It is desirable that such memory cells be fabricated on a DRAM chip with little or no modification of the DRAM process flow. It is further desirable that such memory cells operate with lower programming voltages than that used by conventional DRAM cells, yet still hold sufficient charge to withstand the effects of parasitic capacitances and noise due to circuit operation.

Summary of the Invention

The above mentioned problems for creating DRAM technology high density memory cells as well as other problems are addressed by the present invention and will be understood by reading and studying the following specification. This disclosure teaches structures and methods using MOSFET devices as a multiple bit memory cells in a DRAM integrated circuit. The structures and methods use the existing process sequence for MOSFET's in DRAM technology.

In particular, an illustrative embodiment of the present invention includes a vertical multiple bit memory cell. The vertical multiple bit memory cell includes a vertical metal oxide semiconductor field effect transistor (MOSFET) extending outwardly from a substrate. The MOSFET has a first source/drain region, a second source/drain region, a channel region between the first and the second source/drain regions, and a gate separated from the channel region by a gate insulator. A first transmission line is coupled to the first source/drain region. A second transmission line is coupled to the second source/drain region. The MOSFET is adapted to be programmed to have a charge trapped in at least one of a first storage region and a second storage region in the gate insulator and

operated with either the first source/drain region or the second source/drain region serving as the source region.

These and other embodiments, aspects, advantages, and features of the present invention will be set forth in part in the description which follows, and in part will become apparent to those skilled in the art by reference to the following description of the invention and referenced drawings or by practice of the invention. The aspects, advantages, and features of the invention are realized and attained by means of the instrumentalities, procedures, and combinations particularly pointed out in the appended claims.

Brief Description of the Drawings

Figure 1A is a block diagram of a metal oxide semiconductor field effect transistor (MOSFET) in a substrate according to the teachings of the prior art.

Figure 1B illustrates the MOSFET of Figure 1A operated in the forward direction showing some degree of device degradation due to electrons being trapped in the gate oxide near the drain region over gradual use.

Figure 1C is a graph showing the square root of the current signal (Ids) taken at the drain region of the conventional MOSFET versus the voltage potential (VGS) established between the gate and the source region.

Figure 2A is a diagram of a programmed MOSFET which can be used as a multiple bit cell according to the teachings of the present invention.

Figure 2B is a diagram suitable for explaining the method by which the MOSFET of the multiple bit cell of the present invention can be programmed to achieve the embodiments of the present invention.

Figure 2C is a graph plotting the current signal (Ids) detected at the drain region versus a voltage potential, or drain voltage, (VDS) set up between the drain region and the source region (Ids vs. VDS).

Figure 3A illustrates a vertical NROM 301 having a storage density of one bit per one photolithographic feature squared ($1F^2$) unit area according to the teachings of the present invention.

Figure 3B illustrates an electrical equivalent circuit for the vertical NROM device structure shown in Figure 3A.

Figure 4A illustrates a portion of a memory array 400 according to the teachings of the present invention.

Figure 4B illustrates an electrical equivalent circuit 400 for the portion of the memory array shown in Figure 4A.

Figures 5A-5B illustrates the operation of the novel vertical multiple bit cell formed according to the teachings of the present invention.

Figure 6 illustrates the operation of a conventional DRAM cell.

Figure 7 illustrates a memory device according to the teachings of the present invention.

Figure 8 is a block diagram of an electrical system, or processor-based system, utilizing vertical multiple bit cells constructed in accordance with the present invention.

Description of the Preferred Embodiments

In the following detailed description of the invention, reference is made to the accompanying drawings which form a part hereof, and in which is shown, by way of illustration, specific embodiments in which the invention may be practiced. In the drawings, like numerals describe substantially similar components throughout the several views. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope of the present invention.

The terms wafer and substrate used in the following description include any structure having an exposed surface with which to form the integrated circuit (IC) structure of the invention. The term substrate is understood to include semiconductor wafers. The term substrate is also used to refer to semiconductor structures during processing, and may include other layers that have been fabricated thereupon. Both wafer and substrate include doped and undoped semiconductors, epitaxial semiconductor layers supported by a base semiconductor or insulator, as well as other semiconductor structures well known to one skilled in the art. The term conductor is understood to include semiconductors, and the term insulator is defined to include any material that is less electrically conductive than the materials referred to as conductors. The

following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims, along with the full scope of equivalents to which such claims are entitled.

Figure 1A is useful in illustrating the conventional operation of a MOSFET such as can be used in a DRAM array. Figure 1A illustrates the normal hot electron injection and degradation of devices operated in the forward direction. As is explained below, since the electrons are trapped near the drain they are not very effective in changing the device characteristics.

Figure 1A is a block diagram of a metal oxide semiconductor field effect transistor (MOSFET) 101 in a substrate 100. The MOSFET 101 includes a source region 102, a drain region 104, a channel region 106 in the substrate 100 between the source region 102 and the drain region 104. A gate 108 is separated from the channel region 108 by a gate oxide 110. A sourceline 112 is coupled to the source region 102. A bitline 114 is coupled to the drain region 104. A wordline 116 is coupled to the gate 108.

In conventional operation, a drain to source voltage potential (Vds) is set up between the drain region 104 and the source region 102. A voltage potential is then applied to the gate 108 via a wordline 116. Once the voltage potential applied to the gate 108 surpasses the characteristic voltage threshold (Vt) of the MOSFET a channel 106 forms in the substrate 100 between the drain region 104 and the source

region 102. Formation of the channel 106 permits conduction between the drain region 104 and the source region 102, and a current signal (Ids) can be detected at the drain region 104.

In operation of the conventional MOSFET of Figure 1A, some degree of device degradation does gradually occur for MOSFETs operated in the forward direction by electrons 117 becoming trapped in the gate oxide 110 near the drain region 104. This effect is illustrated in Figure 1B. However, since the electrons 117 are trapped near the drain region 104 they are not very effective in changing the MOSFET characteristics.

Figure 1C illustrates this point. Figure 1C is a graph showing the square root of the current signal (Ids) taken at the drain region versus the voltage potential
(VGS) established between the gate 108 and the source region 102. The change in the slope of the plot of $\sqrt{Ids}$ versus VGS represents the change in the charge carrier mobility in the channel 106.

In Figure 1C, ΔVT represents the minimal change in the MOSFET's threshold voltage resulting from electrons gradually being trapped in the gate oxide 110 near the drain region 104, under normal operation, due to device degradation. This results in a fixed trapped charge in the gate oxide 110 near the drain region 104. Slope 1 represents the charge carrier mobility in the channel 106 for Figure 1A having no electrons trapped in the gate oxide 110. Slope 2 represents the charge mobility in the channel 106 for the conventional MOSFET of Figure 1B having electrons 117 trapped in the gate oxide 110 near the drain region 104. As shown by a comparison of slope 1 and slope 2 in Figure 1C, the electrons 117 trapped in the gate oxide 110 near the drain region 104 of the conventional MOSFET do not significantly change the charge mobility in the channel 106.

There are two components to the effects of stress and hot electron injection. One component includes a threshold voltage shift due to the trapped electrons and a second component includes mobility degradation due to additional scattering of carrier electrons caused by this trapped charge and additional surface states. When a conventional MOSFET degrades, or is "stressed," over operation in the forward direction, electrons do gradually get injected and become trapped in the gate oxide near the drain. In this portion of the conventional MOSFET there is virtually no channel underneath the gate oxide. Thus the trapped charge modulates the threshold voltage and charge mobility only slightly.

The inventors have previously described programmable memory devices and functions based on the reverse stressing of MOSFET's in a conventional CMOS process and technology in order to form programmable address decode

and correction. (See generally, L. Forbes, W.P. Noble and E.H. Cloud, "MOSFET technology for programmable address decode and correction," U.S. application serial number 09/383,804, now issued as U.S. Patent No. 6,521,958). That disclosure, however, did not describe vertical multiple bit cell solutions, but rather address decode and correction issues.

According to the teachings of the present invention, normal MOSFETs can be programmed by operation in the reverse direction and utilizing avalanche hot electron injection to trap electrons in the gate oxide of the MOSFET. When the programmed MOSFET is subsequently operated in the forward direction the electrons trapped in the oxide are near the source and cause the channel to have two different threshold voltage regions. The novel programmed MOSFETs of the present invention conduct significantly less current than conventional MOSFETs, particularly at low drain voltages. These electrons will remain trapped in the gate oxide unless negative gate voltages are applied. The electrons will not be removed from the gate oxide when positive or zero gate voltages are applied. Erasure can be accomplished by applying negative gate voltages and/or increasing the temperature with negative gate bias applied to cause the trapped electrons to be re-emitted back into the silicon channel of the MOSFET. (See generally, L. Forbes, E. Sun, R. Alders and J. Moll, "Field induced re-emission of electrons trapped in SiO_2," IEEE Trans. Electron Device, vol. ED-26, no. 11, pp. 1816-1818 (Nov. 1979); S.S.B. Or, N. Hwang, and L. Forbes, "Tunneling and Thermal emission from a distribution of deep traps in SiO_2," IEEE Trans. on Electron Devices, vol. 40, no. 6, pp. 1100-1103 (June 1993); S.A. Abbas and R.C. Dockerty, "N-channel IGFET design limitations due to hot electron trapping," IEEE Int. Electron Devices Mtg., Washington D.C., Dec. 1975, pp. 35-38).

Figures 2A-2C illustrate are useful in illustrating the present invention in which a much larger change in device characteristics is obtained by programming the device in the reverse direction and subsequently reading the device by operating it in the forward direction.

Figure 2A is a diagram of a programmed MOSFET which can be used as a multiple bit cell according to the teachings of the present invention. As shown

in Figure 2A the multiple bit cell 201 includes a MOSFET in a substrate 200 which has a first source/drain region 202, a second source/drain region 204, and a channel region 206 between the first and second source/drain regions, 202 and 204. In one embodiment, the first source/drain region 202 includes a source region 202 for the MOSFET and the second source/drain region 204 includes a drain region 204 for the MOSFET. Figure 2A further illustrates a gate 208 separated from the channel region 206 by a gate oxide 210. A first transmission line 212 is coupled to the first source/drain region 202 and a second transmission line 214 is coupled to the second source/drain region 204. In one embodiment, the first transmission line includes a sourceline 212 and the second transmission line includes a bit line 214.

As stated above, multiple bit cell 201 is comprised of a programmed MOSFET. This programmed MOSFET has a charge 217 trapped in the gate oxide 210 adjacent to the first source/drain region 202 such that the channel region 206 has a first voltage threshold region (Vt1) and a second voltage threshold region (Vt2) in the channel 206. In one embodiment, the charge 217 trapped in the gate oxide 210 adjacent to the first source/drain region 202 includes a trapped electron charge 217. According to the teachings of the present invention and as described in more detail below, the multiple bit cell can be programmed to have a charge stored in at least one of a first storage region and a second storage region in the gate insulator 210 and operated with either the first source/drain region 202 or the second source/drain region 204 serving as the source region such that the multiple bit cell 201 will have a first voltage threshold region (Vt1) and a second voltage threshold region (Vt2) and such that the programmed multiple bit cell operates at reduced drain source current.

Figure 2A illustrates the Vt2 in the channel 206 is adjacent the first source/drain region 202 and that the Vt1 in the channel 206 is adjacent the second source/drain region 204. However, the invention is not so limited and in one embodiment Vt1 is adjacent the first source/drain region. According to the teachings of the present invention, Vt2 and Vt1 vary depending on in which direction the multiple bit cell is operated. In this manner multiple bits can be stored on the multiple bit cell 201.

Figure 2B is a diagram suitable for explaining the method by which the MOSFET of the multiple bit cell 201 of the present invention can be programmed to achieve the embodiments of the present invention. As shown in Figure 2B the method includes programming the MOSFET in a reverse direction. Programming the MOSFET in the reverse direction includes applying a first voltage potential V1 to a drain region 204 of the MOSFET. In one embodiment, applying a first voltage potential V1 to the drain region 204 of the MOSFET includes grounding the drain region 204 of the MOSFET as shown in Figure 2B. A second voltage potential V2 is applied to a source region 202 of the MOSFET. In one embodiment, applying a second voltage potential V2 to the source region 202 includes applying a high positive voltage potential (VDD) to the source region 202 of the MOSFET, as shown in Figure 2B. A gate potential VGS is applied to a gate 208 of the MOSFET. In one embodiment, the gate potential VGS includes a voltage potential which is less than the second voltage potential V2, but which is sufficient to establish conduction in the channel 206 of the MOSFET between the drain region 204 and the source region 202. As shown in Figure 2B, applying the first, second and gate potentials (V1, V2, and VGS respectively) to the MOSFET creates a hot electron injection into a gate oxide 210 of the MOSFET adjacent to the source region 202. In other words, applying the first, second and gate potentials (V1, V2, and VGS respectively) provides enough energy to the charge carriers, e.g. electrons, being conducted across the channel 206 that, once the charge carriers are near the source region 202, a number of the charge carriers get excited into the gate oxide 210 adjacent to the source region 202. Here the charge carriers become trapped.

In one embodiment of the present invention, the method is continued by subsequently operating the MOSFET in the forward direction in its programmed state during a read operation. Accordingly, the read operation includes grounding the source region 202 and precharging the drain region a fractional voltage of VDD. If the device is addressed by a wordline coupled to the gate, then its conductivity will be determined by the presence or absence of stored charge in the gate insulator. That is, a gate potential can be applied to the gate 208 by a wordline 216 in an effort to form a conduction channel between the

source and the drain regions as done with addressing and reading conventional DRAM cells.

However, now in its programmed state, the conduction channel 206 of the MOSFET will have a first voltage threshold region (Vt1) adjacent to the drain region 204 and a second voltage threshold region (Vt2) adjacent to the source region 202, as explained and described in detail in connection with Figure 2A. According to the teachings of the present invention, the Vt2 has a greater voltage threshold than the Vt1 due to the hot electron injection 217 into a gate oxide 210 of the MOSFET adjacent to the source region 202.

Figure 2C is a graph plotting a current signal (Ids) detected at the second source/drain region 204 versus a voltage potential, or drain voltage, (VDS) set up between the second source/drain region 204 and the first source/drain region 202 (Ids vs. VDS). In one embodiment, VDS represents the voltage potential set up between the drain region 204 and the source region 202. In Figure 2C, the curve plotted as D1 represents the conduction behavior of a conventional MOSFET which is not programmed according to the teachings of the present invention. The curve D2 represents the conduction behavior of the programmed MOSFET, described above in connection with Figure 2A, according to the teachings of the present invention. As shown in Figure 2C, for a particular drain voltage, VDS, the current signal (IDS2) detected at the second source/drain region 204 for the programmed MOSFET (curve D2) is significantly lower than the current signal (IDS1) detected at the second source/drain region 204 for the conventional MOSFET which is not programmed according to the teachings of the present invention. Again, this is attributed to the fact that the channel 206 in the programmed MOSFET of the present invention has two voltage threshold regions and that the voltage threshold, Vt2, near the first source/drain region 202 has a higher voltage threshold than Vt1 near the second source/drain region due to the charge 217 trapped in the gate oxide 217 adjacent to the first source/drain region 202.

Some of these effects have recently been described for use in a different device structure, called an NROM, for flash memories. This latter work in Israel and Germany is based on employing charge trapping in a silicon nitride layer in a

non-conventional flash memory device structure. (See generally, B. Eitan et al., "Characterization of Channel Hot Electron Injection by the Subthreshold Slope of NROM device," IEEE Electron Device Lett., Vol. 22, No. 11, pp. 556-558, (Nov. 2001); B. Etian et al., "NROM: A novel localized Trapping, 2-Bit Nonvolatile Memory Cell," IEEE Electron Device Lett., Vol. 21, No. 11, pp. 543-545, (Nov. 2000)). Charge trapping in silicon nitride gate insulators was the basic mechanism used in MNOS memory devices (see generally, S. Sze, Physics of Semiconductor Devices, Wiley, N.Y., 1981, pp. 504-506), charge trapping in aluminum oxide gates was the mechanism used in MIOS memory devices (see generally, S. Sze, Physics of Semiconductor Devices, Wiley, N.Y., 1981, pp. 504-506), and the present inventors have previously disclosed charge trapping at isolated point defects in gate insulators (see generally, L. Forbes and J. Geusic, "Memory using insulator traps," US Patent 6,140,181, issued October 31, 2000).

In contrast to the above work, the present invention disclosures programming a MOSFET in a reverse direction to trap charge in a first or a second storage region in a gate insulator adjacent either a first or a second source/drain region. The MOSFET can be programmed and operated in either direction such that the MOSFET has a storage density of $1bit/1F^2$. The MOSFET can be operated with either the first or the second source/drain region serving as the source such that a charge trapped in the gate insulator in either the first or the second storage region, adjacent to the first or the second source/drain region serving as the source, will provide a reduced drain source current. The MOSFET having a storage density of $1bit/1F^2$ is based on a modification of DRAM technology.

Prior art DRAM technology generally employs silicon oxide as the gate insulator. Further the emphasis in conventional DRAM devices is placed on trying to minimize charge trapping in the silicon oxide gate insulator. According to the teachings of the present invention, a variety of insulators are used to trap electrons more efficiently than in silicon oxide. That is, in the present invention, the vertical multiple bit memory cell employs charge trapping in gate insulators such as, wet silicon oxide, silicon nitride, silicon oxynitride SON, silicon rich oxide SRO, aluminum oxide Al_2O_3, composite layers of these insulators such as

oxide and then silicon nitride, or oxide and then aluminum oxide, or multiple layers as oxide-nitride-oxide. While the charge trapping efficiency of silicon oxide may be low such is not the case for silicon nitride or composite layers of silicon oxide and nitride.

Figure 3A illustrates a vertical NROM 301 having a storage density of one bit per one photolithographic feature squared ($1F^2$) unit area according to the teachings of the present invention. As shown in Figure 3A, the vertical NROM 301 includes a vertical metal oxide semiconductor field effect transistor (MOSFET) 301 extending outwardly from a substrate 300. The MOSFET 301 has a first source/drain region 302 which in this n-channel embodiment includes a heavily doped (n+) n-type region layered with an n-type doped region. The MOSFET 301 includes a similarly structured second source/drain region 306. A channel region 305 is located in the vertical pillar between the first and the second source/drain regions, 302 and 306 respectively. As shown in the embodiment of Figure 3A, a gate 309 is separated from the channel region 305 by a gate insulator 307 as is located alongside of the vertical pillar opposing the channel region 305. In the embodiment shown in Figure3, the gate insulator 307 includes a gate insulator formed of an oxide-nitride-oxide (ONO) composition 307. In alternative embodiments, discussed below, the gate insulator 307 includes a gate insulator selected from the group of silicon dioxide (SiO_2) formed by wet oxidation, silicon oxynitride (SON), silicon rich oxide (SRO), and silicon rich aluminum oxide (Al_2O_3). In one embodiment, the gate insulator 307 has a thickness of approximately 10 nanometers (nm). In other embodiments, the gate insulator 307 includes a gate insulator 307 selected from the group of silicon rich aluminum oxide insulators, silicon rich oxides with inclusions of nanoparticles of silicon, silicon oxide insulators with inclusions of nanoparticles of silicon carbide, and silicon oxycarbide insulators. In still other embodiments, the gate insulator 307 includes a gate insulator 307 which includes a composite layer selected from the group of an oxide-aluminum oxide (Al_2O_3)-oxide composite layer, and oxide-silicon oxycarbide-oxide composite layer. In still other embodiments, the gate insulator 307 includes a gate insulator 307 which includes a composite layer, or a non-stoichiometric single layer of two or more

materials selected from the group of silicon (Si), titanium (Ti), and tantalum (Ta).

Figure 3B illustrates an electrical equivalent circuit for the vertical NROM device structure shown in Figure 3A. As shown in Figure 3B a first transmission line 304 is coupled to the first source/drain region 302. A second transmission line 311 is coupled to the second source/drain region 306. The circles, shown generally as 317, represent charge traps within the gate insulator 307. Thus, in the embodiment of Figure 3A where the gate insulator includes an ONO layer, the traps 317 represent locations where electrons can be stored within the nitride of the ONO gate insulator 307.

According to the teachings of the present invention, the vertical MOSFET is a programmed MOSFET having a charge programmed in at least one of a first storage region 340 and a second storage region 350 in the gate insulator 307. In the embodiment shown in Figure 3A, the first storage region 340 is adjacent, or neighboring, the second source/drain region 306 and the second storage region 350 is adjacent, or neighboring the first source/drain region 302. The designation first or second storage region is provided for spacial relationship reference in the embodiment of Figure 3A, is not intended to be limiting, and alternatively the first storage region can be associated next to the first source/drain region and the second storage region can be associated next to the second source/drain region.

According to the teachings of the present invention, and as described in more detail below, the vertical MOSFET 301 can be operated in either a first or a second direction, e.g. a first and second mode. That is, the vertical MOSFET 301 can be operated with either the first source/drain region 302 or the second source/drain region 306 serving as the source region. As will be understood by one of ordinary skill in the art upon reading this disclosure, the vertical MOSFET operates at reduced drain source current when reading a programmed charge state stored in either the first or the second storage region, 340 and 350 respectively.

For example, in one embodiment the first source/drain region of the MOSFET serves as a source region and the second source/drain region of the

MOSFET serves as a drain region in a first mode of operation, and the first source/drain region of the MOSFET serves as a drain region and the second source/drain region of the MOSFET serves as a source region in a second mode of operation.

As will be understood by one of ordinary skill in the art upon reading this disclosure and according to the teachings of the present invention, in one embodiment the vertical MOSFET has a storage density of one bit per one photolithographic feature squared ($1F^2$) unit area since a bit can be written to, or stored in as well as read from both the first storage region 340 and the second storage region 350. Thus, in some embodiments, the MOSFET includes a charge programmed in both the first storage region 340 and the second storage region 350.

As one of ordinary skill in the art will understand upon reading this disclosure, the charge programmed in the at least one of the first charge storage region 340 and the second storage region 350 creates a high voltage threshold when the MOSFET is operated with the an adjacent first source/drain region 302 or the second source/drain region 306 serving as the source region. Thus, in one embodiment of the invention the channel region has a first voltage threshold region (Vt1) adjacent to the first source/drain region a second voltage threshold region (Vt2) adjacent to the second source/drain region which vary depending on in which direction the MOSFET is operated, e.g. which of the first or the second source/drain regions, 302 and 306, is presently serving as the source region.

In one embodiment, the second voltage threshold region (Vt2) in the channel is adjacent the first source/drain region, and the first voltage threshold region (Vt1) in the channel is adjacent the second source/drain region. If a charge stored in the second storage region 350 illustrated in the embodiment of Figure 3A, then Vt2 has a higher voltage threshold than the Vt1 when the MOSFET is operated with the first source/drain region serving as the source region.

Thus, Figures 3A and 3B illustrate a change from previous vertical transistors to now form an NROM type device along the sidewall with, in one embodiment, an ONO gate structure. The nitride layer is used as a first and a

second charge storage region when the device is stressed in the reverse direction. The transistor is addressed and read in the forward conduction direction, the presence of stored charge in the first or the second storage region, near the first or the second source/drain region serving as the source, will result in a large change in the current in the forward direction. These transistors as represented by the equivalent circuit, 3B, can be stressed and/or tested in either direction, so that charge can be stored in either end of the channel. This results in the ability of each transistor to store two bits of data and a higher memory density in terms of bits per unit area.

Figure 4A illustrates a portion of a memory array 400 according to the teachings of the present invention. The memory in Figure 4A, is shown illustrating a number of vertical pillars, vertical multiple bit memory cells, and or vertical MOSFETs 401-1 and 401-2 formed according to the teachings of the present invention. As one of ordinary skill in the art will appreciate upon reading this disclosure, the number of vertical pillar are formed in rows and columns extending outwardly from a substrate 403. As shown in Figure 4A, the number of vertical pillars, 401-1 and 401-2 are separated by a number of trenches 430. According to the teachings of the present invention, the number of vertical pillars, 401-1 and 401-2, serve as transistors including a first source/drain region, 402-1 and 402-2 respectively. The first source/drain region, 402-1 and 402-2, is coupled to a first transmission line 404. As shown in the embodiment of Figure 4A, the first transmission line 404 includes a buried first transmission line formed beneath columns of the vertical transistors, 401-1 and 401-2. A second source/drain region, 406-1 and 406-2 respectively, is coupled to a second transmission line 411. Thus, these devices can be formed in array structures such as DRAM arrays, with bit or data lines as a common source line and a common metal wiring line.

As shown in Figure 4A, a channel region 405 is located between the first and the second source/drain regions. A gate 407 is separated from the channel region 405 by a gate insulator 407 in the trenches 430 along columns of the vertical pillars, 401-1 and 401-2. In one embodiment, according to the teachings of the present invention, the gate insulator 407 includes a gate insulator 407

selected from the group of silicon dioxide (SiO_2) formed by wet oxidation, silicon oxynitride (SON), silicon rich oxide (SRO), and aluminum oxide (Al_2O_3). In another embodiment, according to the teachings of the present invention, the gate insulator 407 includes a gate insulator 407 selected from the group of silicon rich aluminum oxide insulators, silicon rich oxides with inclusions of nanoparticles of silicon, silicon oxide insulators with inclusions of nanoparticles of silicon carbide, and silicon oxycarbide insulators. In another embodiment, according to the teachings of the present invention, the gate insulator 407 includes a composite layer 407. In this embodiment, the composite layer 407 includes a composite layer 407 selected from the group of an oxide-aluminum oxide (Al_2O_3)-oxide composite layer, and oxide-silicon oxycarbide-oxide composite layer. In another embodiment, the composite layer 407 includes a composite layer 407, or a non-stoichiometric single layer, of two or more materials selected from the group of silicon (Si), titanium (Ti), and tantalum (Ta). In another embodiment, according to the teachings of the present invention, the gate insulator 407 includes an oxide-nitride-oxide (ONO) gate insulator 407.

Figure 4B illustrates an electrical equivalent circuit 400 for the portion of the memory array shown in Figure 4A. As shown in Figure 4B, a number of vertical multiple bit cells, 401-1, 401-2, 401-3, . . ., 401-N, are provided. Each vertical multiple bit cell, 401-1, 401-2, 401-3, . . ., 401-N, includes a first source/drain region, 402, a second source/drain region 406, a channel region 405 between the first and the second source/drain regions, and a gate 409 separated from the channel region by a gate insulator 407. A first and a second storage region, shown generally as 417, exist in the gate insulator 407 as described herein.

Figure 4B further illustrates a number of first and second transmission lines, bit lines or data lines, 404 and 411, are coupled to the first and the second source/drain regions, 402 and 406 respectively, of each multiple bit cell 401-1, 401-2, 401-3, . . ., 401-N. In one embodiment, as shown in Figure 4B, the number of first and second transmission lines, bit lines or data lines, 404 and 411, are coupled to the first and the second source/drain regions, 402 and 406

respectively, along columns of the memory array. A number of word lines, such as wordlines 413-1, 413-2, 413-3, . . ., 413-N, in Figure 4B, are coupled to the gates 409 of each multiple bit cell along rows of the memory array.

The electrical equivalent circuit of Figure 4B shows the electrical connections in the array. The number of first and second transmission lines, bit lines or data lines, 404 and 411, form a virtual ground in that either one can be grounded depending upon in which direction the transistor is being operated. The transistor is stressed by grounding one line and applying a gate and drain voltage. To read this state the drain and ground are interchanged and the conductivity of the transistor determined. Alternatively, the device can be stressed and read in the opposite direction.

For example, in one embodiment a first write mode, e.g. programming in a first direction, includes creating a hot electron injection into the gate insulator of the one or more vertical MOSFETs and trapping a charge in the first storage region in the gate insulator adjacent to the second source/drain region. In this example, data line 411 will be driven with a high voltage potential, VDD, and the other data line 404 will be held at a ground potential. When a given multiple bit cell 401-1, 401-2, 401-3, . . ., 401-N is addressed using a cell associated wordline, e.g 413-1, 413-2, 413-3, . . ., 413-N, hot electron injection occurs trapping a charge in a first storage region, within 417, in the gate insulator 407 adjacent to the second source/drain region 406. Subsequently, when the multiple bit cell 401-1, 401-2, 401-3, . . ., 401-N is read in the first direction, data line 404 is precharged to a fractional voltage of VDD, data line 411 is grounded, and the cell addressed using a cell associated wordline, e.g 413-1, 413-2, 413-3, . . ., 413-N. The multiple bit cell 401-1, 401-2, 401-3, . . ., 401-N now has a first threshold voltage region (Vt1) adjacent to the first source/drain region 402 and a second threshold voltage region (Vt2) adjacent to the second source/drain region 406, wherein Vt2 is greater than Vt1, and the multiple bit cell 401-1, 401-2, 401-3, . . ., 401-N operates at reduced drain source current reflecting a stored charge trapped in the first storage region, within 417, in the gate insulator 407 adjacent the second source/drain region 406.

Conversely, the multiple bit cell 401-1, 401-2, 401-3, . . ., 401-N is programmed, or written to, and read in a second direction by performing reciprocal actions to those described above. That is, when programming in a second direction, a high voltage potential (VDD) is applied to the first source/drain region 402 of the vertical multiple bit cell, the second source/drain region 406 is grounded, and a gate potential is applied to the gate in order to create a conduction channel between the first and the second source/drain regions of the vertical multiple bit cell. As one or ordinary skill in the art will appreciate upon reading this disclosure, programming in a second direction includes creating a hot electron injection into the gate insulator of the one or more vertical multiple bit cells in a second storage region. This includes trapping a charge in the second storage region in the gate insulator adjacent to the first source/drain region such that when the multiple bit cell is read in the second direction the multiple bit cell has a first threshold voltage region (Vt1) adjacent to the first source/drain region 402 and a second threshold voltage region (Vt2) adjacent to the second source/drain region 406. Here, Vt1 is greater than Vt2 and the MOSFET operates at reduced drain source current when the the first source/drain region 402 is operated as the source region.

In this manner, charge can be stored in either end of the channel 405. As one of ordinary skill in the art will understand according to the teachings of the present invention, there is no interference between the two different storage states since charge stored near the drain has little effect on the transistor's conductivity when it is operated in the saturation region. The devices can be erased by applying a large negative voltage to the gate and positive voltage to the first and/or second source/drain region. The coincidence of gate and first or second source/drain bias at the same location can erase a transistor at this location, but the gate bias alone or first and/or second source/drain region bias alone is not sufficient to disturb or erase the charge storage state of other transistors in the array. This results in the ability of each transistor to store two bits of data and a higher memory density results in terms of bits per unit area.

Hence, when a multiple bit cell 401-1, 401-2, 401-3, . . ., 401-N is addressed its conductivity will be determined by the presence or absence of a

charge stored in the first or second storage region adjacent to the first or the second source/drain region serving as the source region as measured or compared to a reference or dummy cell and so detected using a sense amplifier. The operation of DRAM sense amplifiers is described, for example, in U.S. Pat. Nos. 5,627,785; 5,280,205; and 5,042,011, all assigned to Micron Technology Inc., and incorporated by reference herein. The array would thus be addressed and read in the conventional manner used in DRAM's, but programmed as multiple bit cells in a novel fashion.

The write and possible erase feature could be used during manufacture and test to initially program all cells or devices to have similar or matching conductivity before use in the field. Likewise, the transistors in the reference or dummy cells can all initially be programmed to have the same conductivity states. According to the teachings of the present invention, a sense amplifier can detect small differences in cell or device characteristics due to stress induced changes in device characteristics during the write operation.

In one embodiment, trapping a charge in the gate insulator adjacent to the second source/drain region includes increasing a normal threshold voltage in the Vt2 by approximately 0.5 Volts when the multiple bit cell is read in the first direction. In one embodiment, reading the one or more MOSFETs in the first and the second directions includes using a sense amplifier to detect a change in an integrated drain current. When read in a first direction, with no charge trapped in the first storage region adjacent the second source/drain region 406, the multiple bit cell will exhibit a change in an integrated drain current of approximately 12.5 μA when addressed over approximately 10 ns.

In one embodiment, trapping a charge in the gate insulator adjacent to the first source/drain region 402 includes increasing a normal threshold voltage in the Vt1 by approximately 0.5 Volts when the MOSFET is read in the first direction. In one embodiment, reading the one or more MOSFETs in the first and the second directions includes using a sense amplifier to detect a change in an integrated drain current. When read in a second direction, with no charge trapped in the second storage region adjacent the first source/drain region, the

multiple bit cell will exhibit a change in an integrated drain current of approximately 12.5 μA when addressed over approximately 10 ns.

As one of ordinary skill in the art will understand upon reading this disclosure such arrays of multiple bit cells are conveniently realized by a modification of DRAM technology. According to the teachings of the present invention a gate insulator of the multiple bit cell includes gate insulators selected from the group of thicker layers of SiO_2 formed by wet oxidation, SON silicon oxynitride, SRO silicon rich oxide, Al_2O_3 aluminum oxide, composite layers and implanted oxides with traps (L. Forbes and J. Geusic, "Memory using insulator traps," Micron disclosure 97-0049, US Patent 6,140,181 October 31, 2000). Conventional transistors for address decode and sense amplifiers can be fabricated after this step with normal thin gate insulators of silicon oxide.

Figures 5A-B and 6 are useful in illustrating the use of charge storage in the gate insulator to modulate the conductivity of the vertical multiple bit cell according to the teachings of the present invention. That is, Figures 5A-5B illustrates the operation of the novel vertical multiple bit cell 501 formed according to the teachings of the present invention. And, Figure 6 illustrates the operation of a conventional DRAM cell 601. As shown in Figure 5A, the gate insulator 502 is made thicker than in a conventional DRAM cell, e.g. 502 is equal to or greater than 10nm or 100 Å (10^{-6} cm). In the embodiment shown in Figure 5A a vertical multiple bit cell is illustrated having dimensions of 0.1 μm (10^{-5} cm) by 0.1 μm. The capacitance, Ci, of the structure depends on the dielectric constant, ϵ_i, (given here as 0.3×10^{-12} F/cm), and the thickness of the insulating layers, t, (given here as 10^{-6} cm), such that $Ci = \epsilon i/t$, Farads/cm^2 or 3×10^{-7} F/cm^2. In one embodiment, a charge of 10^{12} electrons/cm^2 is programmed into the first or the second storage regions in the gate insulator of the vertical multiple bit cell. This produces a stored charge $\Delta Q = 10^{12}$ electrons/cm^2 x 1.6 x 10^{-19} Coulombs. In this embodiment, the resulting change in the threshold voltage (Δ Vt)of the vertical multiple bit cell will be approximately 0.5 Volts ($\Delta Vt = \Delta Q/Ci$ or $1.6 \times 10^{-7} / 3 \times 10^{-7} = ½$ Volt). In effect, the programmed vertical multiple bit cell, or modified MOSFET is a programmed MOSFET having a charge trapped in the gate insulator adjacent to a first or a second source/drain

region, serving as a source region, such that the channel region has a first voltage threshold region (Vt1) and a second voltage threshold region (Vt2), where Vt2 is greater than Vt1, and Vt2 is adjacent the first or the second source/drain region, serving as the source region, such that the programmed MOSFET operates at reduced drain source current. For $\Delta Q = 10^{12}$ electrons/cm^2 in the dimensions given above, this embodiment of the present invention involves trapping a charge of approximately 100 electrons in the gate insulator of the vertical multiple bit cell adjacent either the first or the second source/drain region depending on in which direction the multiple bit cell is operated.

Figure 5B aids to further illustrate the conduction behavior of the novel vertical multiple bit cell of the present invention. As one of ordinary skill in the art will understand upon reading this disclosure, if the vertical multiple bit cell is being driven with a gate voltage of 1.0 Volt (V) and the nominal threshold voltage without the gate insulator charged is ½ V, then if the storage region in the gate insulator, adjacent either the first or the second source/drain region serving as the source region, is charged the transistor of the present invention will be off and not conduct. That is, by trapping a charge of approximately 100 electrons in the gate insulator of the vertical multiple bit cell, having dimensions of 0.1 μm (10^{-5} cm) by 0.1 μm, will raise the threshold voltage of the vertical multiple bit cell to 1.0 Volt and a 1.0 Volt gate potential will not be sufficient to turn the device on, e.g. Vt = 1.0 V, I = 0.

Conversely, if the nominal threshold voltage without the gate insulator charged is ½ V, then $I = \mu C_{ox} \times (W/L) \times ((Vgs - Vt)^2/2)$, or 12.5 μA, with $\mu C_{ox} = \mu C_i = 100\ \mu A/V^2$ and W/L =1. That is, the vertical multiple bit cell of the present invention, having the dimensions describe above will produce a current $I = 100\ \mu A/V^2 \times (1/4) \times (½) = 12.5\ \mu A$ when the charge storage region in the gate insulator adjacent either the first or the second source/drain region serving as the source, is not charged. Thus, in the present invention an un-written, or un-programmed storage region the gate insulator adjacent either the first or the second source/drain region serving as the source, can conduct a current of the order 12.5uA and a charge stored in the other storage region of the gate insulator, adjacent either the first or the second source/drain region serving as the drain,

will not significantly affect the conduction. If the particular storage region in the gate insulator, adjacent either the first or the second source/drain region serving as the source, is charged then the vertical multiple bit cell will not conduct. As one of ordinary skill in the art will understand upon reading this disclosure, the sense amplifiers used in DRAM arrays, and as describe above, can easily detect such differences in current on the bit lines.

By way of comparison, in a conventional DRAM with 30 femtoFarad (fF) storage capacitors charged to 50 femtoColumbs (fC), if these are read over 5 nS then the average current on the bit line is only 10 μA. This is illustrated in connection with Figure 6. As shown in Figure 6, storing a 50 fC charge on the storage capacitor equates to storing 300,000 electrons.

According to the teachings of the present invention, the transistors in the array are utilized not just as passive on or off switches as transfer devices in DRAM arrays but rather as active devices providing gain. In the present invention, to program the transistor "off," requires only a stored charge in the storage region in the gate insulator, adjacent either the first or the second source/drain region serving as the source, of about 100 electrons if the area is 0.1 μm by 0.1 μm. Conversely, if the particular storage region of the vertical multiple bit cell is un-programmed, e.g. no stored charge trapped in therein, and if the transistor is addressed over 10 nS, a current of 12.5 μA is provided. The integrated drain current then has a charge of 125 fC or 800,000 electrons. This is in comparison to the charge on a DRAM capacitor of 50 fC which is only about 300,000 electrons. Hence, the use of the transistors in the array as active devices with gain, rather than just switches, provides an amplification of the stored charge, in the gate insulator, from 100 to 800,000 electrons over a read address period of 10 nS.

The retention of the memory devices depends on mobility degradation, which is for all intensive purposes probably permanent and trapped charge which won't decay with zero or positive gate bias. There are some design considerations involved in that the easier programming with SON and/or SRO insulators will result in shorter retention times.

In Figure 7 a memory device is illustrated according to the teachings of the present invention. The memory device 740 contains a memory array 742, row and column decoders 744, 748 and a sense amplifier circuit 746. The memory array 742 consists of a plurality of vertical multiple bit cell cells 700, formed according to the teachings of the present invention whose word lines 780 and bit lines 760 are commonly arranged into rows and columns, respectively. The bit lines 760 of the memory array 742 are connected to the sense amplifier circuit 746, while its word lines 780 are connected to the row decoder 744. Address and control signals are input on address/control lines 761 into the memory device 740 and connected to the column decoder 748, sense amplifier circuit 746 and row decoder 744 and are used to gain read and write access, among other things, to the memory array 742.

The column decoder 748 is connected to the sense amplifier circuit 746 via control and column select signals on column select lines 762. The sense amplifier circuit 746 receives input data destined for the memory array 742 and outputs data read from the memory array 742 over input/output (I/O) data lines 763. Data is read from the cells of the memory array 742 by activating a word line 780 (via the row decoder 744), which couples all of the memory cells corresponding to that word line to respective bit lines 760, which define the columns of the array. One or more bit lines 760 are also activated. When a particular word line 780 and bit lines 760 are activated, the sense amplifier circuit 746 connected to a bit line column detects and amplifies the conduction sensed through a given vertical multiple bit cell, where in the read operation the source region of a given cell is couple to a grounded array plate (not shown), and transferred its bit line 760 by measuring the potential difference between the activated bit line 760 and a reference line which may be an inactive bit line. The operation of memory device sense amplifiers is described, for example, in U.S. Pat. Nos. 5,727,785; 5,280,205; and 5,042,011, all assigned to Micron Technology Inc., and incorporated by reference herein.

Figure 8 is a block diagram of an electrical system, or processor-based system, 800 utilizing vertical multiple bit cell 812 constructed in accordance with the present invention. That is, the vertical multiple bit cell 812 utilizes the

modified DRAM cell as explained and described in detail in connection with Figures 2-4. The processor-based system 800 may be a computer system, a process control system or any other system employing a processor and associated memory. The system 800 includes a central processing unit (CPU) 802, e.g., a microprocessor, that communicates with the vertical multiple bit cell 812 and an I/O device 808 over a bus 820. It must be noted that the bus 820 may be a series of buses and bridges commonly used in a processor-based system, but for convenience purposes only, the bus 820 has been illustrated as a single bus. A second I/O device 810 is illustrated, but is not necessary to practice the invention. The processor-based system 800 can also includes read-only memory (ROM) 814 and may include peripheral devices such as a floppy disk drive 804 and a compact disk (CD) ROM drive 806 that also communicates with the CPU 802 over the bus 820 as is well known in the art.

It will be appreciated by those skilled in the art that additional circuitry and control signals can be provided, and that the memory device 800 has been simplified to help focus on the invention. At least one of the vertical multiple bit cells in NROM 812 includes a programmed MOSFET having a charge trapped in the charge storage region in the gate insulator, adjacent either the first or the second source/drain region serving as the source, such that the channel region has a first voltage threshold region (Vt1) and a second voltage threshold region (Vt2), where Vt2 is greater than Vt1, and Vt2 is adjacent the source region such that the programmed MOSFET operates at reduced drain source current.

It will be understood that the embodiment shown in Figure 8 illustrates an embodiment for electronic system circuitry in which the novel memory cells of the present invention are used. The illustration of system 800, as shown in Figure 8, is intended to provide a general understanding of one application for the structure and circuitry of the present invention, and is not intended to serve as a complete description of all the elements and features of an electronic system using the novel memory cell structures. Further, the invention is equally applicable to any size and type of memory device 800 using the novel memory cells of the present invention and is not intended to be limited to that described above. As one of ordinary skill in the art will understand, such an electronic

system can be fabricated in single-package processing units, or even on a single semiconductor chip, in order to reduce the communication time between the processor and the memory device.

Applications containing the novel memory cell of the present invention as described in this disclosure include electronic systems for use in memory modules, device drivers, power modules, communication modems, processor modules, and application-specific modules, and may include multilayer, multichip modules. Such circuitry can further be a subcomponent of a variety of electronic systems, such as a clock, a television, a cell phone, a personal computer, an automobile, an industrial control system, an aircraft, and others.

Conclusion

Utilization of a modification of well established DRAM technology and arrays will serve to afford an inexpensive memory device. Two transistors occupy an area of 4F squared when viewed from above, or each transistor has an area of 2F squared. Since each transistor can store two bits the data storage density is one bit for each 1F squared unit area. "F" is the minimum resolvable photolithographic dimension in the particular CMOS technology. If the particular CMOS technology is 0.1 micron, then the data storage density is 10 Gigabit per square centimeter.

It is to be understood that the above description is intended to be illustrative, and not restrictive. Many other embodiments will be apparent to those of skill in the art upon reviewing the above description. The scope of the invention should, therefore, be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.

What is claimed is:

1. A vertical multiple bit cell, comprising:

a vertical metal oxide semiconductor field effect transistor (MOSFET) extending outwardly from a substrate, the MOSFET having a first source/drain region, a second source/drain region, a channel region between the first and the second source/drain regions, and a gate separated from the channel region by a gate insulator;

a first transmission line coupled to the first source/drain region; and

a second transmission line coupled to the second source/drain region;

wherein the MOSFET is a programmed MOSFET having a charge programmed in at least one of a first storage region and a second storage region in the gate insulator and operated with either the first source/drain region or the second source/drain region serving as the source region such that the programmed MOSFET operates at reduced drain source current; and

wherein both the first and second source/drain regions of the MOSFET share a source/drain region with a second MOSFET.

2. The multiple bit cell of claim 1, wherein the first source/drain region of the MOSFET serves as a source region and the second source/drain region of the MOSFET serves as a drain region in a first mode of operation and wherein the first source/drain region of the MOSFET serves as a drain region and the second source/drain region of the MOSFET serves as a source region in a second mode of operation.

3. The multiple bit cell of claim 1, wherein the first transmission line includes a buried bit line.

4. The multiple bit cell of claim 1, wherein the MOSFET includes a charge programmed in both the first storage region and the second storage region.

5. The multiple bit cell of claim 1, wherein the first storage region is adjacent the first source/drain region, and wherein the second storage region is adjacent the second source/drain region.

6. The multiple bit cell of claim 5, wherein the charge programmed in the at least one of the first charge storage region and the second storage region creates a high voltage threshold when the MOSFET is operated with the adjacent first source/drain region or the second source/drain region serving as the source region.

7. The multiple bit cell of claim 1, wherein the gate insulator has a thickness of approximately 10 nanometers (nm).

8. The multiple bit cell of claim 7, wherein the gate insulator includes a gate insulator selected from the group of silicon dioxide (SiO_2) formed by wet oxidation, silicon oxynitride (SON), silicon rich oxide (SRO), and silicon rich aluminum oxide (Al_2O_3).

9. A vertical multiple bit cell, comprising:

a vertical metal oxide semiconductor field effect transistor (MOSFET) extending outwardly from a substrate, the MOSFET having a first source/drain region, a second source/drain region, a channel region between the first and the second source/drain regions, and a gate separated from the channel region by a gate insulator;

a wordline coupled to the gate;

a first transmission line coupled to the first source/drain region; and

a second transmission line coupled to the second source/drain region;

wherein the MOSFET is a programmed MOSFET having a charge programmed both a first storage region and a second storage region in the gate insulator and operated with either the first source/drain region or the second source/drain region serving as the source region such that the channel region has

a first voltage threshold region (Vt1) adjacent to the first source/drain region a second voltage threshold region (Vt2) adjacent to the second source/drain region which vary depending on in which direction the MOSFET is operated; and

wherein the first source/drain region and the second source/drain region of the MOSFET share a first and a second source/drain region respectively from a second MOSFET.

10. The multiple bit cell of claim 9, wherein, the second voltage threshold region (Vt2) in the channel is adjacent the first source/drain region, and wherein the first voltage threshold region (Vt1) in the channel is adjacent the second source/drain region, and wherein Vt2 has a higher voltage threshold than the Vt1 when the MOSFET is operated with the first source/drain region serving as the source region.

11. The multiple bit cell of claim 9, wherein the gate insulator has a thickness of approximately 10 nanometers (nm).

12. The multiple bit cell of claim 9, wherein the gate insulator includes a gate insulator selected from the group of silicon rich aluminum oxide insulators, silicon rich oxides with inclusions of nanoparticles of silicon, silicon oxide insulators with inclusions of nanoparticles of silicon carbide, and silicon oxycarbide insulators.

13. The multiple bit cell of claim 9, wherein the gate insulator includes a composite layer.

14. The multiple bit cell of claim 13, wherein the composite layer includes a composite layer selected from the group of an oxide-aluminum oxide (Al_2O_3)-oxide composite layer, and oxide-silicon oxycarbide-oxide composite layer.

15. The multiple bit cell of claim 13, wherein the composite layer includes a composite layer, or a non-stoichiometric single layer of two or more materials selected from the group of silicon (Si), titanium (Ti), and tantalum (Ta).

16. The multiple bit cell of claim 9, wherein the gate insulator includes a multiple layer of oxide-nitride-oxide (ONO).

17. A memory array, comprising:

a number of vertical multiple bit cells extending from a substrate and separated by trenches, wherein each vertical multiple bit cell includes a first source/drain region, a second source/drain region, a channel region between the first and the second source/drain regions, and a gate separated from the channel region by a gate insulator;

a number of first data lines coupled to the second source/drain region of each multiple bit cell along columns of the memory array;

a number of word lines coupled to the gate of each multiple bit cell along rows of the memory array; and

a number of second data lines coupled to the first source/drain region of each multiple bit cell along columns of the memory array;

wherein at least one of the multiple bit cells is a programmed MOSFET having a charge programmed in at least one of a first storage region and a second storage region in the gate insulator and operated with either the first source/drain region or the second source/drain region serving as the source region such that the programmed MOSFET operates at reduced drain source current; and

wherein the first and second source/drain regions of the MOSFET share both the first and second source/drain regions respectively from another of the vertical multiple bit cells.

18. The memory array of claim 17, wherein the number of second data lines include a buried data lines.

19. The memory array of claim 17, wherein the MOSFET includes a charge programmed in both the first storage region and the second storage region.

20. The memory array of claim 17, wherein the first storage region is adjacent the first source/drain region, and wherein the second storage region is adjacent the second source/drain region.

21. The memory array of claim 20, wherein the charge programmed in the at least one of the first charge storage region and the second storage region creates a high voltage threshold when the MOSFET is operated with the an adjacent first source/drain region or the second source/drain region serving as the source region.

22. The memory array of claim 17, wherein the gate insulator of each multiple bit cell has a thickness of approximately 10 nanometers (nm).

23. The memory array of claim 17, wherein the gate insulator includes a gate insulator selected from the group of silicon dioxide (SiO_2) formed by wet oxidation, silicon oxynitride (SON), and silicon rich aluminum oxide.

24. The memory array of claim 17, wherein the number of vertical multiple bit cells extending from a substrate operate as equivalent to a transistor having a size of 1.0 photolithographic feature squared ($1F^2$).

25. A memory array, comprising:

a number of vertical pillars formed in rows and columns extending outwardly from a substrate and separated by a number of trenches, wherein the number of vertical pillars serve as transistors including a first source/drain region, a second source/drain region, a channel region between the first and the second source/drain regions, and a gate separated from the channel region by a gate insulator in the trenches along columns of pillars, wherein each transistor

has an area of two photolithograpic features squared ($2F^2$) and can store two bits such that a data storage density for each transistor is one bit for each one photolithograpic feature squared ($1F^2$);

a number of first transmission lines coupled to the second source/drain region of each transistor along columns of the memory array;

a number of word lines coupled to the gate of each transistor along rows of the memory array; and

a number of second transmission lines coupled to the first source/drain region of each transistor along columns of the memory array;

wherein at least one of multiple bit cell transistors is a programmed MOSFET having a charge programmed in at least one of a first storage region and a second storage region in the gate insulator and operated with either the first source/drain region or the second source/drain region serving as the source region such that the channel region has a first voltage threshold region (Vt1) adjacent to the first source/drain region a second voltage threshold region (Vt2) adjacent to the second source/drain region which vary depending on in which direction the MOSFET is operated; and

wherein the first and second source/drain regions of the MOSFET share both the first and second source/drain regions respectively from another of the multiple bit cell transistors.

26. The memory array of claim 25, wherein, the second voltage threshold region (Vt2) in the channel is adjacent the first source/drain region, and wherein the first voltage threshold region (Vt1) in the channel is adjacent the second source/drain region, and wherein Vt1 has a higher voltage threshold than the Vt2 when the MOSFET is operated with the second source/drain region serving as the source region.

27. The memory array of claim 25, wherein the number of first transmission lines include a buried data lines.

28. The memory array of claim 25, wherein the MOSFET includes a charge programmed in both the first storage region and the second storage region.

29. The memory array of claim 25, wherein the first storage region is adjacent the first source/drain region, and wherein the second storage region is adjacent the second source/drain region.

30. The memory array of claim 29, wherein the charge programmed in the at least one of the first charge storage region and the second storage region creates a high voltage threshold when the MOSFET is operated with the adjacent first source/drain region or the second source/drain region serving as the source region.

31. An electronic system, comprising:

a processor; and

a memory device coupled to the processor, wherein the memory device includes a memory array, the memory array including;

a number of vertical transistors extending outwardly from a substrate and separated by trenches, wherein each transistor includes a first source/drain region, a second source/drain region, a channel region between the source and the drain regions, and a gate separated from the channel region by a gate insulator;

a number of first transmission lines coupled to the second source/drain region of each vertical transistor along columns of the memory array;

a number of wordlines coupled to the gate of each vertical transistor along rows of the memory array;

a number of second transmission lines coupled to the first source/drain region of each vertical transistor along columns of the memory array;

a wordline address decoder coupled to the number of wordlines;

a first address decoder coupled to the number of first transmission lines;

a second address decoder coupled to the number of second transmission lines; and

a sense amplifier coupled to the first and the second number of transmission lines;

wherein at least one of the transistors is a programmed MOSFET having a charge programmed in at least one of a first storage region and a second storage region in the gate insulator and operated with either the first source/drain region or the second source/drain region serving as the source region such that the channel region has a first voltage threshold region (Vt1) adjacent to the first source/drain region a second voltage threshold region (Vt2) adjacent to the second source/drain region which vary depending on in which direction the MOSFET is operated; and

wherein the first and second source/drain regions of the MOSFET share the first and second source/drain regions respectively from another of the transistors.

32. The electronic system of claim 31, wherein, the second voltage threshold region (Vt2) in the channel is adjacent the first source/drain region, and wherein the first voltage threshold region (Vt1) in the channel is adjacent the second source/drain region, and wherein Vt1 has a higher voltage threshold than the Vt2 when the MOSFET is operated with the second source/drain region serving as the source region.

33. The electronic system of claim 31, wherein the number of first transmission lines include a buried data lines.

34. The electronic system of claim 31, wherein the MOSFET includes a charge programmed in both the first storage region and the second storage region.

35. The electronic system of claim 31, wherein the first storage region is adjacent the first source/drain region, and wherein the second storage region is adjacent the second source/drain region.

36. The electronic system of claim 35, wherein the charge programmed in the at least one of the first charge storage region and the second storage region creates a high voltage threshold when the MOSFET is operated with the an adjacent first source/drain region or the second source/drain region serving as the source region.

37. The electronic system of claim 31, wherein the gate insulator of each transistor includes a gate insulator selected from the group of silicon dioxide (SiO_2) formed by wet oxidation, silicon oxynitride (SON), and silicon rich aluminum oxide.

38. The electronic system of claim 37, wherein the gate insulator of each transistor includes an oxide-nitride-oxide (ONO) insulator.

39. The electronic system of claim 31, wherein each transistor operates as equivalent to a transistor having a size of much less than 1.0 lithographic feature squared ($1F^2$).

40. A method for operating a memory, comprising:

programming one or more vertical MOSFETs extending outwardly from a substrate in a DRAM array to have a storage density of one bit per one photolithographic feature squared unit area, wherein each MOSFET in the DRAM array includes a first source/drain region, a second source/drain region, a channel region between the first and the second source/drain regions, and a gate separated from the channel region by a gate insulator, wherein the first and second source/drain regions of a first MOSFET share the first and second source/drain regions of a second MOSFET, and wherein programming the one or

more vertical MOSFETs includes programming the one or more vertical MOSFETs in a first and a second direction, wherein programming in a first and a second direction includes:

applying a first voltage potential to a first source/drain region of the vertical MOSFET;

applying a second voltage potential to a second source/drain region of the vertical MOSFET;

applying a gate potential to a gate of the vertical MOSFET; and

wherein applying the first, second and gate potentials to the one or more vertical MOSFETs includes creating a hot electron injection into the gate insulator of the one or more MOSFETs such that a programmed MOSFET has a charge programmed in at least one of a first storage region and a second storage region in the gate insulator, and the programmed MOSFET can be operated with either the first source/drain region or the second source/drain region serving as the source region.

41. The method of claim 40, wherein when programming in a first direction, applying a first voltage potential to the first source/drain region of the vertical MOSFET includes grounding the first source/drain region of the vertical MOSFET, applying a second voltage potential to the second source/drain region includes applying a high voltage potential (VDD) to the second source/drain region, and applying a gate potential to the gate in order to create a conduction channel between the first and the second source/drain regions of the vertical MOSFET.

42. The method of claim 41, wherein the method further includes reading one or more vertical MOSFETs in the DRAM array in a first direction, wherein reading one or more vertical MOSFETs in the first direction includes:

grounding the second source/drain region;

precharging the first source/drain region to a fractional voltage of VDD; and

applying a gate potential of approximately 1.0 Volt to the gate.

43. The method of claim 42, wherein when programming in a first direction, creating a hot electron injection into the gate insulator of the one or more vertical MOSFETs includes trapping a charge in the first storage region in the gate insulator adjacent to the second source/drain region such that when the MOSFET is read in the first direction the MOSFET has a first threshold voltage region (Vt1) adjacent to the first source/drain region and a second threshold voltage region (Vt2) adjacent to the second source/drain region, wherein Vt2 is greater than Vt1 and the MOSFET operates at reduced drain source current.

44. The method of claim 43, wherein trapping a charge in the gate insulator adjacent to the second source/drain region includes increasing a normal threshold voltage in the Vt2 by approximately 0.5 Volts when the MOSFET is read in the first direction.

45. The method of claim 44, wherein reading the one or more MOSFETs in the first and the second directions includes using a sense amplifier to detect a change in an integrated drain current, and wherein when read in a first direction the MOSFET will exhibit a change in an integrated drain current of approximately 12.5 μA when addressed over approximately 10 ns when no charge is programmed in the first charge storage region.

46. The method of claim 40, wherein when programming in a second direction, applying a first voltage potential to the first source/drain region of the vertical MOSFET includes applying a high voltage potential (VDD) to the first source/drain region of the vertical MOSFET, applying a second voltage potential to the second source/drain region includes grounding the second source/drain region, and applying a gate potential to the gate in order to create a conduction channel between the first and the second source/drain regions of the vertical MOSFET.

47. The method of claim 46, wherein the method further includes reading one or more vertical MOSFETs in the DRAM array in a second direction, wherein reading one or more vertical MOSFETs in the second direction includes:

grounding the first source/drain region;

precharging the second source/drain region to a fractional voltage of VDD; and

applying a gate potential of approximately 1.0 Volt to the gate.

48. The method of claim 47, wherein when programming in a second direction, creating a hot electron injection into the gate insulator of the one or more vertical MOSFETs includes trapping a charge in the second storage region in the gate insulator adjacent to the first source/drain region such that when the MOSFET is read in the second direction the MOSFET has a first threshold voltage region (Vt1) adjacent to the first source/drain region and a second threshold voltage region (Vt2) adjacent to the second source/drain region, wherein Vt1 is greater than Vt2 and the MOSFET operates at reduced drain source current.

49. The method of claim 48, wherein trapping a charge in the gate insulator adjacent to the first source/drain region includes increasing a normal threshold voltage in the Vt1 by approximately 0.5 Volts when the MOSFET is read in the first direction.

50. The method of claim 49, wherein reading the one or more MOSFETs in the first and the second directions includes using a sense amplifier to detect a change in an integrated drain current, and wherein when read in a second direction the MOSFET will exhibit a change in an integrated drain current of approximately 12.5 μA when addressed over approximately 10 ns when no charge is programmed in the second charge storage region.

51. A method for forming a memory, comprising:

forming a vertical multiple bit cell, wherein forming the vertical multiple bit cell includes;

forming a vertical metal oxide semiconductor field effect transistor (MOSFET) extending outwardly from a substrate, the MOSFET having a first source/drain region, a second source/drain region, a channel region between the first and the second source/drain regions, and a gate separated from the channel region by a gate insulator, wherein the first and second source/drain regions of the MOSFET share the first and second source/drain regions of a second MOSFET respectively;

forming a first transmission line coupled to the first source/drain region;

forming a second transmission line coupled to the second source/drain region; and

wherein forming the MOSFET includes forming a MOSFET adapted to be programmable to have a charge programmed in at least one of a first storage region and a second storage region in the gate insulator and to be operated with either the first source/drain region or the second source/drain region serving as the source region such that the programmed MOSFET operates at reduced drain source current.

52. The method of claim 51, wherein forming the MOSFET includes forming the MOSFET such that the first source/drain region of the MOSFET serves as a source region and the second source/drain region of the MOSFET serves as a drain region in a first mode of operation, and such that the first source/drain region of the MOSFET serves as a drain region and the second source/drain region of the MOSFET serves as a source region in a second mode of operation.

53. The method of claim 51, wherein forming the first transmission line includes forming a buried bit line.

54. The method of claim 51, wherein forming the MOSFET includes forming a MOSFET adapted to be programmed to have charge trapped in both the first storage region and the second storage region.

55. The method of claim 51, wherein forming the MOSFET includes forming the MOSFET such that the first storage region is adjacent the second source/drain region, and such that the second storage region is adjacent the first source/drain region.

56. The method of claim 51, wherein forming the MOSFET includes forming the MOSFET such that the charge programmed in the at least one of the first charge storage region and the second storage region creates a high voltage threshold and operates at a reduced drain source current when the MOSFET is operated with an adjacent one of the first source/drain region or the second source/drain region serving as the source region.

57. The method of claim 51, wherein forming the MOSFET includes forming the MOSFET such that the gate insulator has a thickness of approximately 10 nanometers (nm).

58. The method of claim 51, wherein forming the MOSFET includes forming the MOSFET with a gate insulator selected from the group of silicon dioxide (SiO_2) formed by wet oxidation, silicon oxynitride (SON), silicon rich oxide (SRO), and silicon rich aluminum oxide (Al_2O_3).

59. The method of claim 51, wherein forming the MOSFET includes forming the MOSFET with a gate insulator selected from the group of silicon rich aluminum oxide insulators, silicon rich oxides with inclusions of nanoparticles of silicon, silicon oxide insulators with inclusions of nanoparticles of silicon carbide, and silicon oxycarbide insulators.

60. The method of claim 51, wherein forming the MOSFET includes forming the MOSFET with a composite layer gate insulator.

61. The method of claim 60, wherein forming the MOSFET with a composite layer gate insulator includes forming a composite layer gate insulator selected from the group of an oxide-aluminum oxide (Al_2O_3)-oxide composite layer, and oxide-silicon oxycarbide-oxide composite layer.

62. The method of claim 60, wherein forming the MOSFET with a composite layer gate insulator includes forming a composite layer gate insulator, or a non-stoichiometric single layer, of two or more materials selected from the group of silicon (Si), titanium (Ti), and tantalum (Ta).

63. The method of claim 51, wherein forming the MOSFET includes forming the MOSFET such that the gate insulator includes a multiple layer of oxide-nitride-oxide (ONO).

64. The method of claim 51, wherein forming the MOSFET includes forming a MOSFET having a storage density of one bit for each 1.0 photolithographic feature squared ($1F^2$) unit area.