



(51) International Patent Classification:

H01L 29/78 (2006.01) H01L 21/02 (2006.01)
H01L 33/62 (2010.01)

(21) International Application Number:

PCT/US2024/037384

(22) International Filing Date:

10 July 2024 (10.07.2024)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

63/526,758 14 July 2023 (14.07.2023) US

(71) Applicant: **QROMIS, INC.** [US/US]; 2306 Walsh Avenue, Santa Clara, California 95051 (US).

(72) Inventors: **ODNOBLYUDOV, Vlad**; c/o Qromis, Inc., 2306 Walsh Avenue, Santa Clara, California 95051 (US).
BASCERI, Cem; c/o Qromis, Inc., 2306 Walsh Avenue, Santa Clara, California 95051 (US).

(74) Agent: **WEN, Ruming** et al.; Mailstop: IP Docketing 22, 1100 Peachtree Street, Suite 2800, Atlanta, Georgia 30309 (US).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM,

AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CV, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IQ, IR, IS, IT, JM, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, MG, MK, MN, MU, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, CV, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SC, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, ME, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

(54) Title: METHOD AND SYSTEM FOR VERTICAL FETS FABRICATED ON AN ENGINEERED SUBSTRATE

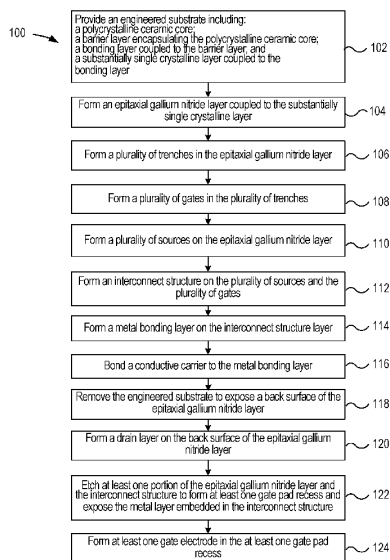


FIG. 1

(57) Abstract: A method of fabricating a semiconductor device includes providing an engineered substrate. The method further includes forming an epitaxial gallium nitride (GaN) layer coupled to the engineered substrate, forming a plurality of trenches in the epitaxial GaN layer, and forming a plurality of gates in the trenches. The method further includes forming a plurality of sources coupled to the epitaxial GaN layer, forming an interconnect structure on the gates and sources, forming a metal bonding layer on the interconnect structure, bonding a conductive carrier to the metal bonding layer, removing the engineered substrate, forming a drain layer on the back surface of the epitaxial GaN layer, etching at least one portion of the epitaxial GaN layer and the interconnect structure to form at least one gate pad recess and expose the embedded metal track; and forming at least one gate electrode in the gate pad recess.