METHOD AND APPARATUS PROVIDING A TWO-WAY SHARED STORAGE GATE ON A FOUR-WAY SHARED PIXEL

FIELD OF THE INVENTION

[0001] The present invention relates generally to digital image sensors and in particular to a CMOS pixel cell array architecture having shared components among pixel cells of the array.

BACKGROUND OF THE INVENTION

[0002] A CMOS imager circuit includes a focal plane array of pixel cells, each one of the cells including a photosensor, for example, a photogate, photoconductor or a photodiode for accumulating photo-generated charge in a specified portion of a substrate. Each pixel cell has a charge storage region, formed on or in the substrate, which is connected to the gate of an output transistor that is part of a readout circuit. The charge storage region may be constructed as a floating diffusion region. In some imager circuits, each pixel may include at least one electronic device such as a transistor for transferring charge from the photosensor to the storage region and one device, also typically a transistor, for resetting the storage region to a predetermined charge level prior to charge transference.

[0003] In a CMOS imager, the active elements of a pixel cell perform the functions of: (1) photon to charge conversion; (2) accumulation of image charge; (3) resetting the storage region to a known state; (4) transfer of charge to the storage region; (5) selection of a pixel for readout; and (6) output and amplification of a signal

representing pixel charge. Photo-charge may be amplified when it moves from the initial charge accumulation region to the storage region. The charge at the storage region is typically converted to a pixel output voltage by a source follower output transistor.

[0004] CMOS imagers of the type discussed above are generally known as discussed, for example, in U.S. Patent no. 6,140,630, U.S. Patent no. 6,376,868, U.S. Patent no. 6,310,366, U.S. Patent no. 6,326,652, U.S. Patent no. 6,204,524 and U.S. Patent no. 6,333,205, assigned to Micron Technology, Inc., which are hereby incorporated by reference in their entirety.

[0005] With reference to FIGS. 1, 2 and 3, which respectively illustrate a top-down view, a partial cross-sectional view and electrical circuit schematic of a conventional four transistor (4T) CMOS pixel sensor cell 100. When incident light 187 strikes the surface of a photosensor (photodiode)120, electron/hole pairs are generated in the p-n junction of the photosensor (represented at the boundary of n-type accumulation region 122 and p-type surface layer 123 (FIG. 2)). The generated electrons (photo-charges) are collected in the n-type accumulation region 122 of the photosensor 120. The photo-charges move from the initial charge accumulation region 122 to a floating diffusion region 110 via a transfer transistor 106. The charge at the floating diffusion region 110 is typically converted to a pixel output voltage by a source follower transistor 108 which is output on a column output line 111 via a row select transistor 109.

[0006] Conventional CMOS imager designs, such as that shown in FIGs. 1-3 for pixel cell 100, provide only approximately a fifty percent fill factor, meaning only half of the pixel cell 100 is utilized in converting light to charge carriers. As shown,

only a small portion of the cell 100 comprises a photosensor 120. The remainder of the pixel cell 100 includes isolation regions 102, shown as STI regions in a substrate 101, the floating diffusion region 110 coupled to a transfer transistor gate 106' of the transfer transistor 106, and source/drain regions 115 for reset 107, source follower 108, and row select 109 transistors having respective gates 107', 108', and 109'. Moreover, as the total pixel area continues to decrease (due to desired scaling), it becomes increasingly important to create high sensitivity photosensors that utilize a minimum amount of surface area or to find more efficient layouts on the pixel array for the non-photosensitive components of the pixel cells to provide increased photosensitive areas.

[0007] FIG. 4 illustrates in electrical schematic form a six transistor (6T) pixel cell having a storage transistor 130 and associated storage gate 130'. Storage transistors 130 having storage gates 130' and associated storage regions may be desirably used for various purposes, such as a frame shutter or to increase the charge capacity of the pixels. In addition, pixel cells also may include an anti-blooming transistor 140 having an associated gate 140' to prevent charge overflow from a charge saturated photosensor 120. However, when additional transistors, such as a storage transistor 130 and/or anti-blooming transistor 140 are added to the pixel cell, the photosensor fill factor in further decreased.

[0008] Accordingly, there is a desire for a pixel cell, which includes storage transistors and/or anti-blooming transistors with associated gates, while having an efficient layout to permit a high fill factor.

BRIEF SUMMARY OF THE INVENTION

[0009] The present invention, in the various exemplary embodiments, provides a method of operating a pixel array including the steps of activating a global storage signal to store a photosensor charge in a first storage region of each pixel of the

array, activating a first reset signal for the pixels in a first row of the array to reset a second storage region of each pixel in the first row, sampling the reset second storage region for the pixels of the first row, activating a third reset signal for the pixels in a second row of the array to reset a third storage region of each pixel in the second row, sampling the reset third storage region for the pixels of the second row, transferring the photosensor charge from the first storage region of each pixel in a first set of columns of the first and second rows of the array respectively to the second and third storage regions for the pixels in the first and second rows, sampling the photosensor charge from the second storage region from the pixels in the first row and first set of columns, and sampling the photosensor charge from the third storage region from the pixels in the second row and first set of columns.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] The foregoing and other aspects of the invention will be better understood from the following detailed description of the invention, which is provided in connection with the accompanying drawings, in which:

[0011] FIG. 1 is a top-down view of a conventional CMOS pixel cell;

[0012] FIG. 2 is a cross-sectional view of the pixel cell of FIG. 1, taken along line 1-1';

[0013] FIG. 3 is a circuit diagram of the conventional CMOS pixel of FIGS. 1 and 2;

[0014] FIG. 4 is a circuit diagram of a conventional CMOS pixel which employs storage and/or anti-blooming transistors with associated gates;

[0015] FIG 5 is a top-down view of a portion of a pixel array constructed in accordance with an exemplary embodiment of the invention;

[0016] FIG. 5A is a schematic view of a portion of a pixel array constructed in accordance with an exemplary embodiment of the invention;

[0017] FIG. 6 is a timing diagram illustrating an exemplary method of operating a pixel array constructed in accordance with the exemplary embodiment of the invention;

[0018] FIG. 7 is a block diagram of a CMOS imager chip having an array of pixel cells constructed in accordance with the invention; and

[0019] FIG. 8 is a schematic diagram of a processing system employing a CMOS imager constructed in accordance with the invention.

DETAILED DESCRIPTION OF THE INVENTION

[0020] In the following detailed description, reference is made to the accompanying drawings, which form a part hereof and show by way of illustration specific embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized, and that structural, logical, and electrical changes may be made without departing from the spirit and scope of the present invention. The progression of processing steps described is exemplary of embodiments of the invention; however, the sequence of steps is not limited to that set forth herein and may be changed as is known in the art, with the exception of steps necessarily occurring in a certain order.

[0021] The terms "wafer" and "substrate," as used herein, are to be understood as including silicon, epitaxial, silicon-on-insulator (SOI) or silicon-on-sapphire (SOS) technology, doped and undoped semiconductors, and other semiconductor structures. Furthermore, when reference is made to a "wafer" or "substrate" in the following description, previous processing steps may have been utilized to form regions, junctions, or material layers in or over the base semiconductor structure or foundation. In addition, the semiconductor need not be silicon-based, but could be based on silicon-germanium, germanium, gallium arsenide or other semiconductors.

[0022] The terms "pixel," or "pixel cell," as used herein, refers to a photo-element unit cell containing a photosensor and associated transistors for converting photons to an electrical signal. For purposes of illustration, a small number of representative pixels are illustrated in the figures and description herein; however, typically fabrication of a large plurality of like pixels proceeds simultaneously. Accordingly, the following detailed description is only exemplary of the invention and is not to be taken as limiting. The scope of the present invention is defined only by the appended claims.

[0023] The terms "at an angle," "angled," and "slanted," as used herein are to be interpreted as meaning at any angle, with respect to some stated reference point, that is not exactly parallel or exactly perpendicular. Accordingly, when at least a portion of an object and some reference point meet to form an angle that is not 0°, 90°, or 180°, the object is considered "angled," "at an angle," or "slanted" with respect to the reference point.

[0024] Now referring to the figures, where like numerals designate like elements, FIG. 5 illustrates a top-down view of a portion of a pixel array 400

constructed in and over a silicon substrate with a pixel layout design in accordance with exemplary embodiments of the present invention. FIG. 5A is a circuit diagram depicting portions of the exemplary pixel array 400. The pixel array 400 includes a sharing of a pixel readout circuit by four pixels. The pixels involved in the four-way readout sharing are represented by photosensors 401, 404, 405, 406. The shared components include pixel signal readout components located on a linearly-extending trunk 450 within the area between a first pair of photosensors 401, 405 and between a second pair of photosensors 404, 406 which are adjacent to the first pair. In addition, optional anti-blooming gates 418, 419, 434, 435 are each also shared by four photosensors in array 400, though not the same four photosensors as share a common readout circuit. In the illustrated example, four photosensors 401, 405, 407, 408 are shown as having a shared anti-blooming gate 418. Photosensors 404, 406, 506, 507 also share anti-blooming gate 419. Anti-blooming gates may overlap associated photosensors as shown in detail by the exemplary dotted lines beneath anti-blooming gate 419. Anti-blooming gates 434, 435 are associated in the illustrated example with respective photosensors 402, 403 and are shared with other photosensors which are not illustrated in FIG. 4.

[0025] It should be noted that FIG. 5A depicts only three rows of a pixel array, Row_{000}, Row_{001}, Row_{002}. As shown, the four-way readout sharing is for pixels in Row_{000} having photo sensors 405, 406 and for pixels in Row_{001} having photosensors 401, 404. In a similar manner, Row_{002}, having pixels with photosensors 402, 403, and Row_{003} (not illustrated) would have pixels sharing a readout circuit.

[0026] Column adjacent pixels (e.g. photosensors 402, 401) share a common first storage gate 409 for storing the generated photo-charges in respective first and second storage regions 413, 413a prior to a readout of the charges. First storage gate 409 may be controlled by global storage gate control signal SG shown in the FIG. 6 timing

diagram explained below. The photosensors 401, 402 may be any photosensitive structure for converting light photons into electrons (photo-charges), and in a preferred embodiment, the photosensors, e.g. 401, 402, are photodiode regions.

[0027] A second storage gate 410 is shared by a second pair of column adjacent photosensors 403, 404. Charge from the photosensors 403, 404 are stored under control of gate 410 in respective third and fourth storage regions 414, 414a. Storage gate 410 may also controlled by the global storage gate control signal SG. Photosensors 405, 504 share a third storage gate 411 with their respective charges stored under control of gate 411 in respective fifth and a sixth storage regions 415a, 415. Photosensors 406, 505 share a fourth storage gate 412 with their respective charges stored in a seventh and an eighth storage regions 416a, 416. The shared storage gate configuration reduces the number of storage gate control signal lines that would otherwise be required with separate storage gates for each photosensor. At least a portion of each of the gates 409, 410, 411, 412 have side edges 431 which are preferably at an angle and at a corner with respect to the photosensors 401, 402, 403, 404, 405, 406, 504, 505, which provides for a larger photon collection area for the photosensors and, consequently, high fill factor. It should be understood that the storage regions 413, 413a, 414, 414a, 415, 415a, 416, 416a primarily comprise a doped region (n-type) located under the respective storage gates 409, 410, 411, 412 in the substrate.

[0028] As illustrated in FIGs. 5 and 5A, photosensors 401, 402 also share a transfer transistor gate 423, photosensors 403, 404 share a transfer transistor gate 424, and photosensors 405, 504 share a transfer gate 425, and photosensors 406, 505 share a transfer gate 426. At least a portion of each of the transfer transistor gates 423, 424, 425, 426 have side edges 432 preferably at an angle and at a corner with respect to each of the photosensors 401, 402, 403, 404, 405, 406, 504, 505. It should be noted that the transfer transistor gates 423, 424, 425, 426 of this embodiment are being shared, each

among two column adjacent pixels in array 400. For example, as shown in FIG. 5, column adjacent photosensors 401, 402, which share storage gate 409, also share the transfer transistor gate 423. The transfer transistor gates 423, 424 transfer charges from charge storage regions 413a, 414a to a common floating diffusion region 421a.

[0029] Photosensors 401, 402 do not share a floating diffusion region or readout circuit. Rather, in the illustrated embodiment, two row adjacent pixels having photosensors 401, 404 share a first floating diffusion region 421a and two row adjacent photosensors 405, 406 share a second floating diffusion region 421b. The two floating diffusion regions 421a, 421b are electrically connected to one another, either by conductive trace or a doped region in the substrate. The floating diffusion regions 421a, 421b may also optionally be coupled to a capacitor 429 which serves to increase the charge storage capacity of the connected floating diffusion regions 421a, 421b. Capacitor 429 is also coupled to Vaa-pix and increases dynamic range. FIG. 5 also shows a third floating diffusion region 430 which is shared by row adjacent photosensors 402, 403. This region is connected to another floating diffusion region, in the same manner that regions 421a and 421b are connected.

[0030] The use of storage gates 409, 410, 411, 412 in association with storage regions 413a, 414a, 415a, 416a provides for a frame shutter and/or additional storage for photosensor charge storage for the pixels which share a readout circuit which include photosensors 401, 404, 405, 406. For example, the storage gates 409, 410, 411, 412 transfer the charges generated by the photosensors 401, 404, 405, 406 following an integration period into the associated storage region 413a, 414a, 415a, 416a, where they can be stored and read out.

[0031] Preferably, as shown in FIG. 5, each of the storage gates 409, 410, 411, 412 and transfer transistor gates 423, 424, 425, 426 have at least a portion thereof

that is angled with respect to their associated photosensors 401, 402, 403, 404, 405, 406, 504, 505 so that each gate overlaps a corner region of an associated photosensor. For example, the edges 431 of the storage gate 410 are shown as being slanted with respect to the length L and the width W of the associated photosensors 403, 404 such that gate 410 overlaps an upper right-hand corner of photosensor 404 and an upper left-hand corner of photosensor 403. Similarly, each of the transfer transistor gates 423, 424, 425, 426 has an edge 432 that is similarly slanted with respect to the length L and the width W of the photosensors 403, 404 such that the gate overlaps a corner of an associated photosensor. This preferred angled geometry and photosensor overlap of the gates 409, 410, 411, 412, 423, 424, 425, 426 allows for an efficient layout of the gates 409, 410, 411, 412, 423, 424, 425, 426, to improve the leakage and lag performance of the pixels in array 400. In addition, this arrangement is also beneficial in maximizing the fill factor of array 400, by maximizing the area of the photosensors 401, 402, 403, 404, 405, 406, 504, 505. The anti-blooming gates 418, 419, 434, 435 of the optional anti-blooming transistors also have slanted edges, e.g. 418a, and also overlap a corner of an associated photosensor, e.g. 407.

[0032] The shared pixel readout structure will now be further described. One reset transistor having a gate 436 is utilized for resetting charges at the interconnected floating diffusion regions 421a, 421b. To one side of the reset gate 436 is a source/drain region 425 that is capable of receiving a supply voltage Vaa-pix. The remaining readout components on the readout trunk 450 shared among photosensors 401, 404, 405, 406 include a source follower transistor 426' having a gate 426 connected to the floating diffusion regions 421a, 421b, and a row select transistor 427' having a gate 427 which selectively gates the output of the source follower transistor 426' to a readout column line. Isolation regions 433 in the substrate are utilized to isolate the active areas on the trunk 450 from the photosensors, and to also isolate the individual

charge accumulation regions of photosensors 401, 404, 405, 406 from one another. Any known isolation technique, including but not limited to shallow trench isolation (STI), may be used to form isolation regions 433.

[0033] The four-way shared pixel readout layout described herein illustratively has a first pair of column-adjacent pixels having respective photosensors 405, 406 and a second pair of column adjacent pixels having respective photosensors 401, 404 sharing one set of readout circuitry, e.g. trunk 450 leading to a column output line 420 . Thus, a column output line 420 is only necessary, in accordance with this exemplary embodiment, for every other column of a pixel array 400. As such, two column-adjacent pixels, e.g. 405, 401 will be sequentially read onto the same output line 420, and their respective signals need to be separately sampled and held in order to maintain maximum resolution for the pixel array 400. Sample and hold circuit 635 (FIG. 5) is connected to a column line 420 and comprises switch 636 and two sets of capacitors 637, 638. Switch 636 determines whether the incoming signal from the column line 420 should go to the first set of capacitors 637 or the second set of capacitors 638. In practice, each pixel, as represented by a respective photosensor and the associated readout circuit, produces two output signals, a reset signal Vrst after the common floating diffusion region 421a, 421b is reset by the rest transistor , e.g. 436', and a photosensor signal Vsig produced by charges accumulated in a photosensor, e.g. 401, during an integration period. A difference signal Vrst – Vsig is produced by differential amplifier 640 for each pixel. Vrst – Vsig represents the amount of light impinging on a pixel. Accordingly, each pair of capacitors 637 and 638 receives at one capacitor of the pair a signal Vrst and at another capacitor of the pair a signal Vsig, for one of two column adjacent pixels.

[0034] FIG. 6 is a timing diagram illustrating an exemplary operation of the array 400 illustrated in FIGs. 5 and 5A. It should be noted that the transfer transistor

gate signal lines TX_ODD, TX_EVEN, respectively represent the transfer control signal for the odd or even pixel columns in the array 400. Further, "Row_{xxx}" is used to designate row number "xxx" of the array 400. It should be noted that the timing diagram of FIG. 6 represents only one exemplary way of operating the structure depicted in FIGs. 5 and 5A and other operational schemes may be employed.

[0035] Global storage gate control signal SG is turned to high ending a photosensor integration period and charges from all photosensors are transferred through the storage gates into their respective storage regions. In this example, charge from photosensor 401 is transferred to storage region 413a, charge from photosensor 402 is transferred to storage region 413, charge from photosensor 403 is transferred to storage region 414, charge from photosensor 404 is transferred to storage region 414a, charge from photosensor 405 is transferred to storage region 415a, charge from photosensor 406 is transferred to storage region 416a, charge from photosensor 504 is transferred to storage region 415a, and charge from photosensor 505 is transferred to storage region 416a.

[0036] Subsequently, for row Row_{001} of the array 400 containing photosensors 401, 404, a row select gate 427 is activated by asserting a row select signal (ROW) high. A reset of the common floating diffusion region 421a, 421b is performed by activating reset gate 436 of reset transistor 436 with reset signal Reset. A signal Vrst representing the reset condition is read out onto column line 420 and is sampled and held on the Vrst capacitor of capacitor pair 638 in sample and hold circuit 635 by sample and hold reset signal SHR. The In_sel signal controls switch 636 to determine whether the signal on column line 420 should go to the first set of capacitors 637 or the second set of capacitors 638. For Row_{001}, In_sel is low controlling storage of the reset signal into the reset signal capacitor of capacitor set 638 (FIG. 5A). Then, for a next row, Row_{002} this same sequence of steps is repeated, turning the appropriate row select (RS)

537, reset (Reset) 536, and sample and hold reset (SHR) signals high for a second row Row_{002} to read out a reset signal onto the column line 420 for a reset condition of the floating diffusion region 430 for Row_{002}, and a connected floating diffusion region of Row_{003}, which is not shown in FIG. 5A. This time, however, the In_sel signal is high, causing the signal to be stored in a reset capacitor of pair 637. Then, the row select and sample and hold signals ROW and SHS return to low.

[0037] Next, a transfer signal TX_EVEN is turned to high, to activate the even column transfer transistor gates 424 in two adjacent rows. Charges stored in the storage area 414a are thus transferred through the transfer transistor 424' into a floating diffusion region 421a and similarly for the charges generated by photosensor 403 in the next row Row_{002} by turning "on" transfer transistor gate 424. Next, for Row_{001}, a pixel voltage signal V_{sig} is read onto the column line 420 by activating the row select transistor 427' with the signal ROW, and sample and hold circuit 635 with a high SHS signal to sample the first row. This is done while the In_sel signal is low which selects the capacitor set 638 through switch 636. As a readout the photosensor 404 signal Vsig is stored on the Vsig capacitor of capacitor set 628. Capacitor set 638 now holds the reset signal Vrst and the photosensor signal Vsig corresponding to photosensor 404. For Row_{002}, a pixel voltage signal V_{sig} is now read out repeating the pulsing of row select (ROW) and sample and hold signals (SHS). From floating diffusion region 430, a signal is generated by source follower transistor gate 526, through row select transistor 537 and onto the column line 420. During this readout, however, the In_sel signal is returned to high to store the photosensor signal Vsig from Row_{002} into the Vsig capacitor of capacitor set 627. The row select and sample and hold signals ROW and SHS return again to low.

[0038] This exemplary method is performed simultaneously for every other column in a row, utilizing the alternative transfer transistor gate signal TX_ODD to

activate transfer transistor gates in odd columns of the array. The method is repeated in this sequence for each pair of rows (e.g. Row_{001} and Row_{002}, Row_{003} and Row_{004}, etc.) until signals are read out for each pixel in array 400. It should be understood that these operational steps are exemplary only, and the invention is in no way limited to the method of readout operation as described herein.

[0039] FIGs. 5 and 5A also illustrate antiblooming gates, e.g. 418, 434, 419, 435 (FIG. 5), and assorted antiblooming transistors. The gates of the antiblooming transistors are operated by control signals on lines HDR (FIG. 5A) to limit the amount of charge which is accumulated by corresponding photosensors, e.g. 406, 404, 401, 405, during a charge integration period. The antiblooming gate may also be used as a global reset gate to begin the integration period.

[0040] FIG. 7 shows a CMOS imager 600 in which the invention may be employed within pixel array 605. The CMOS imager 600 is operated by a control circuit 630, which controls address decoders 615, 625 for selecting the appropriate row and column lines for pixel readout. Control circuit 630 also controls the row and column driver circuitry 610, 620 so that they apply driving voltages to the drive transistors of the selected row and column lines. As noted, the pixel output signals include a pixel reset signal Vrst read out of a floating diffusion region, e.g. 421a, 421b, after it is reset by the reset transistor and a pixel image signal Vsig, which is read out of the floating diffusion region after photo-generated charges are transferred there by a transfer gate from a storage region controlled by a storage gate. For each pixel, the Vrst and Vsig signals are sampled by the sample and hold circuit 635 and are subtracted by a differential amplifier 640, to produce a differential signal Vrst – Vsig representing the amount of light impinging on the pixels. This difference signal is digitized by an analog-to-digital converter 645. The digitized pixel signals are fed to an image processor 650 to form a digital image output. The digitizing and image processing can

be located on or off the imager chip. In some arrangements the differential signal Vrst – Vsig can be amplified as a differential signal and directly digitized by a differential analog to digital converter.

[0041] FIG. 8 illustrates an imaging processor-based system 700, for example a camera system, which generally comprises a central processing unit (CPU) 705, such as a microprocessor, that communicates with an input/output (I/O) device 710 over a bus 715. The system 700 also includes an imaging device 600 constructed in accordance with the embodiments of the invention described herein. Imager 600 also communicates with the CPU 705 over bus 715. The processor-based system 700 also includes random access memory (RAM) 720, and can include removable memory 725, such as flash memory, which also communicate with CPU 705 over the bus 715. Imager 600 may be combined with a processor, such as a CPU, digital signal processor, or microprocessor, with or without memory storage on a single integrated circuit or on a different chip than the processor.

[0042] The invention further includes a method of operating a pixel array of the embodiments illustrated in FIGs. 5-8. The method comprises the steps of generating charge in response to applied light in a first photosensor, generating charge in response to applied light in a second photosensor, and storing charge from the first and second photosensors in respective first and second storage regions with a first and second storage transistor having a common first storage gate respectively connected to the first and second photosensors. The first and second photosensors are column adjacent.

[0043] The processes and devices described above illustrate preferred methods and typical devices of many that could be used and produced. The above description and drawings illustrate embodiments, which achieve the objects, features,

and advantages of the present invention. However, it is not intended that the present invention be strictly limited to the above-described and illustrated embodiments. For example, although the invention is discussed only with reference to pixel arrays having a 4-pixel sharing of a readout circuit and a two-pixel sharing of storage and transfer gates, other multi-pixel sharing arrays are also intended to be within the scope of the invention. Additionally, any modifications, though presently unforeseeable, of the present invention that come within the spirit and scope of the following claims should be considered part of the present invention.

CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method of operating a pixel array comprising the steps of:

activating a global storage signal to store a photosensor charge in a first storage region of each pixel of said array;

activating a first reset signal for the pixels in a first row of said array to reset a second storage region of each pixel in said first row;

sampling said reset second storage region for the pixels of said first row;

activating a third reset signal for the pixels in a second row of said array to reset a third storage region of each pixel in said second row;

sampling said reset third storage region for the pixels of said second row;

transferring said photosensor charge from said first storage region of each pixel in a first set of columns of said first and second rows of said array respectively to said second and third storage regions for the pixels in said first and second rows;

sampling said photosensor charge from said second storage region from said pixels in said first row and first set of columns; and

sampling said photosensor charge from said third storage region from said pixels in said second row and first set of columns.

2. The method of claim 1, further comprising the steps of:

transferring said photosensor charge from said first storage region of each pixel in a second set of columns of said first and second rows of said array respectively to said second and third storage regions for the pixels in said first and second rows;

sampling said photosensor charge from said second storage region from said pixels in said first row and first set of columns; and

sampling said photosensor charge from said third storage region from said pixels in said second row and first set of columns,

wherein said first and second sets of columns are alternating columns.

3. The method of claim 2, wherein said step of sampling said reset second storage region comprises:

storing charge from said reset second storage region in a first pair of sampling capacitors.

4. The method of claim 3, wherein said step of sampling said reset third storage region comprises:

storing charge from said reset third storage region in a second pair of sampling capacitors.

5. The method of claim 4, wherein said step of sampling said photosensor charge from said second storage region comprises:

storing said photosensor charge from said second storage region in said first pair of sampling capacitors.

6. The method of claim 5, wherein said step of sampling said photosensor charge from said third storage region comprises:

storing said photosensor charge from said third storage region in said second pair of sampling capacitors.