ABSTRACT

Disclosed is a semiconductor device comprising a substrate including an active pattern, a channel pattern on the active pattern and including semiconductor patterns spaced apart from and vertically stacked on each other, a source/drain pattern connected to the semiconductor patterns having a p-type, a gate electrode on the semiconductor patterns and including inner electrodes between neighboring semiconductor patterns and an outer electrode on an uppermost semiconductor pattern, and a gate dielectric layer between the gate electrode and the semiconductor patterns and including an inner gate dielectric layer adjacent to the inner electrode and an outer gate dielectric layer that extends from bottom to lateral surfaces of the outer electrode. The outer electrode and the outer gate dielectric layer have an inverted T shape.

FIG. 5B