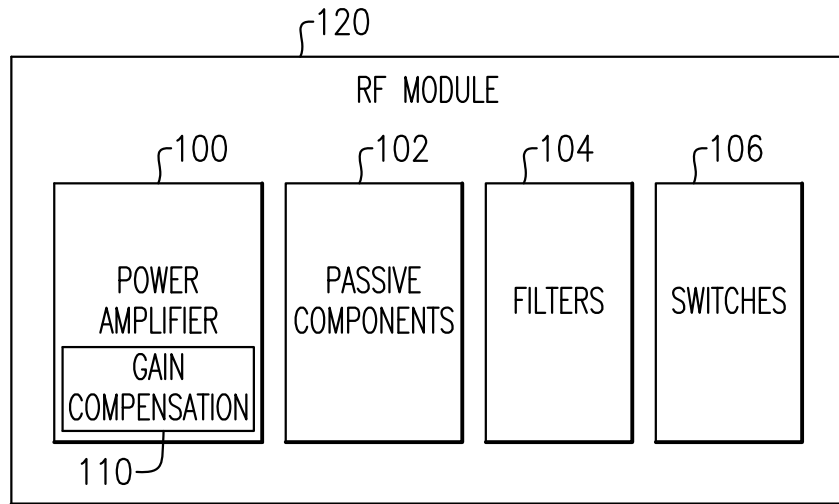
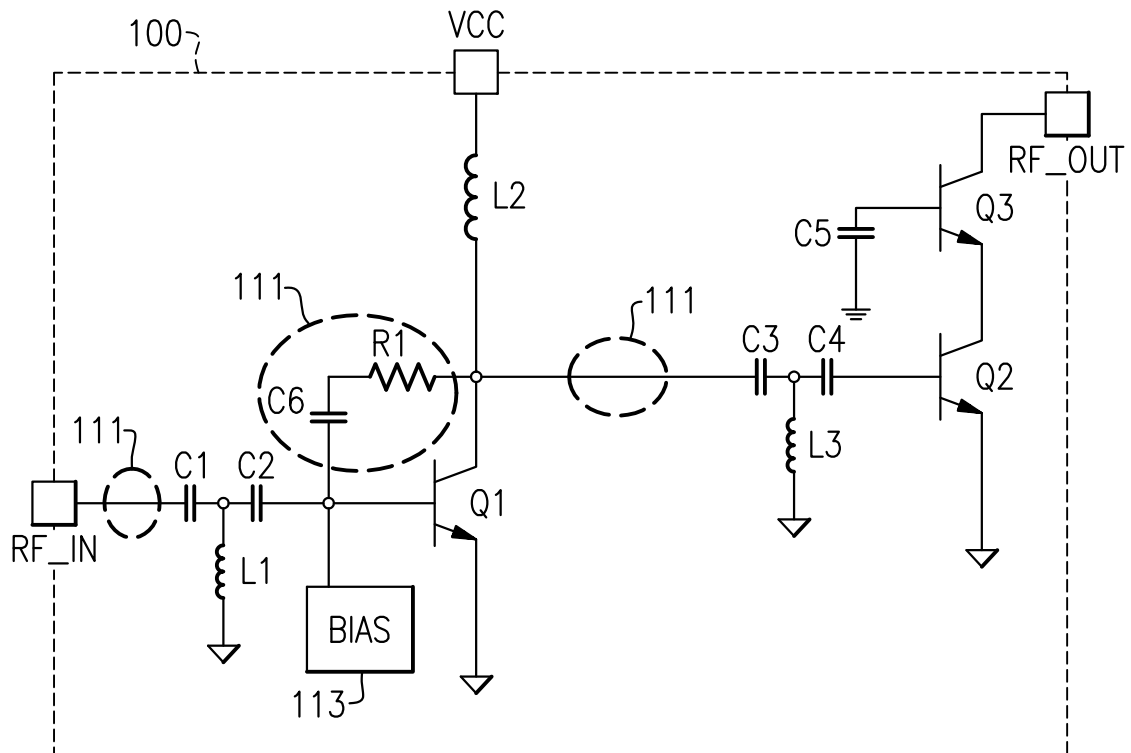


**FIG.1****FIG.2**

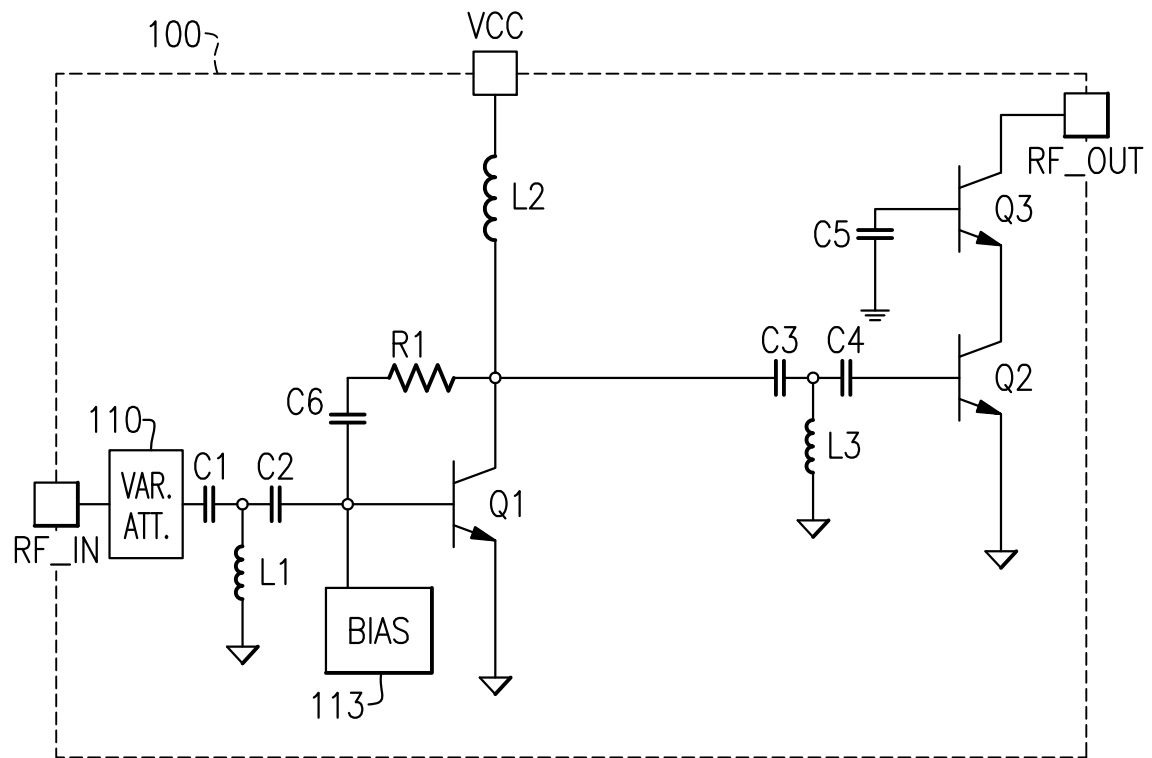
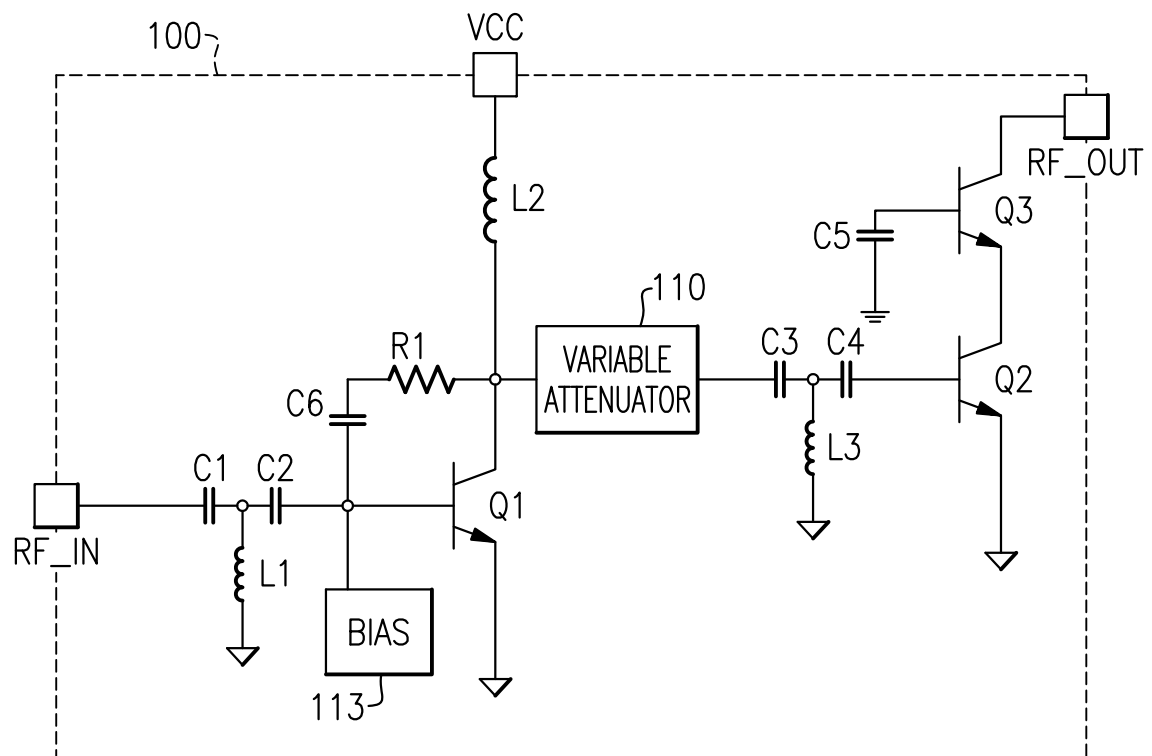
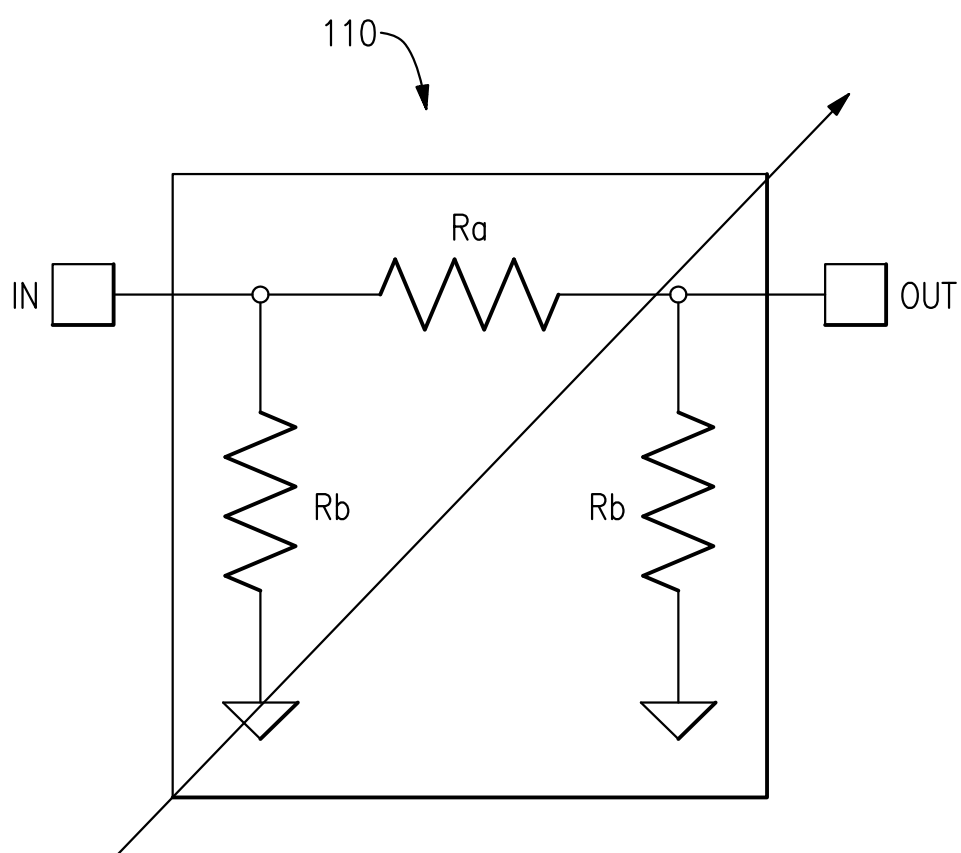
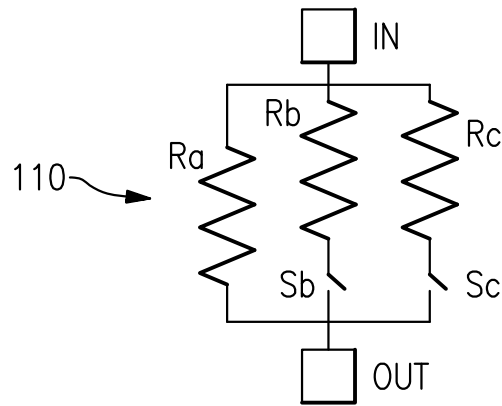
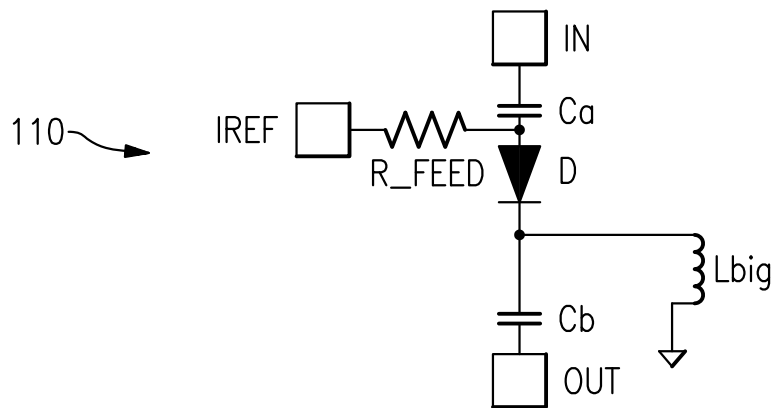
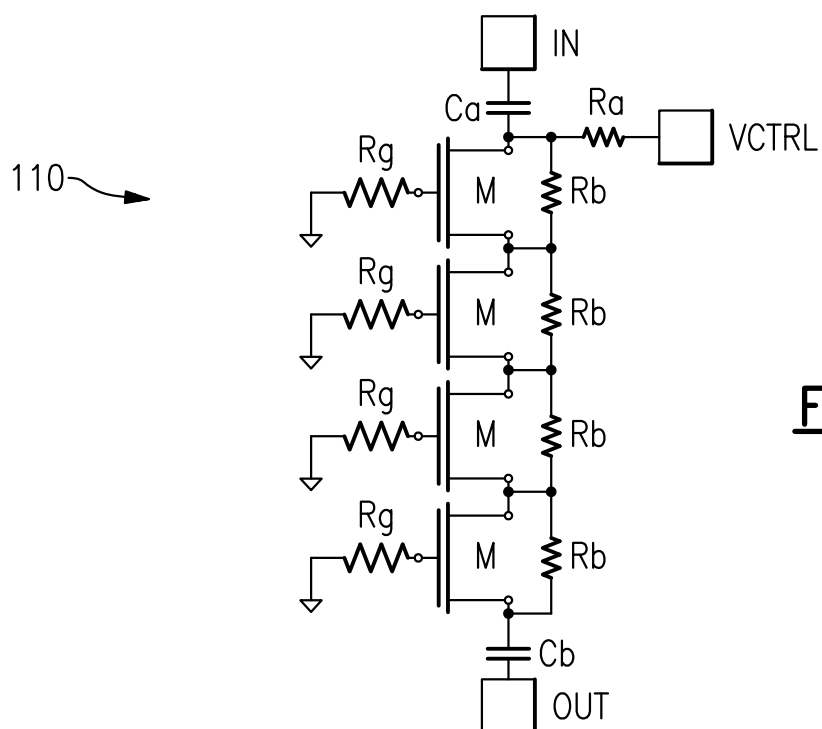
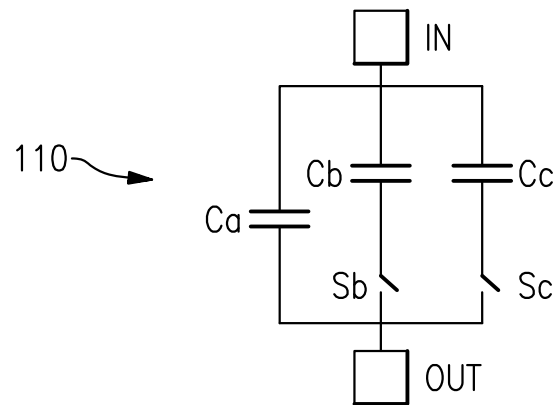
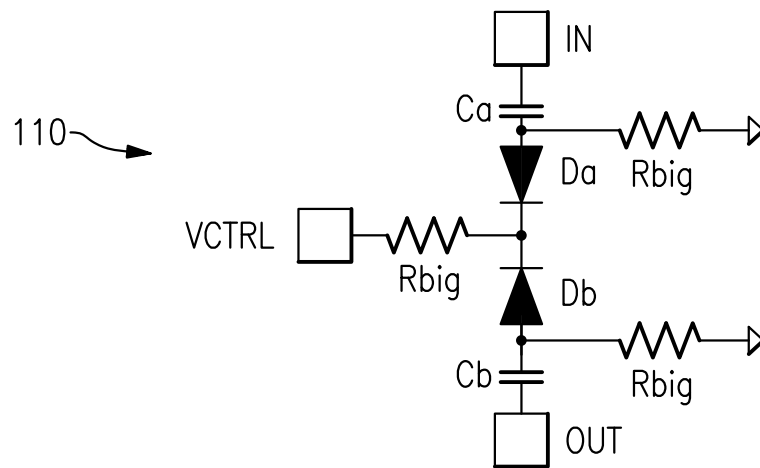
**FIG.3****FIG.4**

FIG.6

FIG.7

**FIG.8A****FIG.8B****FIG.8C**

**FIG. 9A****FIG. 9B**

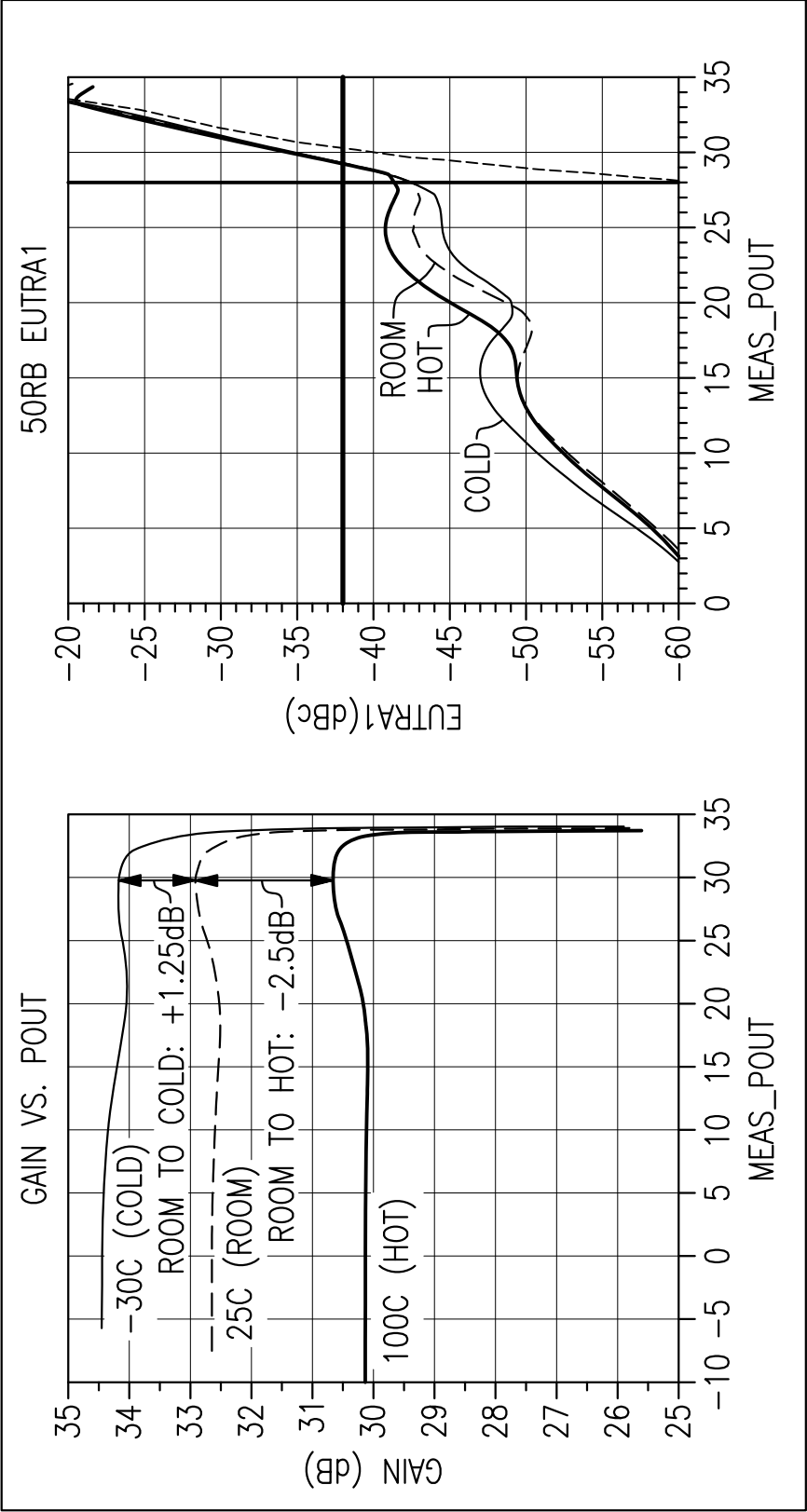


FIG.10

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CAPACITANCE VS. VCTRL AT 1800MHz

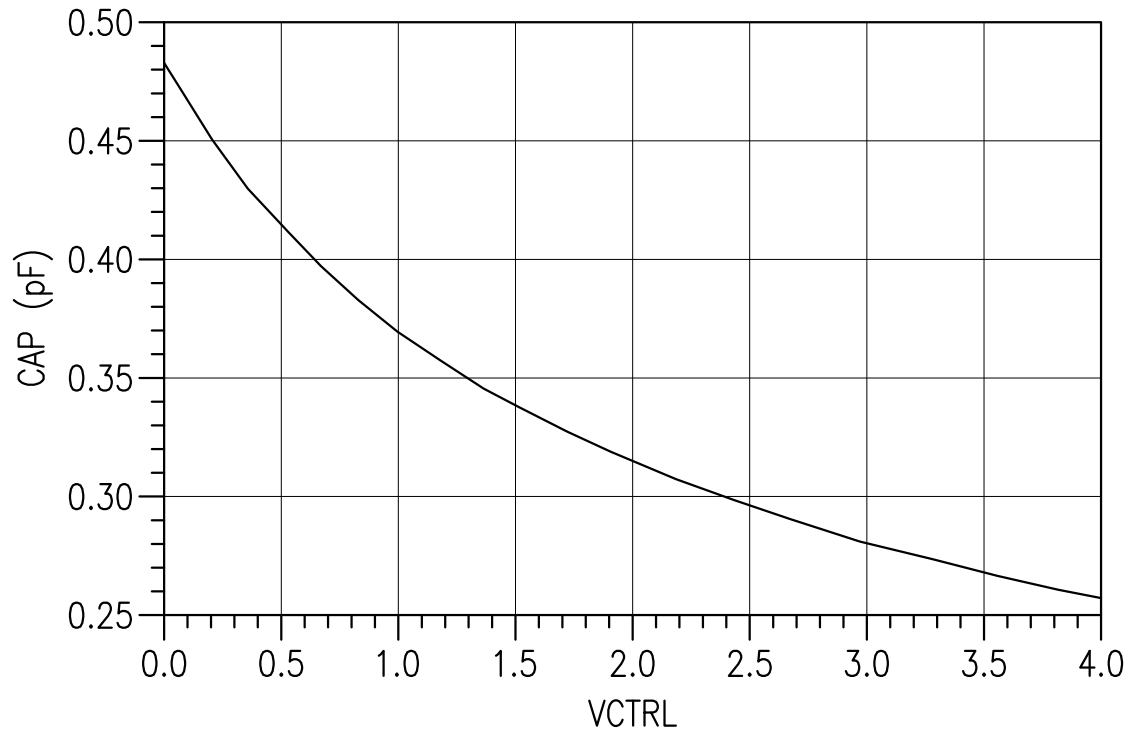


FIG.11A

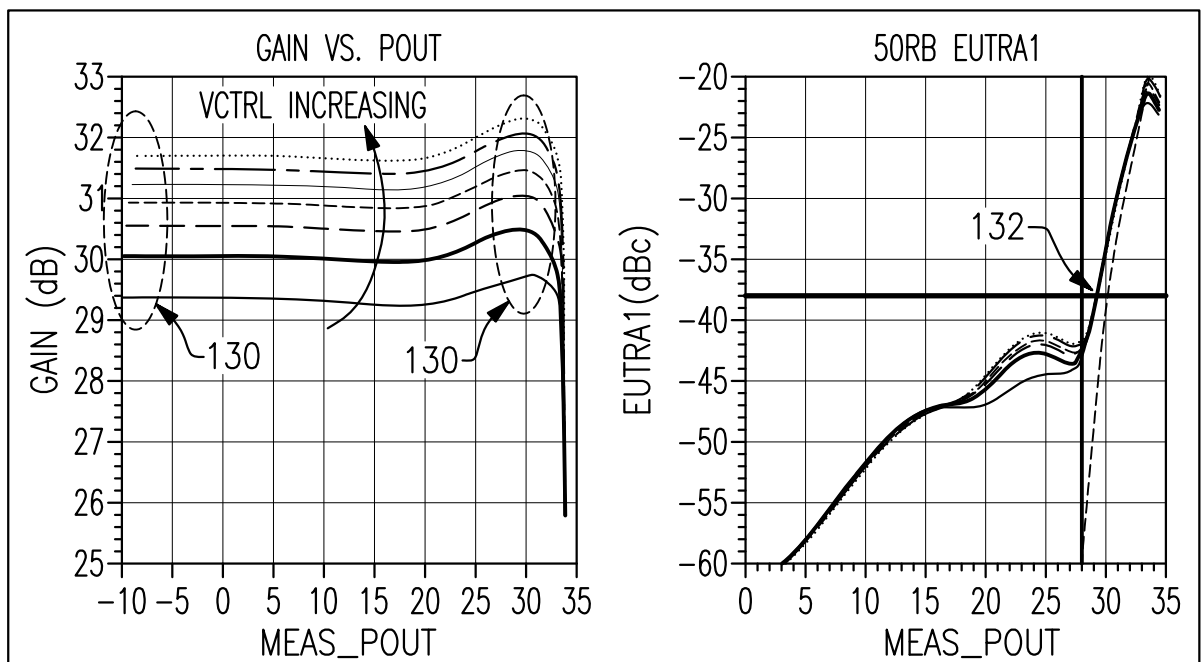


FIG.11B

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VCTRL VS. TEMP

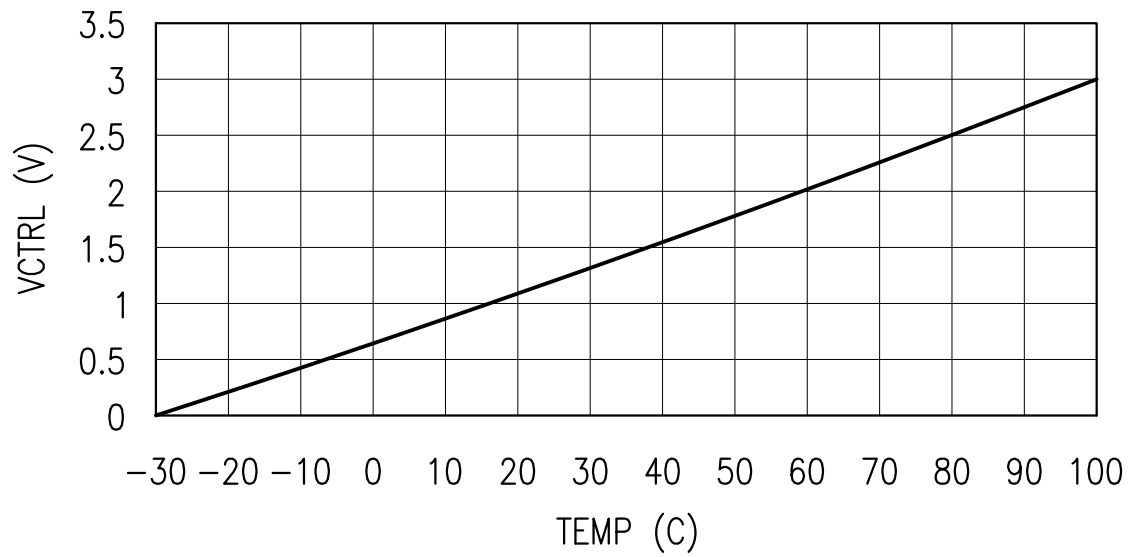


FIG.11C

IREF TC VS. TEMP

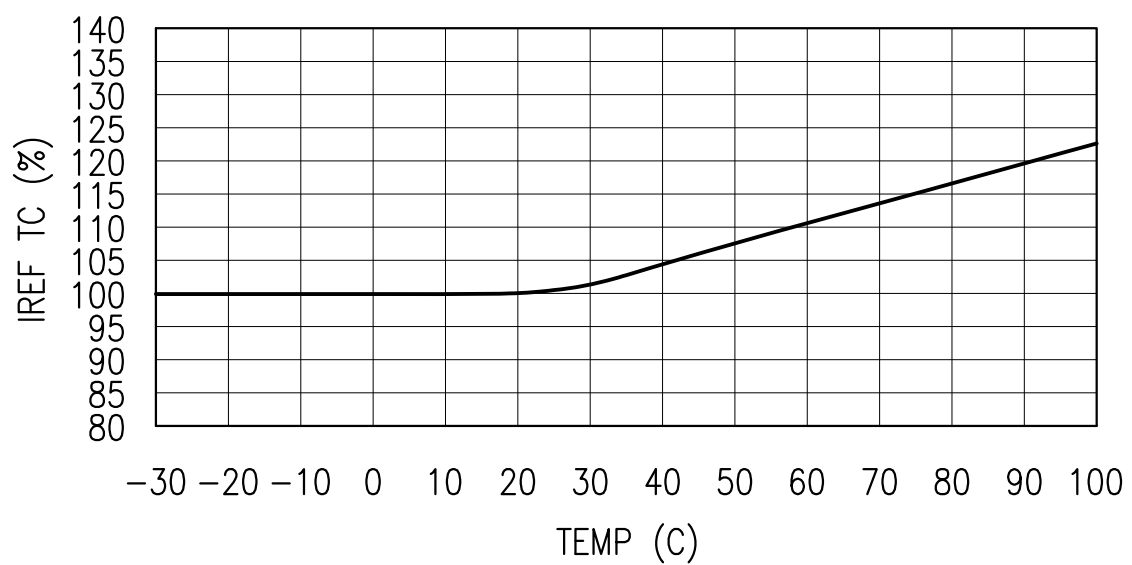


FIG.11D

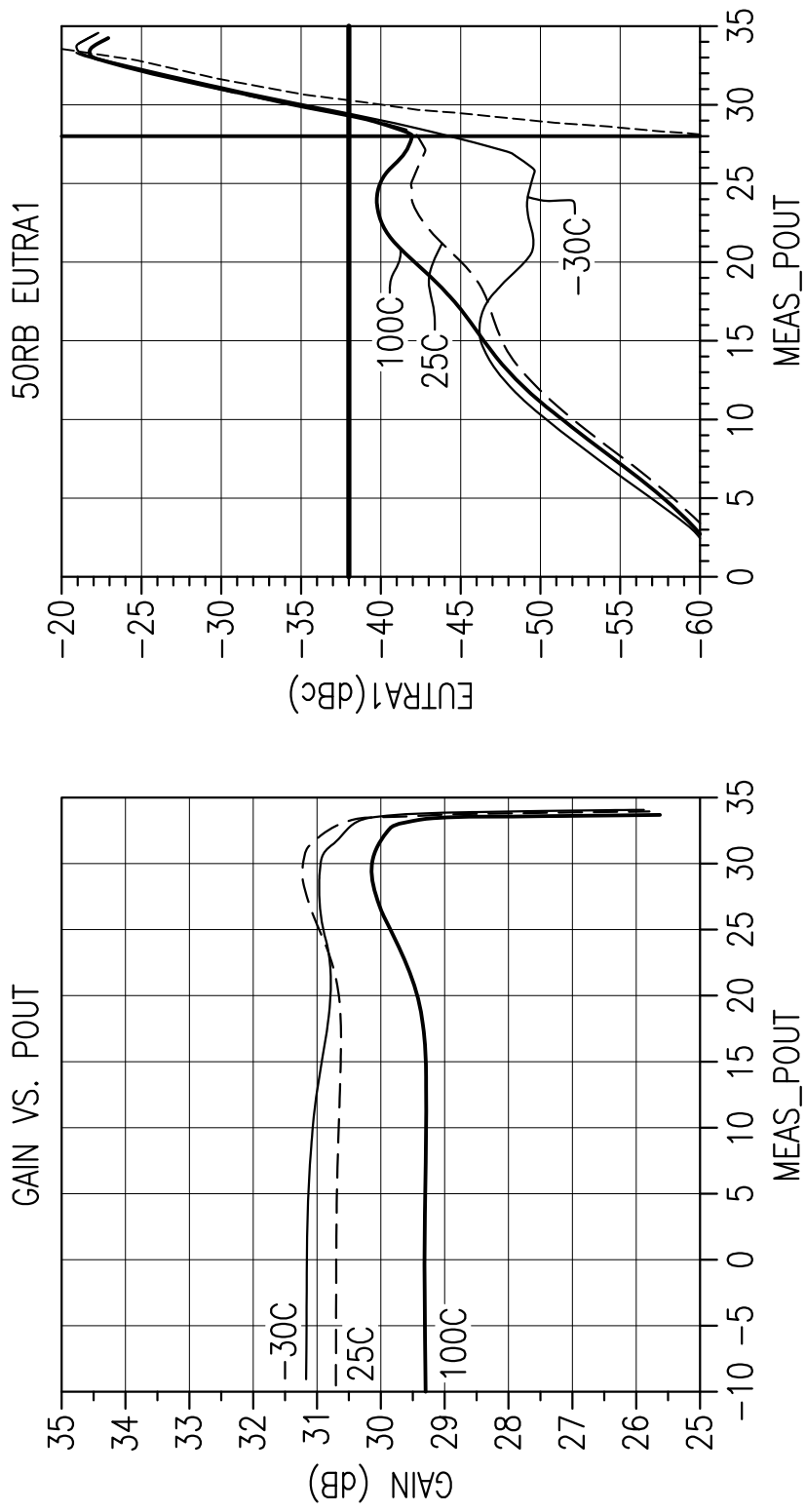


FIG.11E

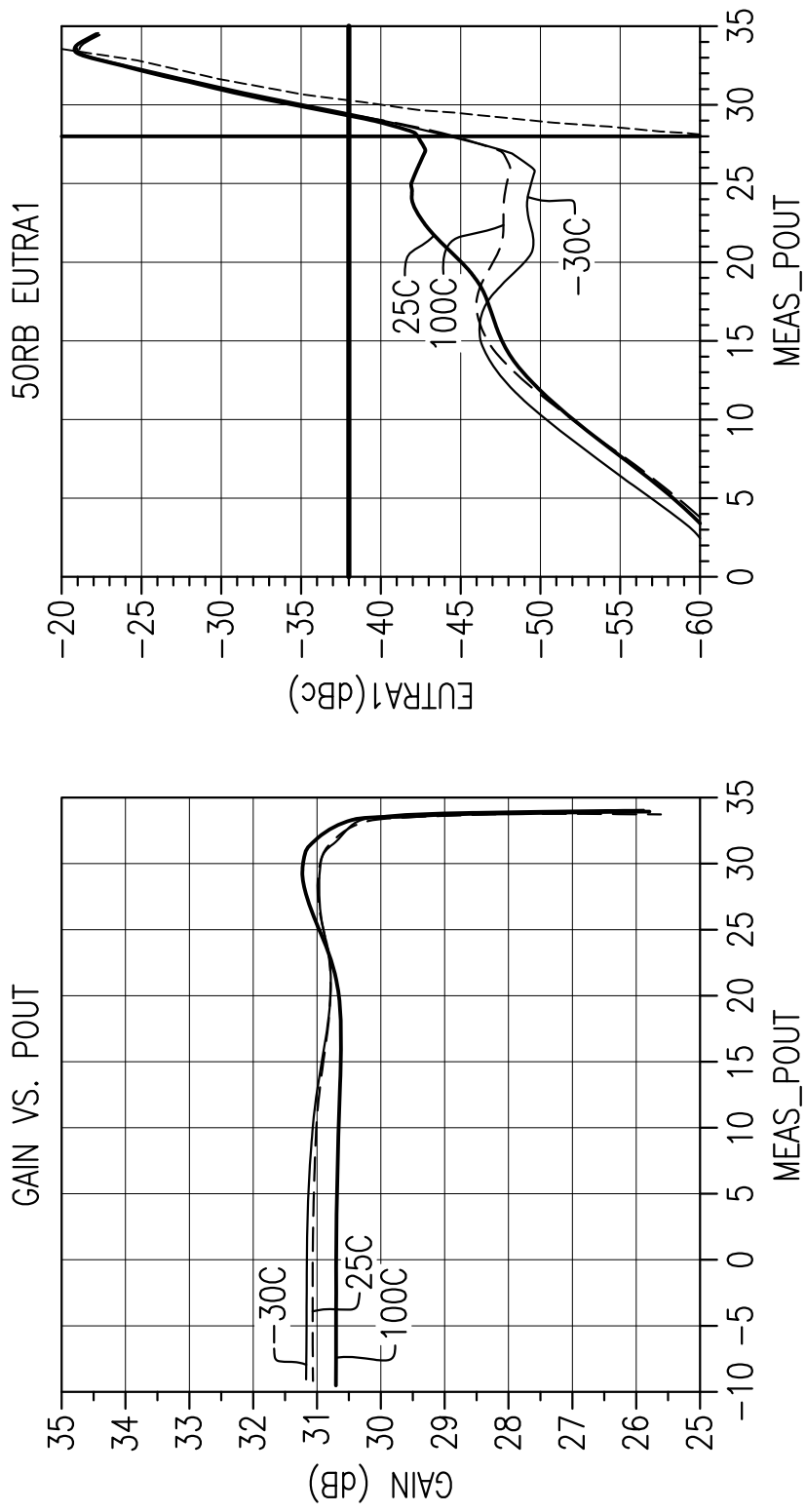


FIG.11F

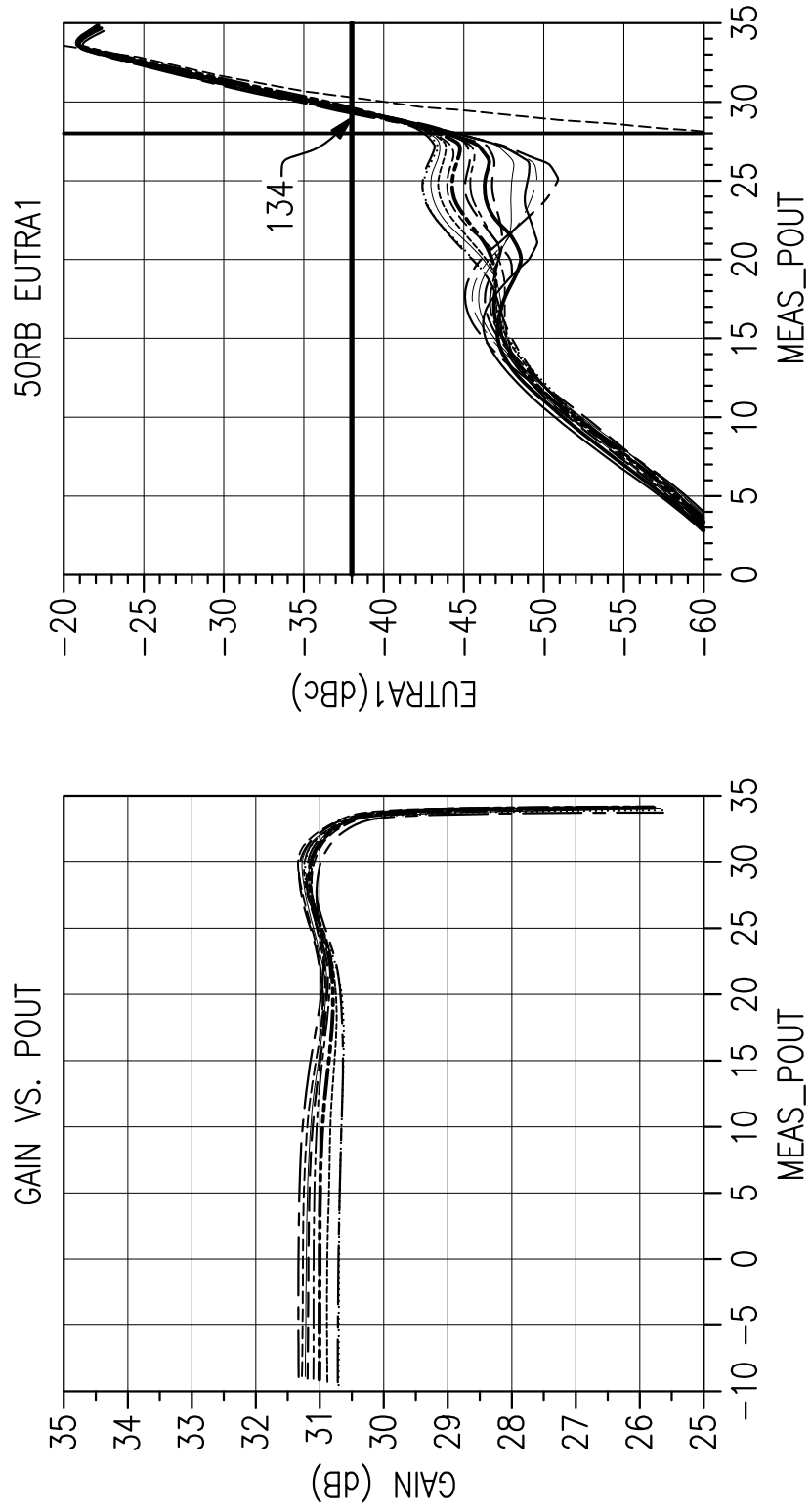


FIG.11G

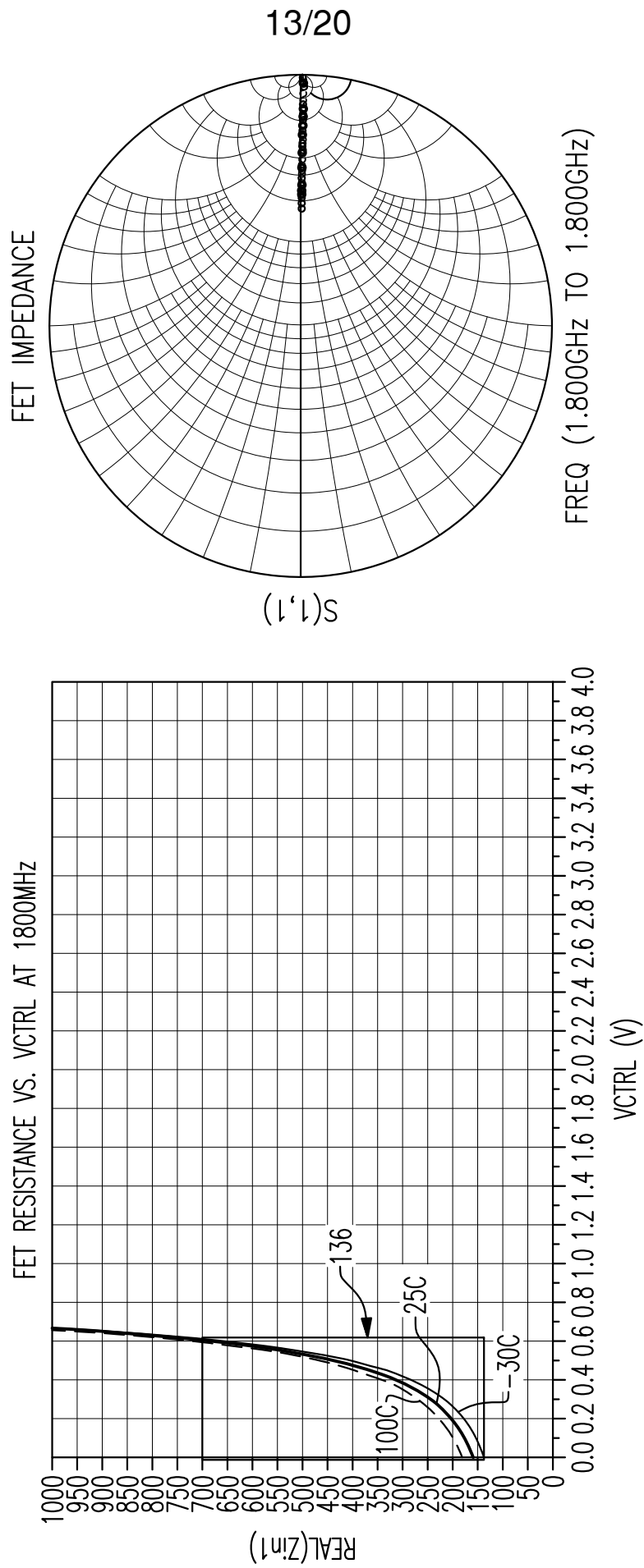


FIG.12A

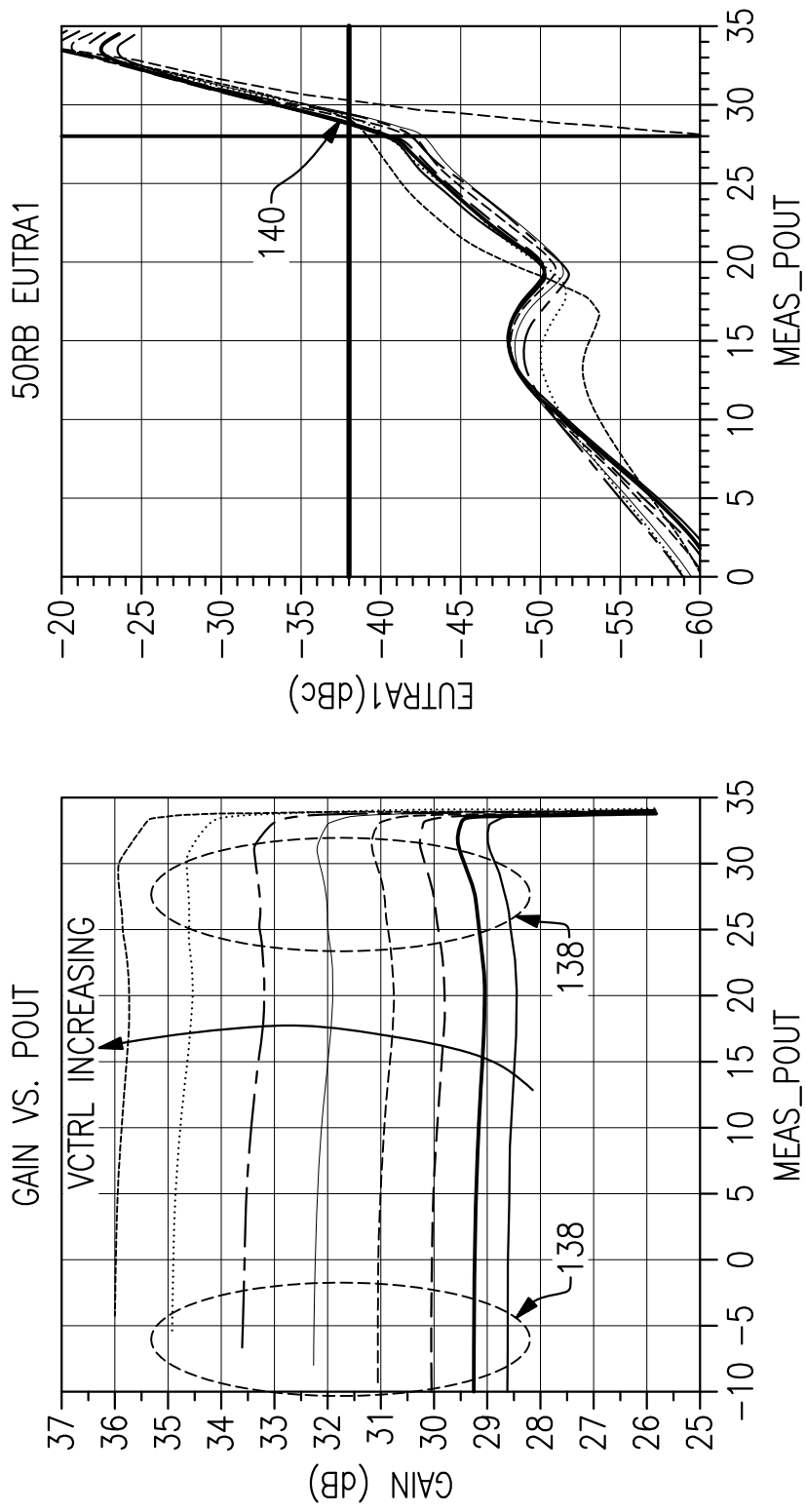


FIG.12B

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VCTRL VS. TEMP

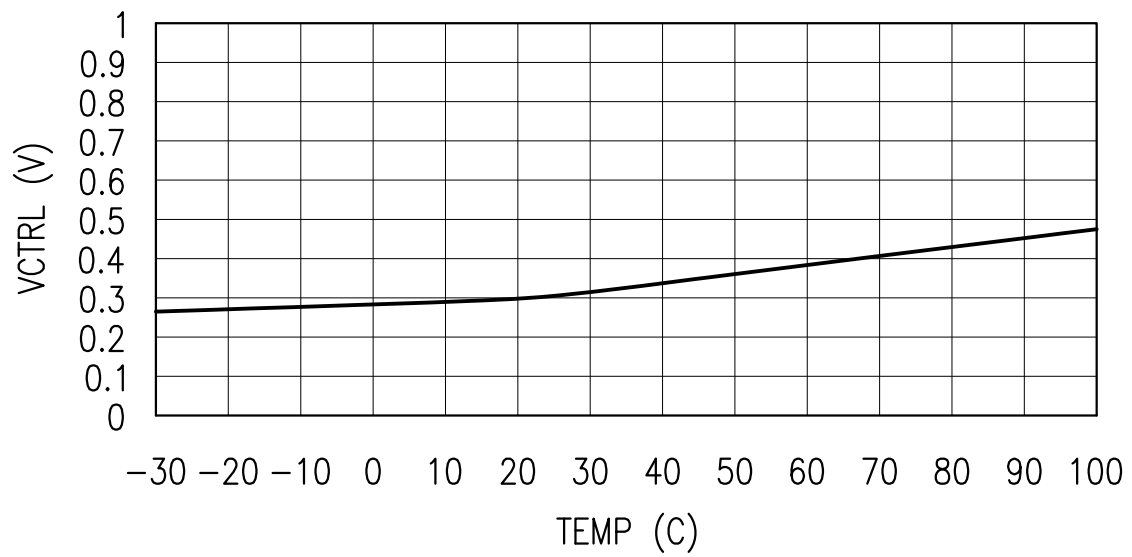


FIG.12C

IREF TC VS. TEMP

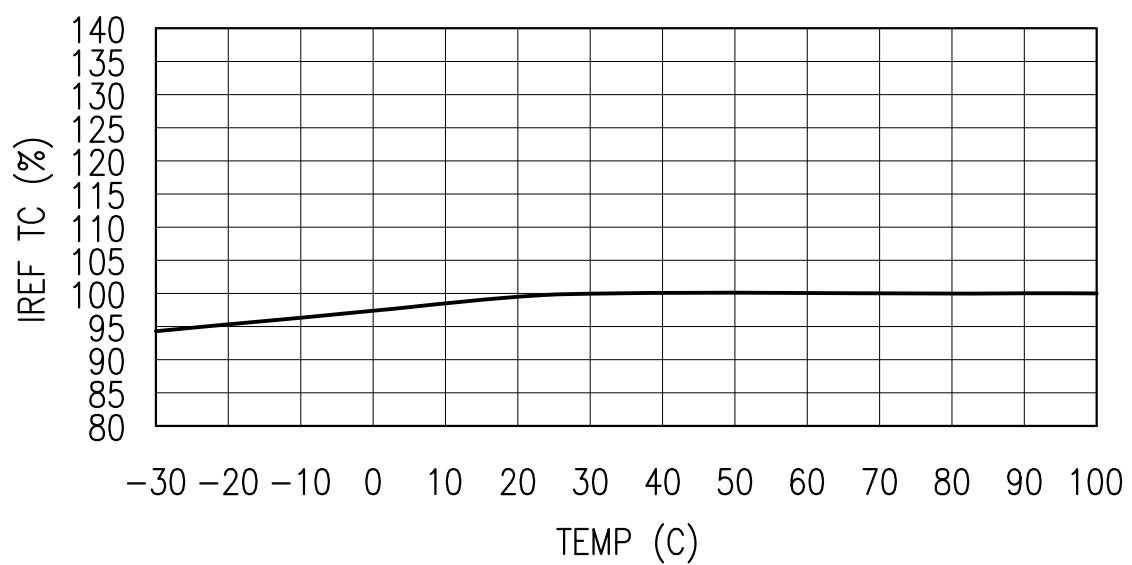


FIG.12D

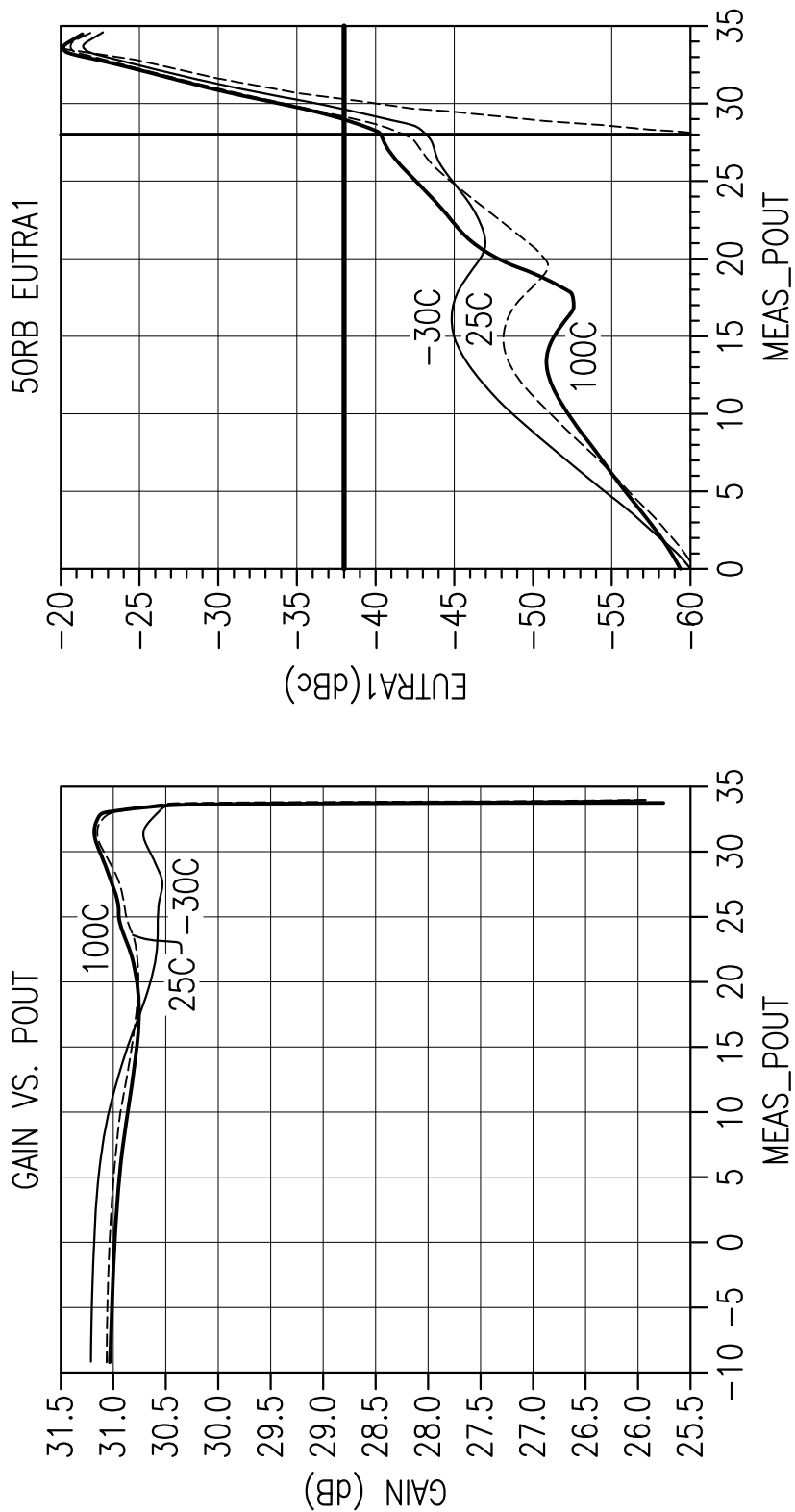


FIG.12E

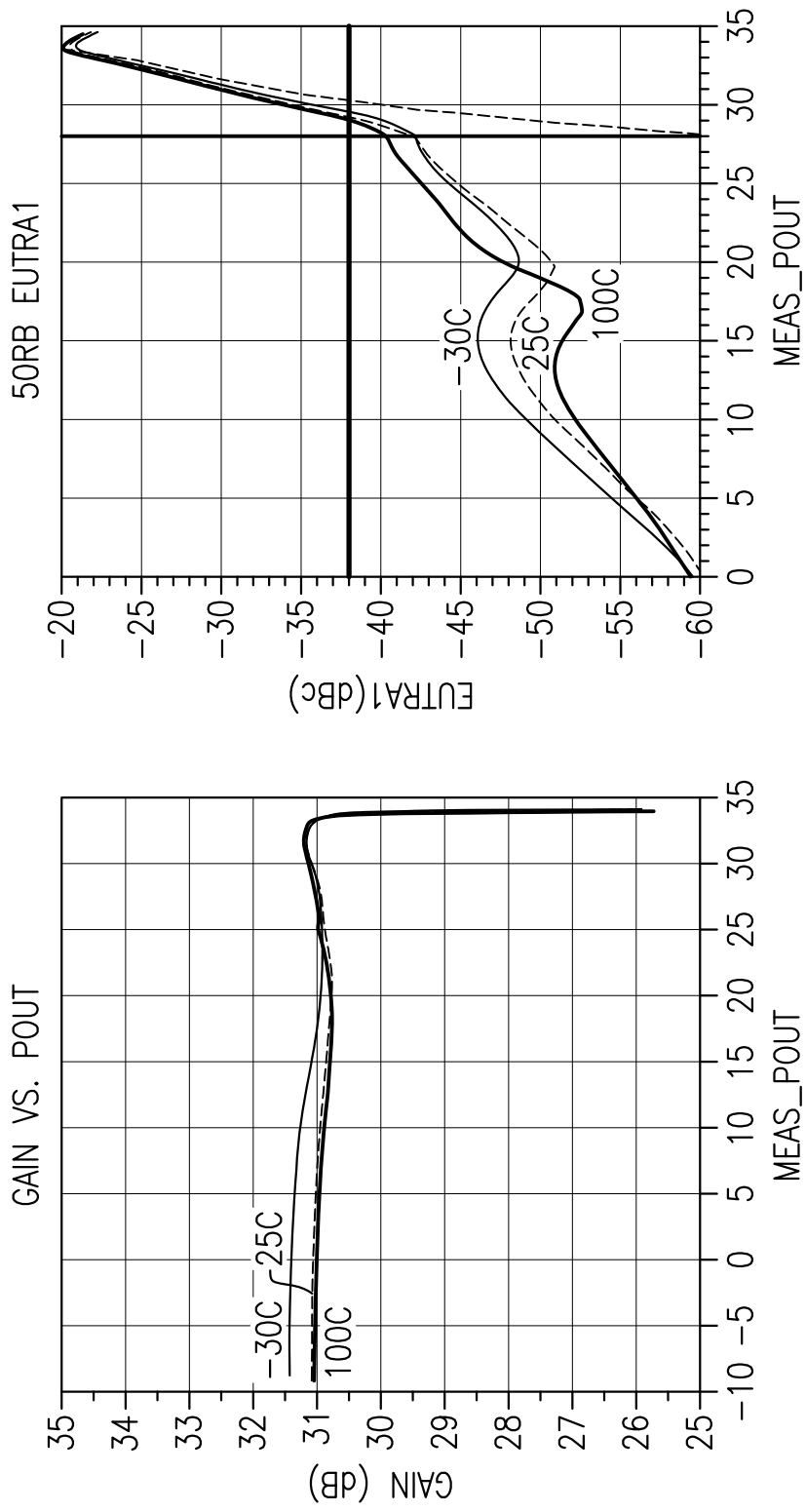


FIG.12F

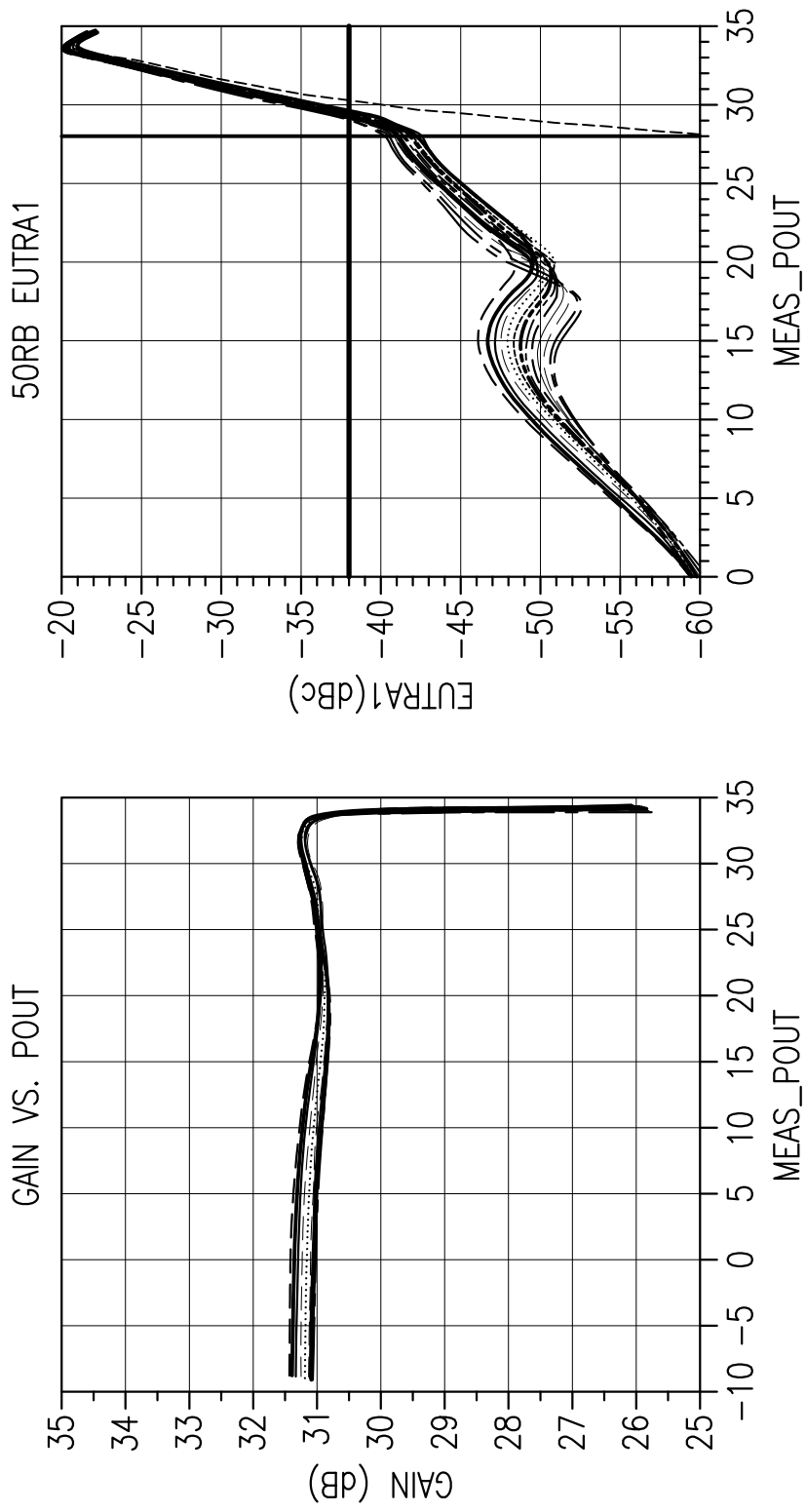


FIG.12G

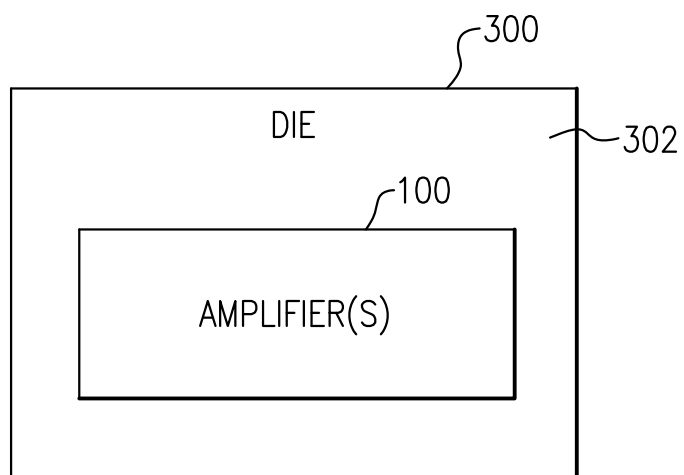


FIG.13

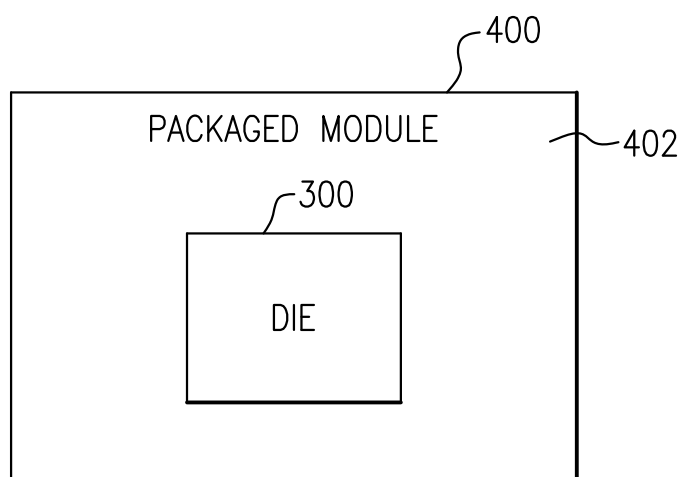


FIG.14

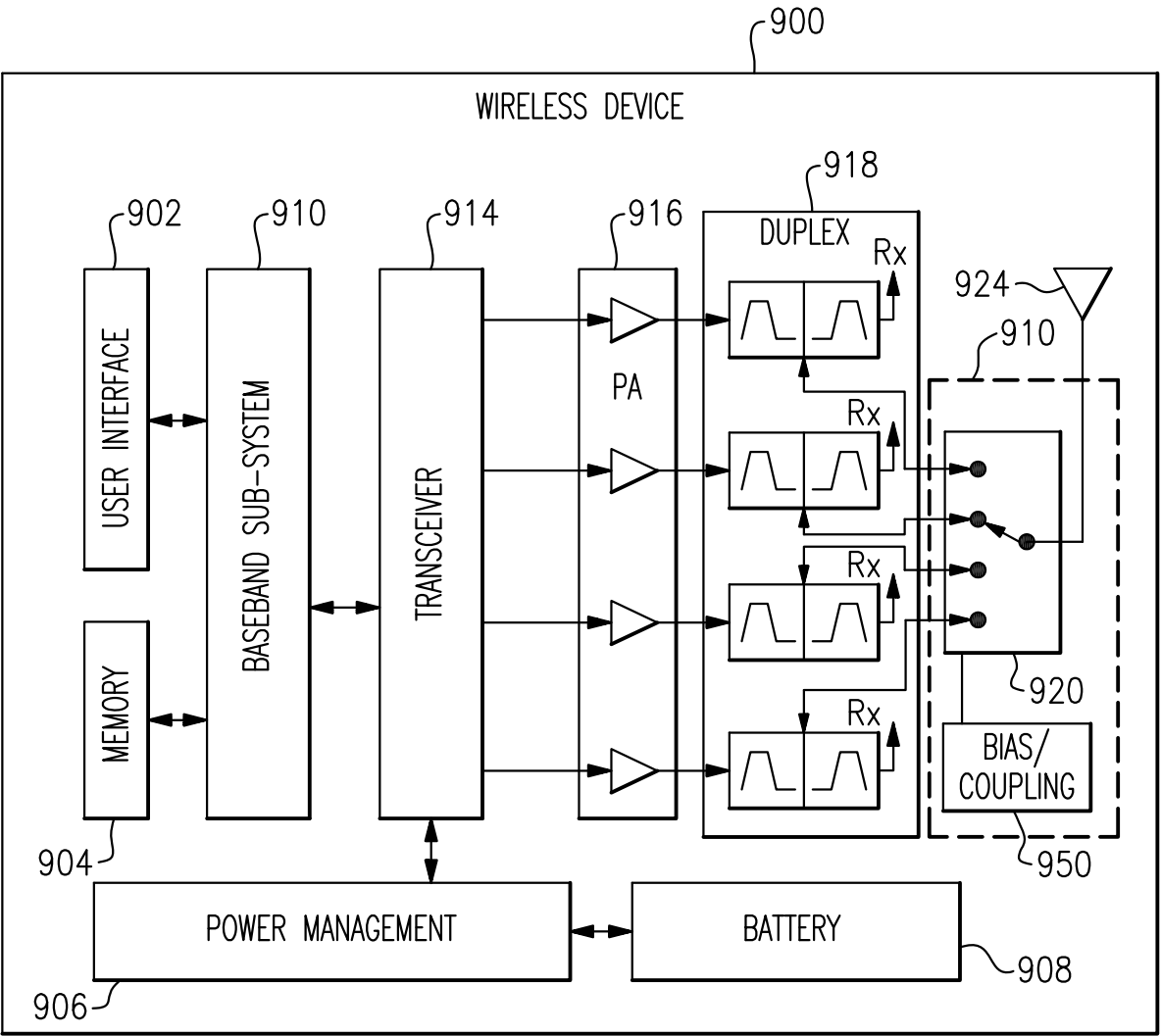


FIG.15