thickness that physically and electrically enables the formation of active and/or passive device structures.

[0047] A first device 108 can be formed over, on and/or within the substrate 106 by conventional deposition, patterning, photolithography, and etching techniques known in the semiconductor processing industry for the manufacture of active and/or passive devices. In some embodiments, the first device 108 may include one or more of a PFET device, an NFET device, and/or a combination thereof (i.e. – a CMOS device), even though only one of the first device 108 is depicted.

[0048] In general, the first device 108 includes a gate 110, a gate dielectric 112 under the gate 110, a channel 114, a liner 116, a spacer 118, a source/drain extension 120, and a source/drain 122.

[0049] In some embodiments, the gate 110 may be formed from conventional materials including doped and undoped semiconducting materials (such as, for example, polySi, amorphous Si, or SiGe), a metal, a metallic alloy, a silicide, or a combination thereof, for example. In other embodiments, the gate 110 may also include any conducting material or composition that becomes amorphous upon implantation. The gate dielectric 112 may be made from materials including, but not limited to, silicon oxide, silicon oxynitride, silicon nitride, a silicon oxide/nitride/oxide stack, a high-k dielectric material (i.e. – one having a dielectric constant value greater than silicon oxide), or a combination thereof. However, it is to be understood that the type of material chosen for the gate dielectric 112 is not limited to the above examples; for example, the gate dielectric 112 may include any material that permits induction of a charge in the channel 114 when an appropriate voltage is applied to the gate 110. Accordingly, other materials, which may be known to those skilled in the art for gate structures, may also be used for the gate 110 and the gate dielectric 112.

[0050] Generally, the thickness of the gate 110 is between about 500 angstroms and about 3000 angstroms and the thickness of the gate dielectric 112 is between about 10 angstroms and about 50 angstroms. However, larger or smaller thicknesses of the gate 110 and the gate dielectric 112 may be appropriate depending on the design specifications of the first device 108.

[0051] The liner 116 may include dielectric materials such as an oxide, a nitride, or a combination thereof, but preferably includes silicon dioxide. The spacer 118 may also be formed from conventional dielectric materials such as an oxide, a nitride, or a combination thereof, but preferably includes silicon nitride. However, it is to be understood that the type of materials chosen for the liner 116 and the spacer 118 are not limited to the above examples

What is claimed is:

1. An integrated circuit system comprising:

providing a substrate including a first region and a second region;

forming a first device over the first region and a resistance device over the second region;

forming a first dielectric layer and a second dielectric layer over the substrate;

removing a portion of the second dielectric layer; and

annealing the integrated circuit system to remove dopant from the resistance device.

2. The system as claimed in claim 1 wherein:

forming the first dielectric layer includes forming an oxide and forming the second dielectric layer includes forming a nitride.

3. The system as claimed in claim 1 wherein:

removing a portion of the second dielectric layer includes removing the second dielectric layer from over the first device.

4. The system as claimed in claim 1 wherein:

annealing the integrated circuit system includes forming the resistance device with a sheet resistance value between about 700 ohms/square to about 900 ohms/square.

5. The system as claimed in claim 1 further comprising:

configuring the density of the second dielectric layer to alter the resistivity of the resistance device.

6. An integrated circuit system comprising:

providing a substrate including a first region and a second region;

forming a first device over the first region and a resistance device over the second region;

forming a first dielectric layer over the substrate;

processing the first dielectric layer with a hydrogen treatment;

forming a second dielectric layer over the first dielectric layer;

removing a portion of the second dielectric layer; and

annealing the integrated circuit system to remove dopant from the resistance device.

7. The system as claimed in claim 6 wherein:

processing the first dielectric layer with a hydrogen treatment includes utilizing a hydrogen forming gas anneal.

8. The system as claimed in claim 6 wherein:

processing the first dielectric layer with a hydrogen treatment includes utilizing a hydrogen plasma treatment.

9. The system as claimed in claim 6 wherein:

forming the second dielectric layer over the first dielectric layer prevents deposition of an electrical contact over the resistance device.

10. The system as claimed in claim 6 further comprising:

configuring the density of the second dielectric layer to alter the resistivity of the resistance device.

11. An integrated circuit system comprising:

providing a substrate including a first region and a second region;

forming a first device and a second device over the first region and a resistance device over the second region;

forming a first dielectric layer and a second dielectric layer over the substrate;

removing a portion of the second dielectric layer; and

annealing the integrated circuit system to remove dopant from the resistance device.

12. The system as claimed in claim 11 wherein:

forming the first dielectric layer includes forming an oxide and forming the second dielectric layer includes forming a nitride.

13. The system as claimed in claim 11 wherein:

removing a portion of the second dielectric layer includes removing the second dielectric layer from over the first region.

14. The system as claimed in claim 11 wherein:

removing a portion of the second dielectric layer includes removing the second dielectric layer from over the second device or removing the second dielectric layer from over the first device and the second device.

15. The system as claimed in claim 11 wherein:

removing a portion of the second dielectric layer includes removing the second dielectric layer from over the first region either before annealing or after annealing.

16. The system as claimed in claim 11 wherein:

annealing the integrated circuit system includes a stress memorization transfer process.

17. The system as claimed in claim 11 wherein:

providing the substrate includes providing the substrate with a crystalline plane that is rotated about forty-five degrees.

18. The system as claimed in claim 11 further comprising:

processing the first dielectric layer with a hydrogen treatment.

19. The system as claimed in claim 11 further comprising:

configuring the density of the second dielectric layer to alter the resistivity of the resistance device.

20. The system as claimed in claim 11 further comprising:

forming an electrical contact over a gate and a source/drain of the first device and the second device.

What is claimed is:

1. A method of manufacture of an integrated circuit system comprising:

providing a substrate including a first region and a second region;

forming a first device over the first region, the first device having a first gate over a first gate dielectric;

forming a resistance device over the second region, the resistance device having a second gate over a second gate dielectric similar to the first gate and the first gate dielectric of the first device;

forming a first dielectric layer and a second dielectric layer over the substrate wherein forming the second dielectric layer includes increasing the density of the second dielectric layer to increase a resistance value of the resistance device;

removing a portion of the second dielectric layer; and

annealing the integrated circuit system to remove dopant from the resistance device.

2. The method as claimed in claim 1 wherein:

forming the first dielectric layer includes forming an oxide and forming the second dielectric layer includes forming a nitride.

3. The method as claimed in claim 1 wherein:

removing a portion of the second dielectric layer includes removing the second dielectric layer from over the first device.

4. The method as claimed in claim 1 wherein:

annealing the integrated circuit system includes forming the resistance device with a sheet resistance value between about 700 ohms/square to about 900 ohms/square.

5. The method as claimed in claim 1 wherein:

increasing the density of the second dielectric layer includes forming the second dielectric layer by rapid thermal chemical vapor deposition.

6. A method of manufacture of an integrated circuit system comprising:

providing a substrate including a first region and a second region;

forming a first device over the first region, the first device having a first gate over a first gate dielectric;

forming a resistance device over the second region, the resistance device having a second gate over a second gate dielectric similar to the first gate and the first gate dielectric of the first device;

forming a first dielectric layer over the substrate;

processing the first dielectric layer with a hydrogen treatment;

forming a second dielectric layer over the first dielectric layer wherein forming the second dielectric layer includes increasing the density of the second dielectric layer to increase a resistance value of the resistance device;

removing a portion of the second dielectric layer; and

annealing the integrated circuit system to remove dopant from the resistance device.

7. The method as claimed in claim 6 wherein:

processing the first dielectric layer with a hydrogen treatment includes utilizing a hydrogen forming gas anneal.

8. The method as claimed in claim 6 wherein:

processing the first dielectric layer with a hydrogen treatment includes utilizing a hydrogen plasma treatment.

9. The method as claimed in claim 6 wherein:

forming the second dielectric layer over the first dielectric layer prevents deposition of an electrical contact over the resistance device.

10. The method as claimed in claim 6 wherein:

increasing the density of the second dielectric layer includes forming the second dielectric layer by rapid thermal chemical vapor deposition.

11. A method of manufacture of an integrated circuit system comprising:

providing a substrate including a first region and a second region;

forming a first device and a second device over the first region, the first device having a first gate over a first gate dielectric;

forming a resistance device over the second region, the resistance device having a second gate over a second gate dielectric similar to the first gate and the first gate dielectric of the first device;

forming a first dielectric layer and a second dielectric layer over the substrate wherein forming the second dielectric layer includes increasing the density of the second dielectric layer to increase a resistance value of the resistance device;

removing a portion of the second dielectric layer; and

annealing the integrated circuit system to remove dopant from the resistance device.

12. The method as claimed in claim 11 wherein:

forming the first dielectric layer includes forming an oxide and forming the second dielectric layer includes forming a nitride.

13. The method as claimed in claim 11 wherein:

removing a portion of the second dielectric layer includes removing the second dielectric layer from over the first region.

14. The method as claimed in claim 11 wherein:

removing a portion of the second dielectric layer includes removing the second dielectric layer from over the second device or removing the second dielectric layer from over the first device and the second device.

15. The method as claimed in claim 11 wherein:

removing a portion of the second dielectric layer includes removing the second dielectric layer from over the first region either before annealing or after annealing.

16. The method as claimed in claim 11 wherein:

annealing the integrated circuit system includes a stress memorization transfer process.

17. The method as claimed in claim 11 wherein:

providing the substrate includes providing the substrate with a crystalline plane that is rotated about forty-five degrees.

18. The method as claimed in claim 11 further comprising:

processing the first dielectric layer with a hydrogen treatment.

19. The method as claimed in claim 11 wherein:

increasing the density of the second dielectric layer includes forming the second dielectric layer by rapid thermal chemical vapor deposition.

20. The method as claimed in claim 11 further comprising:

forming an electrical contact over the first gate and a source/drain of the first device and the second device.