support 248 that are brought together to enclose semiconductor die 124 and TSV semiconductor die 212 with open space 250. MUF material 242 in a liquid state is injected into one side of chase mold 244 with nozzle 252 while an optional vacuum assist 254 draws pressure from the opposite side to uniformly fill open space 250 around semiconductor die 124 and TSV semiconductor die 212 with the MUF material. MUF material 242 can be polymer composite material, such as epoxy resin with filler, epoxy acrylate with filler, or polymer with proper filler. MUF material 242 is formed around and between semiconductor die 124 and TSV semiconductor die 212 and cured, as shown in FIG. 7n.

In FIG. 7o, a portion of encapsulant 228 ~~240 or MUF material 242~~ is removed by grinder 258 to expose conductive vias 218.

FIG. 7p shows semiconductor die 124 and TSV semiconductor die 212 surrounded by encapsulant 240 or MUF material 242 after the grinding operation. A build-up interconnect structure 260 is formed over active surface 214 of TSV semiconductor die 212 opposite semiconductor die 124. The build-up interconnect structure 260 includes an electrically conductive layer or RDL 262 formed using a patterning and metal deposition process such as sputtering, electrolytic plating, and electroless plating. Conductive layer 262 can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. Conductive layer 262 includes horizontal and vertical portions for electrical interconnect. One portion of conductive layer 262 is electrically connected to conductive vias 218. Other portions of conductive layer 262 can be electrically common or electrically isolated depending on the design and function of semiconductor die 124 and 212.

An insulating or passivation layer 264 is formed

Claims

What is claimed:

1. A method of making a semiconductor device, comprising:

providing a semiconductor wafer ~~having first and second opposing surfaces~~ including an active surface and a second surface opposite the active surface;

forming a plurality of conductive vias partially through the ~~first~~ active surface of the semiconductor wafer;

singulating the semiconductor wafer ~~into a plurality of~~ to separate a first semiconductor die;

~~providing a carrier;~~

~~mounting the first semiconductor die to the carrier;~~

~~mounting~~ disposing a second semiconductor die ~~to~~ over the first semiconductor die with the active surface oriented toward the second semiconductor die;

depositing an encapsulant over and around the first and second semiconductor dies ~~and carrier~~;

removing a portion of the second surface to expose a surface of the conductive vias coplanar with the second surface and the encapsulant~~the carrier and a portion of the second surface to expose the conductive vias~~; and

forming an interconnect structure over ~~a surface of the first semiconductor die opposite the second semiconductor die~~ the first semiconductor die opposite the second semiconductor die, the interconnect structure including a first insulating layer and a first conductive layer.

2. The method of claim 1, wherein a footprint of the second semiconductor die is larger than a footprint of the first semiconductor die.

3. The method of claim 1, further including:

forming a second conductive layer over the ~~first surface of the substrate prior to mounting the second semiconductor die, the conductive layer being electrically connected to the conductive vias~~ active surface of the first semiconductor die prior to mounting the second semiconductor die, the second conductive layer being electrically connected to the conductive vias; and

forming ~~an~~ a second insulating layer over the ~~first surface of the substrate~~ active surface of the first semiconductor die.

4. The method of claim 1, further including depositing a mold underfill material between the first semiconductor die and second semiconductor die.

5. The method of claim 1, wherein the second semiconductor die includes a memory device.

6. The method of claim 1, further including stacking a plurality of second semiconductor die over the first semiconductor die.

7. A method of making a semiconductor device, comprising:

providing a ~~plurality of~~ first semiconductor die including an active surface and second surface;

forming a plurality of conductive vias through the active surface of the first semiconductor die;

forming a first interconnect structure over the active surface of the first semiconductor die;

~~providing a carrier;~~

~~mounting the first semiconductor die to the carrier;~~

~~mounting~~ disposing a second semiconductor die ~~to~~over the first semiconductor die~~, wherein a footprint of the second semiconductor die is larger than a footprint of the first semiconductor die~~ with the first interconnect structure between the first and second semiconductor dies, the second semiconductor die extending outside a footprint of the first semiconductor die; and

depositing an encapsulant ~~over~~ around the first and second semiconductor die~~s and carrier~~.

8. The method of claim 7, further including:

~~removing the carrier; and~~

forming ~~an~~a second interconnect structure~~ over the first semiconductor die opposite the second semiconductor die~~ including an insulating layer and conductive layer over the first semiconductor die opposite the second semiconductor die.

9. The method of claim 7, further including:

disposing the first semiconductor die over a carrier;

forming the plurality of conductive vias partially through ~~a first~~ the active surface of the first semiconductor die;

removing the carrier; and

removing a portion of a second surface of the first semiconductor opposite the ~~first~~ active surface of the first semiconductor die to expose the conductive vias.

10. The method of claim 7, ~~further including:~~

~~forming a conductive layer over the first semiconductor die prior to mounting the second semiconductor die, the conductive layer being electrically connected to the conductive vias; and~~

~~forming an insulating layer over the first semiconductor die~~ wherein the first interconnect structure includes an insulating layer and conductive layer, the conductive layer being electrically connected to the conductive vias.

11. The method of claim 7, further including depositing a mold underfill material between the first semiconductor die and second semiconductor die.

12. The method of claim 7, further including stacking a plurality of second semiconductor die over the first semiconductor die.

13. The method of claim 7, further including forming a plurality of conductive vias through the encapsulant.

14. The method of claim 7, wherein a footprint of the semiconductor die is larger than a footprint of the substrate.

145. A method of making a semiconductor device, comprising:

providing ~~a plurality of~~a first semiconductor die including an active surface and second surface;

forming a plurality of conductive vias through the active surface of the first semiconductor die and coplanar with the active surface of the first semiconductor die~~first semiconductor die~~;

providing a carrier;

mounting the first semiconductor die to the carrier;

depositing a first encapsulant over the first semiconductor die and carrier;

removing the carrier;

mounting a second semiconductor die to the first semiconductor die; and

depositing a second encapsulant over the second semiconductor diedepositing a first encapsulant over the first semiconductor die including on the active surface;

forming an interconnect structure over the second surface of the first semiconductor die, the interconnect structure including a first insulating layer and a first conductive layer;

disposing a second semiconductor die over the first semiconductor die opposite the active surface with the interconnect structure between the first and second semiconductor dies;

depositing a second encapsulant over the second semiconductor die; and

removing a portion of the first encapsulant on the active surface of the first semiconductor die.

156. The method of claim 145, wherein a footprint of the second semiconductor die is larger than a footprint of the first semiconductor die.

167. The method of claim 145, wherein the second semiconductor die includes a memory device.

~~17. The method of claim 14, further including forming an interconnect structure over the first semiconductor die opposite the second semiconductor die.~~

~~18. The method of claim 14, further including:~~

~~forming the plurality of conductive vias partially through a first surface of the first semiconductor die; and~~

~~removing a portion of a second surface of the first semiconductor opposite the first surface of the first semiconductor die to expose the conductive vias.~~

~~19. The method of claim 14, further including removing a portion of the first encapsulant to expose the conductive vias.~~

~~20~~18. The method of claim 1~~4~~5, further including depositing a mold underfill material between the first semiconductor die and second semiconductor die.

~~21. A semiconductor device, comprising:~~

~~a first semiconductor die having a plurality of conductive vias formed through the first semiconductor die;~~

~~a second semiconductor die mounted to the first semiconductor die, wherein a footprint of the second semiconductor die is larger than a footprint of the first semiconductor die;~~

~~an encapsulant deposited over the first and second semiconductor die; and~~

~~an interconnect structure formed over the first semiconductor die opposite the second semiconductor die.~~

~~22. The semiconductor device of claim 21, wherein the second semiconductor die includes a memory device.~~

~~23. The semiconductor device of claim 21, further including a mold underfill material deposited between the first and second semiconductor die.~~

~~24. The semiconductor device of claim 21, further including:~~

~~a conductive layer formed over the first semiconductor die and electrically connected to the conductive vias; and~~

~~an insulating layer formed over the first semiconductor die.~~

~~25. The semiconductor device of claim 21, further including a plurality of second semiconductor die stacked over the first semiconductor die.~~

19. A method of making a semiconductor device, comprising:

providing a substrate including a plurality of conductive vias formed through the substrate;

forming an interconnect structure over the substrate, the interconnect structure including a first insulating layer and a first conductive layer;

depositing a first encapsulant around the substrate and interconnect structure;

disposing a semiconductor die over the substrate with the interconnect structure between the substrate and semiconductor die; and

depositing a second encapsulant over the semiconductor die after disposing the semiconductor die over the substrate.

20. The method of claim 19, further including:

forming the plurality of conductive vias partially through the substrate; and

removing a portion of the substrate to expose the conductive vias.

21. The method of claim 19, wherein the substrate includes an active surface.

22. The method of claim 19, further including depositing a mold underfill material between the substrate and semiconductor die.

23. A method of making a semiconductor device, comprising:

providing a substrate;

forming an interconnect structure over the substrate by,

(a) forming a first insulating layer over the substrate, and

(b) forming a first conductive layer over the substrate;

depositing a first encapsulant over the substrate and interconnect structure;

disposing a semiconductor die over the substrate with the interconnect structure between the substrate and semiconductor die; and

depositing a second encapsulant over the semiconductor die after disposing the semiconductor die over the substrate.

24. The method of claim 23, further including:

forming a plurality of conductive vias through the substrate.

25. The method of claim 24, further including:

forming a second conductive layer over the conductive vias; and

forming a second insulating layer over the second conductive layer.

26. The method of claim 23, further including depositing a mold underfill material between the semiconductor die and the first insulating layer.

27. The method of claim 23, wherein a footprint of the semiconductor die extends outside a footprint of the substrate.

28. The method of claim 23, wherein the substrate includes an active surface.